CMOS Voltage Converters

The Intersil ICL7660 and ICL7660A are monolithic CMOS power supply circuits which offer unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of -1.5V to -10.0V and the ICL7660A does the same conversions with an input range of +1.5V to +12.0V resulting in complementary output voltages of -1.5V to -12.0V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 and ICL7660A can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input.

Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the ICL7660 and +3.5V to +12.0V for the ICL7660A), the LV pin is left floating to prevent device latchup.

Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (V_{OUT} = (-n)V_{IN})
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range
  - ICL7660 ........................................ 1.5V to 10.0V
  - ICL7660A ......................................... 1.5V to 12.0V
- ICL7660A 100% Tested at 3V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temp. and Voltage Range

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized μProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Pinouts

Ordering Information

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
</tr>
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<tbody>
<tr>
<td>ICL7660CBA</td>
<td>0 to 70</td>
<td>8 Ld SOIC (N)</td>
<td>M8.15</td>
</tr>
<tr>
<td>ICL7660CBA-T</td>
<td>0 to 70</td>
<td>8 Ld SOIC (N) Tape and Reel</td>
<td>M8.15</td>
</tr>
<tr>
<td>ICL7660CPA</td>
<td>0 to 70</td>
<td>8 Ld PDIP</td>
<td>E8.3</td>
</tr>
<tr>
<td>ICL7660MTV†</td>
<td>0 to 70</td>
<td>8 Pin Metal Can</td>
<td>T8.C</td>
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<td>ICL7660ACBA</td>
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<td>8 Ld SOIC (N)</td>
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<td>8 Ld SOIC (N) Tape and Reel</td>
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<td>8 Ld PDIP</td>
<td>E8.3</td>
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<td>ICL7660AIBA</td>
<td>-40 to 85</td>
<td>8 Ld SOIC (N)</td>
<td>M8.15</td>
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<td>ICL7660AIBA-T</td>
<td>-40 to 85</td>
<td>8 Ld SOIC (N) Tape and Reel</td>
<td>M8.15</td>
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<td>ICL7660AIPA</td>
<td>-40 to 85</td>
<td>8 Ld PDIP</td>
<td>E8.3</td>
</tr>
</tbody>
</table>

† Add /883B to part number if 883B processing is required.
**Absolute Maximum Ratings**

Supply Voltage
- ICL7660 ........................................... +10.5V
- ICL7660A .......................................... +13.0V

LV and OSC Input Voltage: 0.3V to (V+ + 0.3V) for V+ < 5.5V
(Note 2).......................... (V+-5.5V) to (V++0.3V) for V+ > 5.5V
Current into LV (Note 2).................. 20µA for V+ > 3.5V
Output Short Duration (V_{SUPPLY} ≤ 5.5V) ............ Continuous

**Operating Conditions**

Temperature Range
- ICL7660M ........................................... -55°C to 125°C
- ICL7660C, ICL7660AC .......................... 0°C to 70°C
- ICL7660AI ........................................... -40°C to 85°C

**Thermal Information**

Thermal Resistance (Typical, Note 1) \( \theta_{JA} \), \( \theta_{JC} \)
- PDIP Package ........................................ 150 N/A
- SOIC Package ......................................... 165 N/A
- Metal Can Package (ICL7660 Only) ............ 160 70

Maximum Storage Temperature Range ............. -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) ............ 300°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. \( \theta_{JA} \) is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**

ICL7660 and ICL7660A, \( V_+ = 5V, T_A = 25°C, C_{OSC} = 0 \), Test Circuit Figure 11

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL7660</th>
<th>ICL7660A</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>I+</td>
<td>( RL = \infty )</td>
<td>-</td>
<td>170</td>
<td>500</td>
</tr>
<tr>
<td>Supply Voltage Range - Lo</td>
<td>( V_{L+} )</td>
<td>( MIN &lt; T_A \leq MAX, RL = 10k\Omega, LV \rightarrow GND )</td>
<td>1.5</td>
<td>-</td>
<td>3.5</td>
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<tr>
<td>Supply Voltage Range - Hi</td>
<td>( V_{H+} )</td>
<td>( MIN &lt; T_A \leq MAX, RL = 10k\Omega, LV \rightarrow Open )</td>
<td>3.0</td>
<td>-</td>
<td>10.0</td>
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<tr>
<td>Output Source Resistance</td>
<td>( R_{OUT} )</td>
<td>( I_{OUT} = 20mA, T_A = 25°C )</td>
<td>-</td>
<td>55</td>
<td>100</td>
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<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 20mA, 0°C \leq T_A \leq 70°C )</td>
<td>-</td>
<td>-</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 20mA, -55°C \leq T_A \leq 125°C )</td>
<td>-</td>
<td>-</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{OUT} = 20mA, -40°C \leq T_A \leq 85°C )</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_+ = 2V, I_{OUT} = 3mA, LV \rightarrow GND, 0°C \leq T_A \leq 70°C )</td>
<td>-</td>
<td>-</td>
<td>300</td>
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<tr>
<td></td>
<td></td>
<td>( V_+ = 2V, I_{OUT} = 3mA, LV \rightarrow GND, -55°C \leq T_A \leq 125°C )</td>
<td>-</td>
<td>-</td>
<td>400</td>
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<tr>
<td>Oscillator Frequency</td>
<td>( f_{OSC} )</td>
<td></td>
<td></td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Power Efficiency</td>
<td>( P_{EF} )</td>
<td>( RL = 5k\Omega )</td>
<td>95</td>
<td>98</td>
<td>96</td>
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<tr>
<td>Voltage Conversion Efficiency</td>
<td>( V_{OUT} EF )</td>
<td>( RL = \infty )</td>
<td>97</td>
<td>99.9</td>
<td>99</td>
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<tr>
<td>Oscillator Impedance</td>
<td>( Z_{OSC} )</td>
<td>( V_+ = 2V )</td>
<td>-</td>
<td>1.0</td>
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<tr>
<td></td>
<td></td>
<td>( V_+ = 5V )</td>
<td>-</td>
<td>100</td>
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ICL7660A, \( V_+ = 3V, T_A = 25°C, OSC = \) Free running, Test Circuit Figure 11, Unless Otherwise Specified

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL7660A</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Supply Current (Note 3)</td>
<td>I+</td>
<td>( V_+ = 3V, RL = \infty, 25°C )</td>
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<tr>
<td></td>
<td></td>
<td>( 0°C &lt; T_A &lt; 70°C )</td>
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<td>-</td>
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<tr>
<td></td>
<td></td>
<td>( -40°C &lt; T_A &lt; 85°C )</td>
<td>-</td>
<td>-</td>
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<tr>
<td>Output Source Resistance</td>
<td>( R_{OUT} )</td>
<td>( V_+ = 3V, I_{OUT} = 10mA )</td>
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<td>-</td>
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<tr>
<td></td>
<td></td>
<td>( 0°C &lt; T_A &lt; 70°C )</td>
<td>-</td>
<td>-</td>
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<tr>
<td></td>
<td></td>
<td>( -40°C &lt; T_A &lt; 85°C )</td>
<td>-</td>
<td>-</td>
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<tr>
<td>Oscillator Frequency (Note 3)</td>
<td>( f_{OSC} )</td>
<td>( V_+ = 3V ) (same as 5V conditions)</td>
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<td></td>
<td></td>
<td>( 0°C &lt; T_A &lt; 70°C )</td>
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<tr>
<td></td>
<td></td>
<td>( -40°C &lt; T_A &lt; 85°C )</td>
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</table>
### Electrical Specifications

ICL7660 and ICL7660A, $V_+ = 5V$, $T_A = 25^\circ C$, $C_{OSC} = 0$, Test Circuit Figure 11

Unless Otherwise Specified (Continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL7660 MIN</th>
<th>ICL7660A MIN</th>
<th>ICL7660 MAX</th>
<th>ICL7660A MAX</th>
<th>UNITS</th>
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<tr>
<td>Voltage Conversion Efficiency</td>
<td>$V_{OUTE}$</td>
<td>$V_+ = 3V$, $R_L = \infty$</td>
<td>-</td>
<td>-</td>
<td>99</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{MIN} &lt; T_A &lt; T_{MAX}$</td>
<td>-</td>
<td>-</td>
<td>99</td>
<td>-</td>
<td>%</td>
</tr>
<tr>
<td>Power Efficiency</td>
<td>$P_{EFF}$</td>
<td>$V_+ = 3V$, $R_L = 5k\Omega$</td>
<td>-</td>
<td>-</td>
<td>96</td>
<td>-</td>
<td>%</td>
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<tr>
<td></td>
<td></td>
<td>$T_{MIN} &lt; T_A &lt; T_{MAX}$</td>
<td>-</td>
<td>-</td>
<td>95</td>
<td>-</td>
<td>%</td>
</tr>
</tbody>
</table>

NOTES:

2. Connecting any input terminal to voltages greater than $V_+$ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the ICL7660, ICL7660A.

3. Derate linearly above $50^\circ C$ by $5.5\text{mW/}^\circ C$.

4. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of $5pF$.

5. The Intersil ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

### Functional Block Diagram

![Functional Block Diagram](image)

### Typical Performance Curves

(Test Circuit of Figure 11)

- **Figure 1.** Operating Voltage as a Function of Temperature

- **Figure 2.** Output Source Resistance as a Function of Supply Voltage
Typical Performance Curves (Test Circuit of Figure 11) (Continued)

**FIGURE 3.** OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

**FIGURE 4.** POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY

**FIGURE 5.** FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

**FIGURE 6.** UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

**FIGURE 7.** OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

**FIGURE 8.** SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT
**Typical Performance Curves**  (Test Circuit of Figure 11)  (Continued)

![Figure 9. Output Voltage as a Function of Output Current](image1)

**Figure 9. Output Voltage as a Function of Output Current**

**Figure 10. Supply Current and Power Conversion Efficiency as a Function of Load Current**

**NOTE:**
6. These curves include in the supply current that current fed directly into the load $R_L$ from the $V_+$ (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660/ICL7660A, to the negative side of the load. Ideally, $V_{OUT} \approx 2V_{IN}$, $I_S \approx 2I_L$, so $V_{IN} \times I_S \approx V_{OUT} \times I_L$.

![Figure 11. ICL7660, ICL7660A Test Circuit](image2)

**Figure 11. ICL7660, ICL7660A Test Circuit**

**Detailed Description**

The ICL7660 and ICL7660A contain all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 12, which shows an idealized negative voltage converter. Capacitor $C_1$ is charged to a voltage, $V_+$, for the half cycle when switches $S_1$ and $S_3$ are closed. (Note: Switches $S_2$ and $S_4$ are open during this half cycle.) During the second half cycle of operation, switches $S_2$ and $S_4$ are closed, with $S_1$ and $S_3$ open, thereby shifting capacitor $C_1$ negatively by $V_+$ volts. Charge is then transferred from $C_1$ to $C_2$ such that the voltage on $C_2$ is exactly $V_+$, assuming ideal switches and no load on $C_2$. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660 and ICL7660A, the 4 switches of Figure 12 are MOS power switches; $S_1$ is a P-Channel device and $S_2$, $S_3$ and $S_4$ are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of $S_3$ and $S_4$ must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON” resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V_+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 and ICL7660A by a logic network which senses the output voltage ($V_{OUT}$) together with the level translators, and switches the substrates of $S_3$ and $S_4$ to the correct level to maintain necessary reverse bias.
The voltage regulator portion of the ICL7660 and ICL7660A is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the “LV” pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

**Theoretical Power Efficiency Considerations**

In theory a voltage converter can approach 100% efficiency if certain conditions are met.

1. The driver circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 and ICL7660A approach these conditions for negative voltage conversion if large values of C1 and C2 are used.

**Do’s And Don’ts**

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C1 must be connected to pin 2 of the ICL7660 and ICL7660A and the + terminal of C2 must be connected to GROUND.
5. If the voltage supply driving the ICL7660 and ICL7660A has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

**ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

\[ E = \frac{1}{2} C_1 (V_1^2 - V_2^2) \]

where \( V_1 \) and \( V_2 \) are the voltages on \( C_1 \) during the pump and transfer cycles. If the impedances of \( C_1 \) and \( C_2 \) are relatively high at the pump frequency (refer to Figure 12) compared to the value of \( R_L \), there will be a substantial difference in the voltages \( V_1 \) and \( V_2 \). Therefore it is not only desirable to make \( C_2 \) as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for \( C_1 \) in order to achieve maximum efficiency of operation.
Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 and ICL7660A for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 13A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 13B. The voltage source has a value of -V+. The output impedance (RO) is a function of the ON resistance of the internal MOS switches (shown in Figure 12), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for RO is:

\[
RO \cong \frac{2(R_{SW1} + R_{SW3} + ESR_{C1})}{f_{PUMP} (C1)} + ESR_{C2}
\]

\[
1 + \frac{1}{f_{OSC}} \cdot \frac{1}{R_{SWX}} = MOSFET \text{ switch resistance}
\]

Combining the four R_{SWX} terms as R_{SW}, we see that:

\[
RO \cong 2(R_{SW}) + \frac{1}{f_{PUMP} (C1)} + 4(ESR_{C1}) + ESR_{C2}
\]

RSW, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at 25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the 1/(f_{PUMP} \cdot C1) component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the 1/(f_{PUMP} \cdot C1) term, but may have the side effect of a net increase in output impedance when C1 > 10μF and there is no longer enough time to fully charge the capacitors.
every cycle. In a typical application where \( f_{\text{OSC}} = 10\text{kHz} \) and 
\( C = C_1 = C_2 = 10\mu\text{F} \):

\[
R_O \approx \frac{2}{(23)} + \frac{1}{(5 \times 10^3)(10^{-5})} + 4(\text{ESR}_{C1}) + \text{ESR}_{C2}
\]

\[
R_O \approx 46 + 20 + 5(\text{ESR}_{C})
\]

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low \( 1/(f_{\text{PUMP}} \cdot C_1) \) term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as \( 10\Omega \).

\[
R_O / \approx \frac{2}{(23)} + \frac{1}{(5 \times 10^3)(10^{-5})} + 4(\text{ESR}_{C1}) + \text{ESR}_{C2}
\]

\[
R_O \approx 46 + 20 + 5(\text{ESR}_{C})
\]

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**Output Ripple**

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 14. Segment A is the voltage drop across the ESR of \( C_2 \) at the instant it goes from being charged by \( C_1 \) (current flow into \( C_2 \)) to being discharged through the load (current flowing out of \( C_2 \)). The magnitude of this current change is \( 2 \times I_{\text{OUT}} \), hence the total drop is \( 2 \times I_{\text{OUT}} \times \text{ESR}_{C2}V \). Segment B is the voltage change across \( C_2 \) during time \( t_2 \), the half of the cycle when \( C_2 \) supplies current to the load. The drop at B is \( I_{\text{OUT}} \times t_2/C_{2}V \). The peak-to-peak ripple voltage is the sum of these voltage drops:

\[
\text{VRIPPLE} = \left[ \frac{1}{2(\text{ESR}_{C2})} + 2 \times \text{ESR}_{C2} \right] I_{\text{OUT}}
\]

Again, a low ESR capacitor will reset in a higher performance output.

**Paralleling Devices**

Any number of ICL7660 and ICL7660A voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, \( C_2 \), serves all devices while each device requires its own pump capacitor, \( C_1 \). The resultant output resistance would be approximately:

\[
\text{ROUT} = \frac{\text{ROUT (of ICL7660/ICL7660A)}}{n \,(\text{number of devices})}
\]

**Cascading Devices**

The ICL7660 and ICL7660A may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

\[
V_{\text{OUT}} = -n \, (V_{\text{IN}})
\]

where \( n \) is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 and ICL7660A \( R_{\text{OUT}} \) values.

**Changing the ICL7660/ICL7660A Oscillator Frequency**

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 17. In order to prevent possible device latchup, a \( 1k\Omega \) resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a \( 10k\Omega \) pullup resistor to \( V^+ \) supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be \( 1/2 \) of the clock frequency. Output transitions occur on the positive-going edge of the clock.

![FIGURE 17. EXTERNAL CLOCKING](image-url)

It is also possible to increase the conversion efficiency of the ICL7660 and ICL7660A at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 18. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (\( C_1 \)) and reservoir (\( C_2 \)) capacitors; this is overcome by increasing the values of \( C_1 \) and \( C_2 \) by the same factor that the frequency has been reduced. For example, the addition of a \( 100pF \) capacitor between pin 7 (OSC) and \( V^+ \) will lower the oscillator frequency to \( 1kHz \) from its nominal frequency of \( 10kHz \) (a multiple of 10), and thereby necessitate a corresponding increase in the value of \( C_1 \) and \( C_2 \) (from \( 10\mu\text{F} \) to \( 100\mu\text{F} \)).
Positive Voltage Doubling

The ICL7660 and ICL7660A may be employed to achieve positive voltage doubling using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 and ICL7660A are used to charge $C_1$ to a voltage level of $V_+ - V_F$ (where $V_+$ is the supply voltage and $V_F$ is the forward voltage drop of diode $D_1$). On the transfer cycle, the voltage on $C_1$ plus the supply voltage ($V_+$) is applied through diode $D_2$ to capacitor $C_2$. The voltage thus created on $C_2$ becomes $(2V_+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes $D_1$ and $D_2$.

The source impedance of the output ($V_{OUT}$) will depend on the output current, but for $V_+ = 5V$ and an output current of 10mA it will be approximately $60\, \Omega$.

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 21. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 16, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 and ICL7660A can be a problem, particularly if the load current varies substantially. The circuit of Figure 22 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660s and ICL7660As output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660 and ICL7660A, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.
Other Applications
Further information on the operation and use of the ICL7660 and ICL7660A may be found in AN051 “Principals and Applications of the ICL7660 and ICL7660A CMOS Voltage Converter”. 

FIGURE 22. REGULATING THE OUTPUT VOLTAGE

FIGURE 23. RS232 LEVELS FROM A SINGLE 5V SUPPLY

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