Large scale electromagnetic and electrostatic simulations

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Agere Systems

Simulation of devices and interconnect

- Modeling of passive structures
- Interconnect (wires on a chip)
  - High frequencies cause severe coupling, glitches, crosstalk, delay, etc.
- Components (for RF/Optical circuits)
  - Inductors, filters need accurate modeling
- Models used in higher level simulators
  - Spice, HB, delay calculators, Reduced order modeling tools

The physics

- The problems are well described by Maxwell's equations
- Low-frequency Helmholtz or Laplace's equation in layered dielectric media

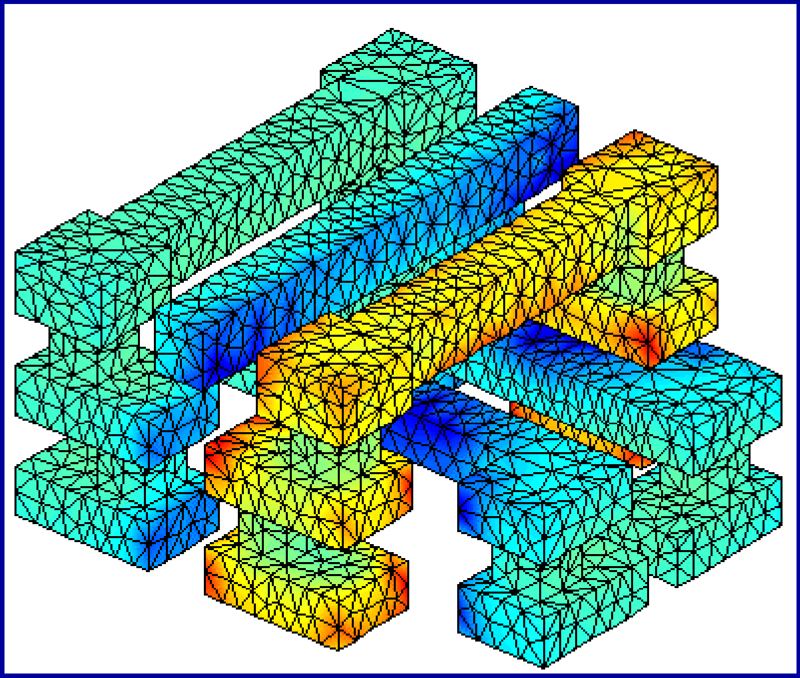
$$\nabla^2(\phi) = 0 \qquad\qquad (\nabla^2 + k^2)\phi = 0$$

- Traditionally two approaches to solving these problems
  - Finite element/Finite Difference methods
  - Integral-equation or boundary element methods

Integral equation solutions

- The fundamental advantage of integral approaches over finite-element methods is that they exploit the known analytic solutions of Maxwell's equations
- Instead of discretizing the operator as in FE methods, the solution is composed of a linear combination of solutions that satisfy the underlying PDE.
- It is sufficient to discretize boundaries between materials as opposed to all of space
- Very well conditioned linear systems amenable to iterative techniques

Capacitance formulation



- The potential is computed by adding the influence of each surface charge

$$\phi(r) = \int_{R'} G(r, r')\sigma(r')dr'$$

- In discretized form, we get a matrix equation

$$G(r, r') = \frac{1}{4\pi\varepsilon\|r - r'\|}$$

$$A\sigma = \varphi$$

Why integral equations? cont.

- Integral methods lead to a dense system of linear equations, as compared to sparse systems that arise from finite element approaches
- Because of the $O(n^3)$ cost of computing and solving the system, integral equations were largely abandoned
- Modern numerical methods reduce the cost to $O(n)$

1. Iterative techniques for solving linear systems
2. Fast matrix-vector products for the sorts of matrices that arise from integral equations

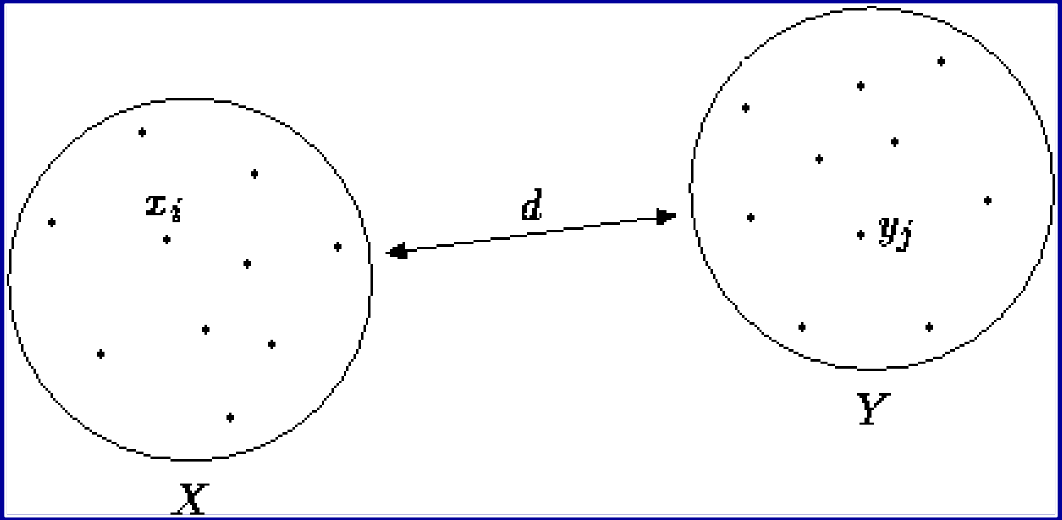
Fast Matrix-vector products

- Black box approaches
  - Methods based on the FFT
  - Methods base on low-rank decompositions (SVDs)
- Kernel based approaches
  - Fast-multipole and fast-multipole like methods

- Both the Fast Multipole methods and the SVD based methods are based on efficient approximation of potential kernels of the form 1/r

Low-rank nature of matrices

- Key observation: With well-separated points interaction matrix is numerically low rank.



$$G(r, r') = \frac{1}{4\pi\varepsilon\|r - r'\|}$$

SVD compression

- For an $N\ x\ N$ matrix A of rank r the SVD is used to factor

$$\begin{pmatrix} \\ \\ & A & \\ \\ \\ \end{pmatrix} = \begin{pmatrix} \\ \\ U \\ \\ \\ \end{pmatrix} \begin{pmatrix} & V & \end{pmatrix}$$

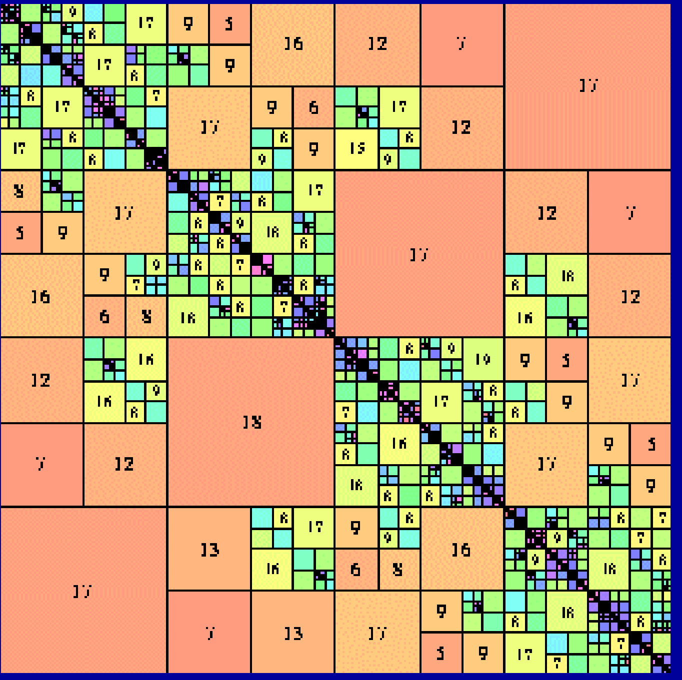
  where U and V are N *by* r matrices
- Matrix vector product
  - Directly: requires $O(N^2)$ operations
  - Using the UV representation requires $2\ r\ N$ operations
- *When $r << N$ this is far more efficient*
- FMM based on similar factorization with efficient multipole representation

IES³

- IES^3 is a method for matrix compression based on the singular value decomposition
- Order points, and recursively subdivide space into well-separated regions
- Primarily used to solve time-harmonic Maxwell

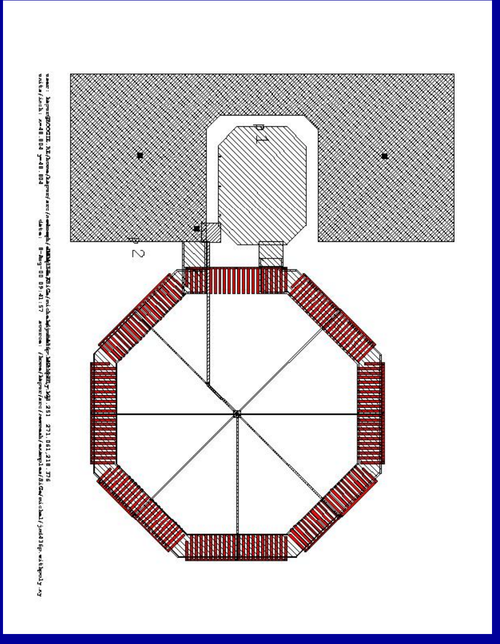
$$B(\omega) = \Omega + j\omega A + \frac{\Phi}{j\omega}$$

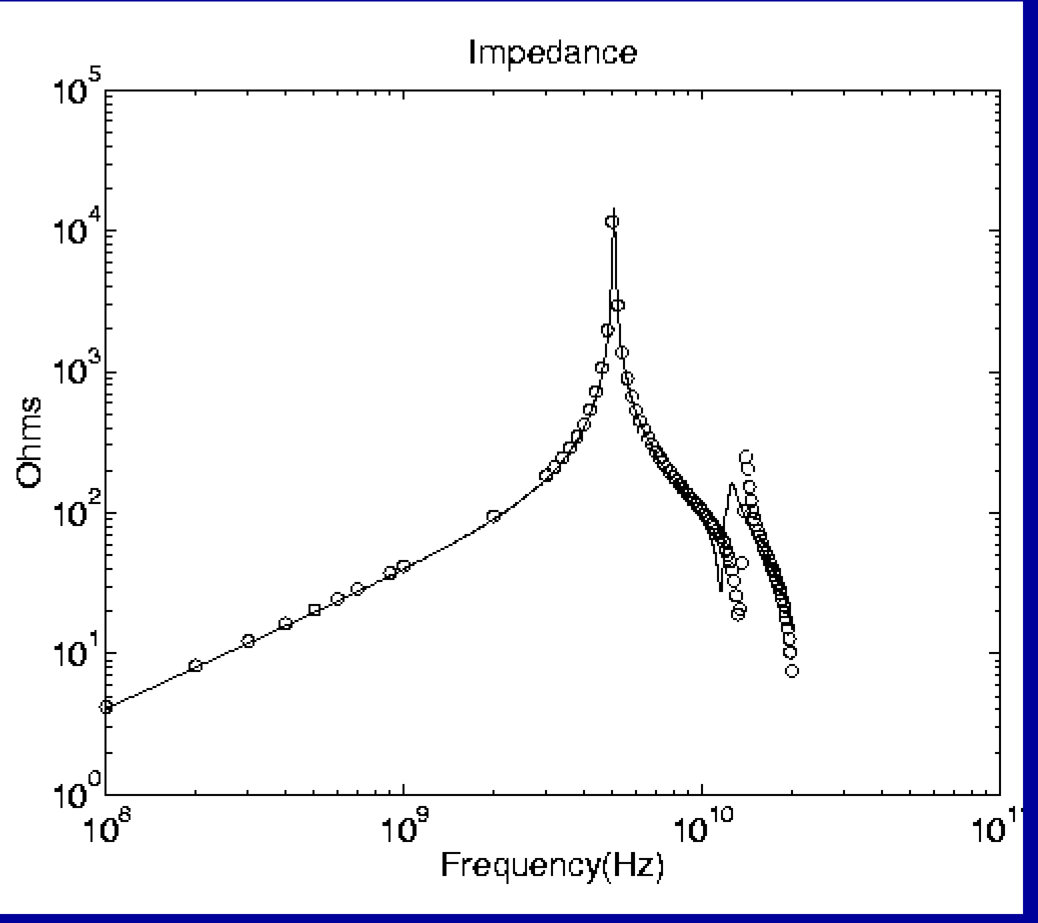
- Has been successfully used for a few years both internally and commercially for component level simulation



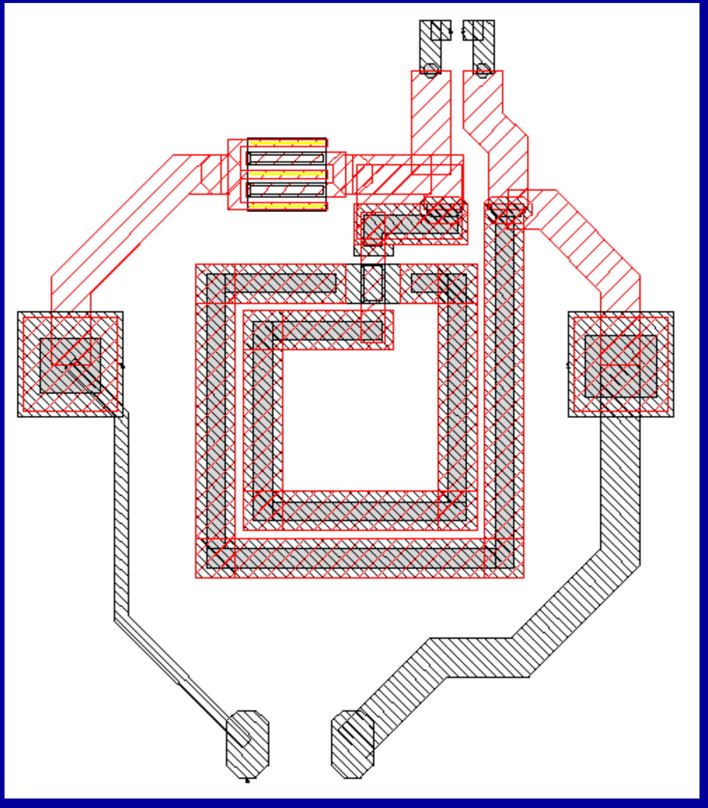
Excellent predictive capabilities

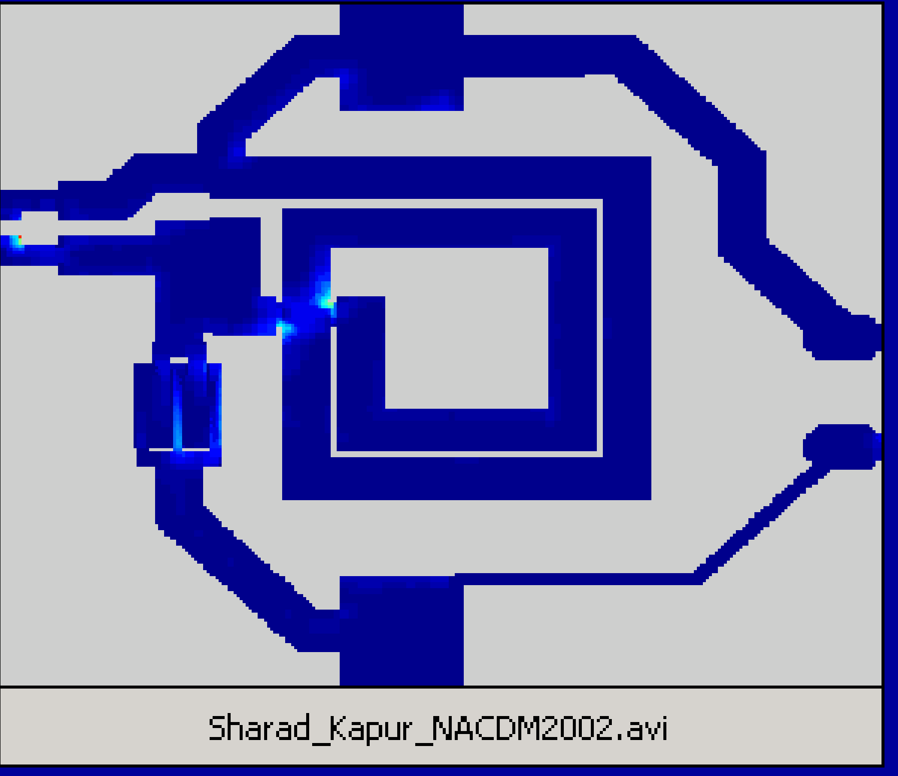
- Inductor design





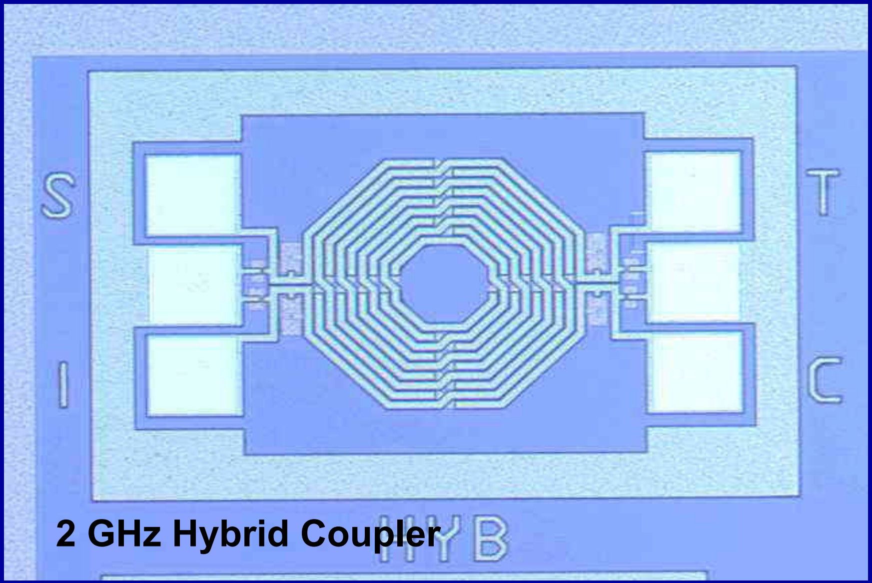
Entire VCOs



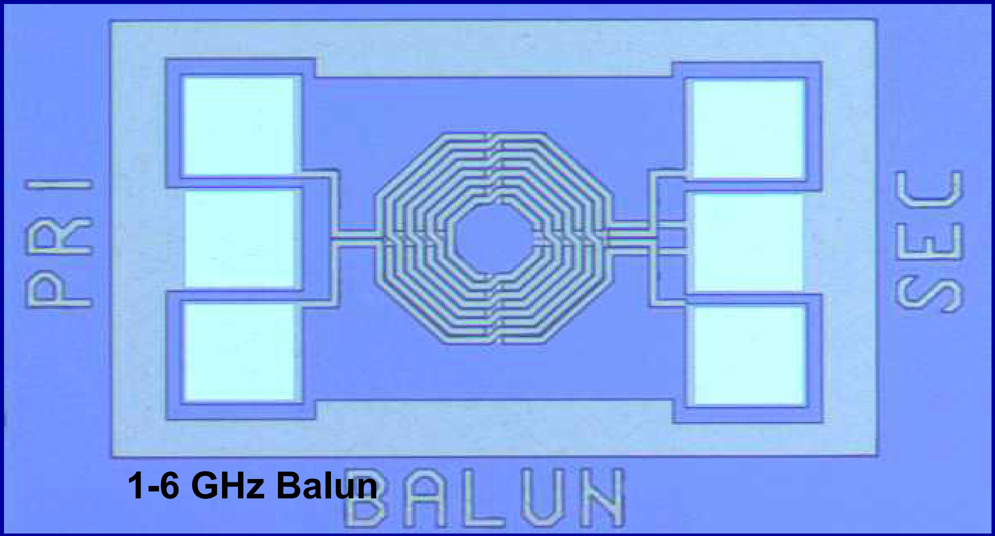


Baluns and Hybrids (with R.Frye and R.Melville)

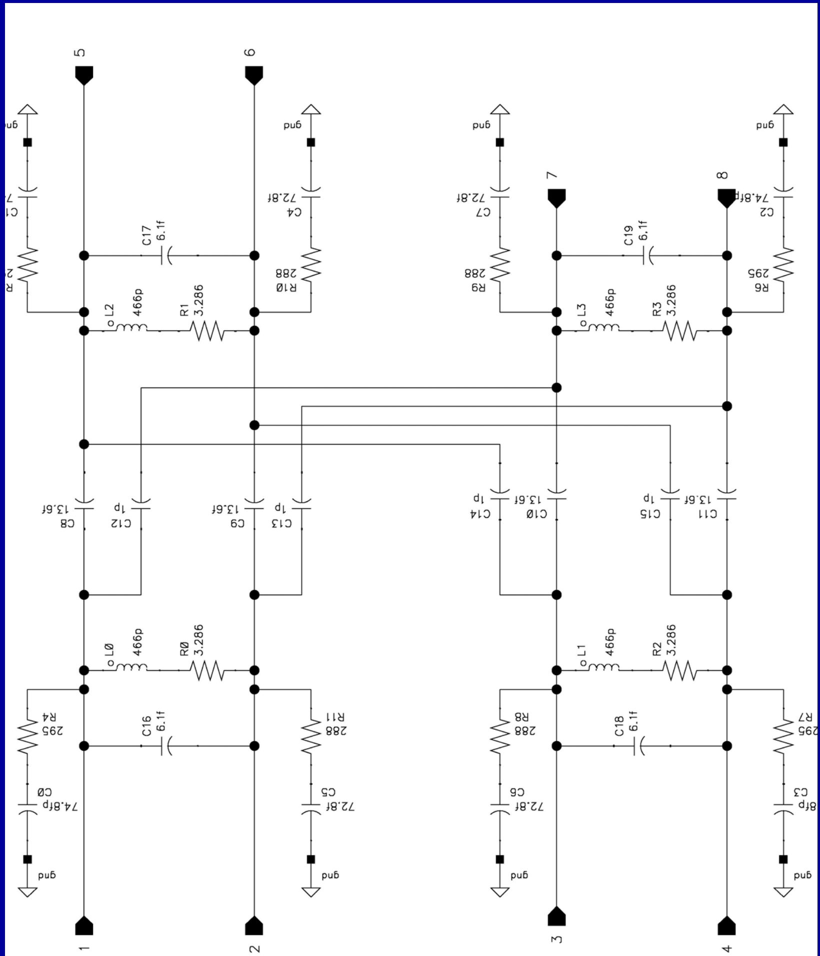
Use inductive coupling to change phase
Replace off-chip components or non-linear elements
for wireless circuits



2 GHz Hybrid Coupler

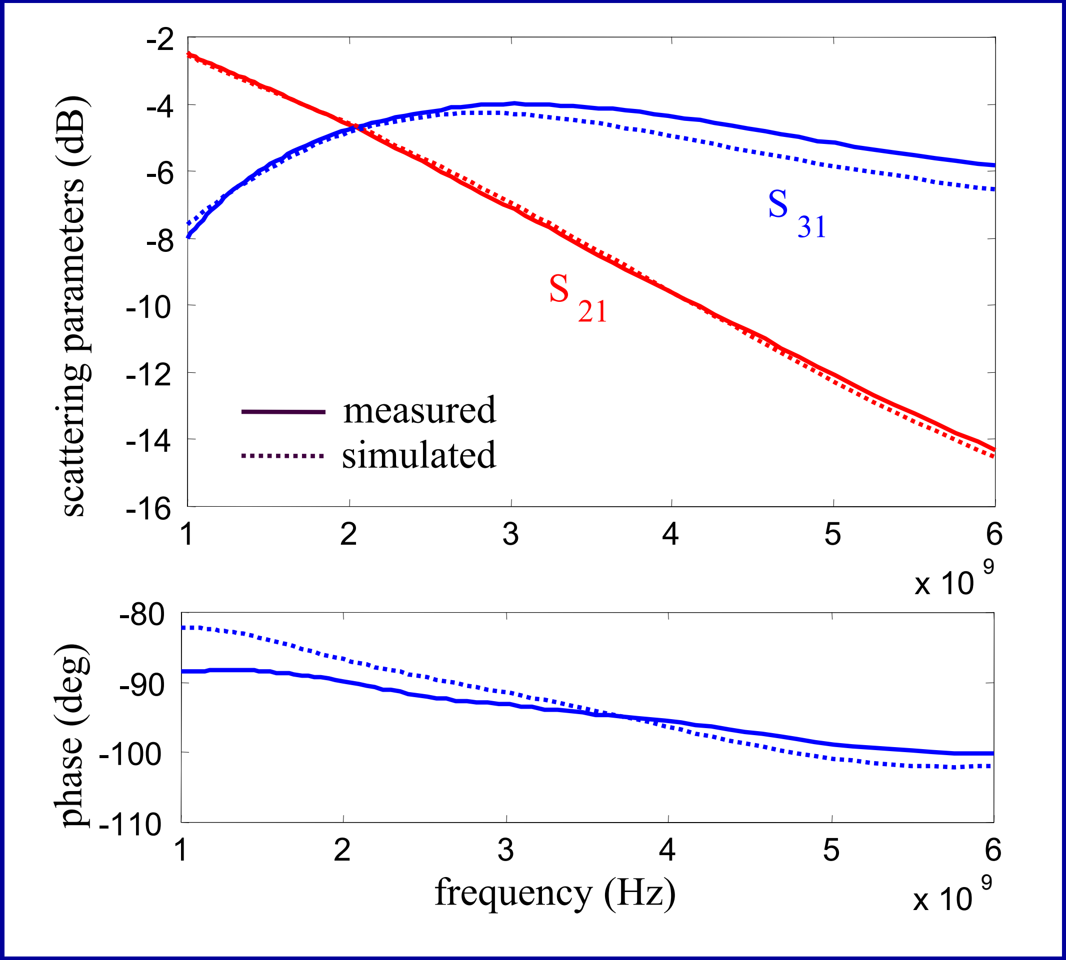


1-6 GHz Balun

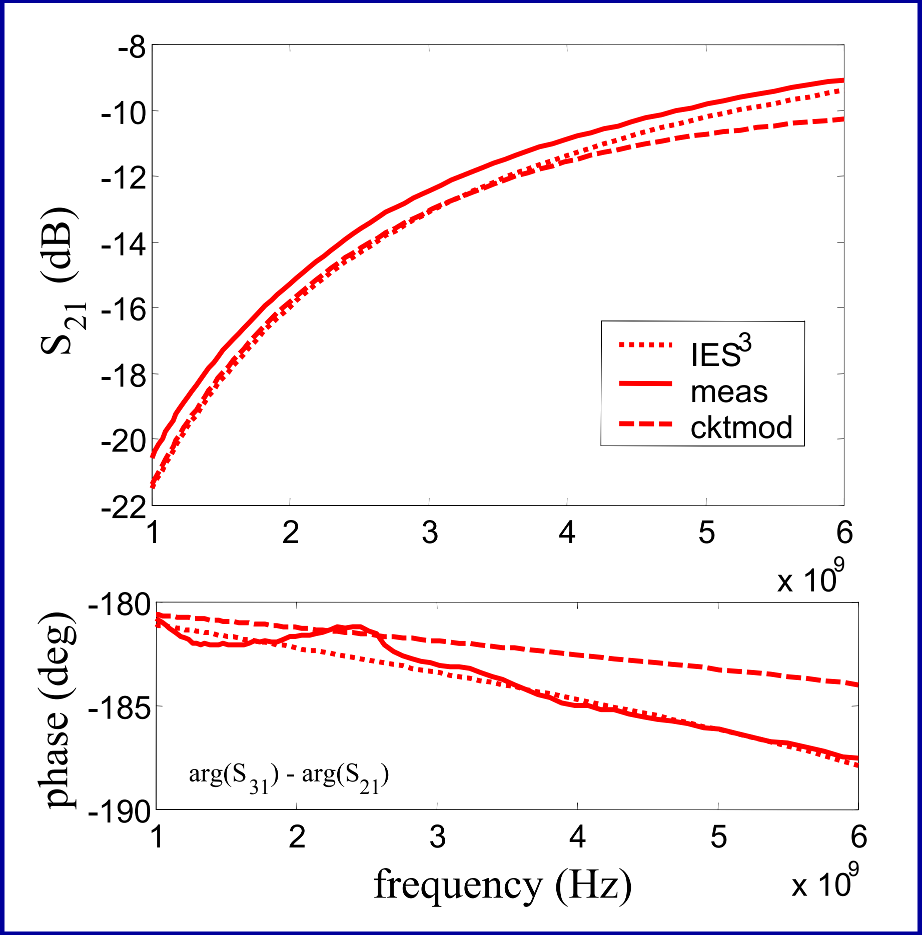


Simulation vs coupler measurements

Hybrid



Balun



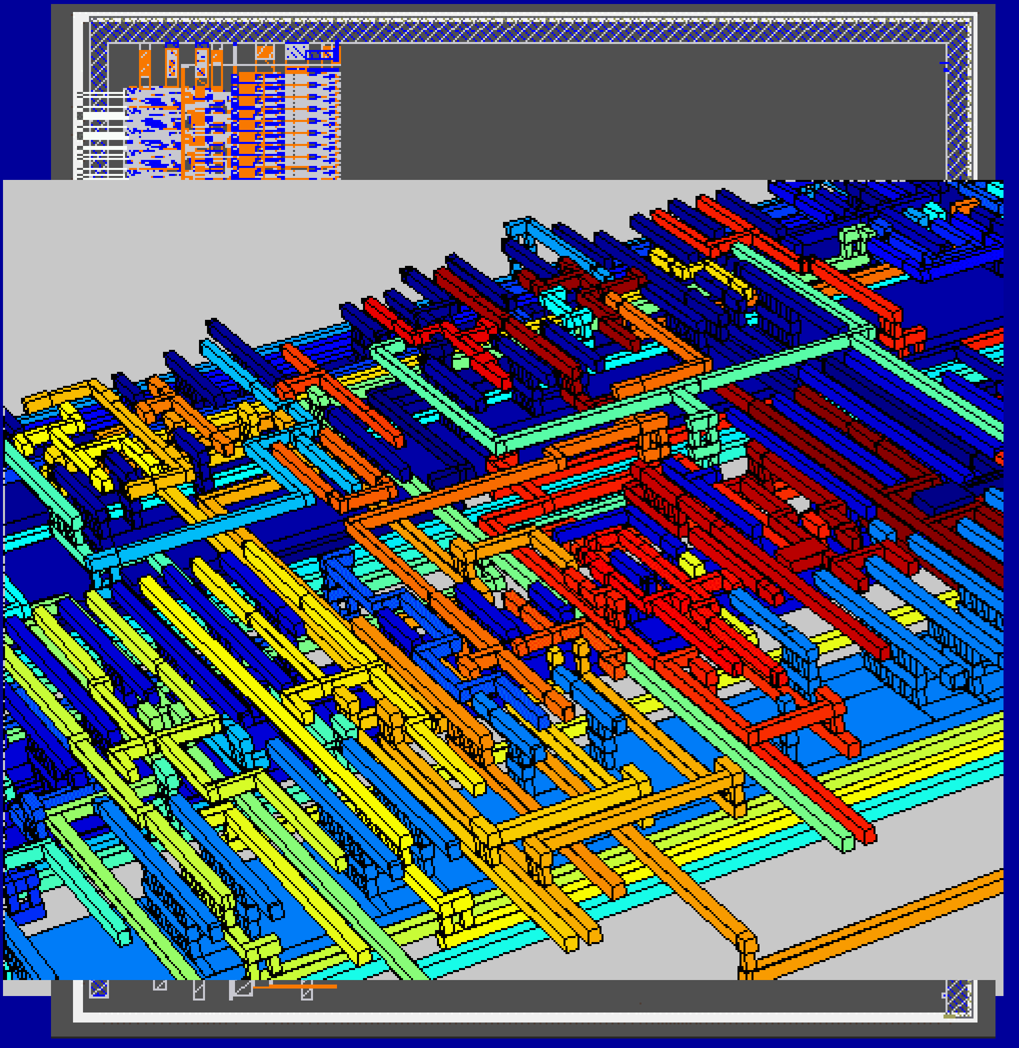
Not good enough

- IES^3 can tackle relatively tiny problems.
- Needed some significant improvement
- Could handle problems from 10^5 to 10^6 unknowns with standard discretizations
- New approach:

1. Change the discretization strategy
2. Change to a version of the Fast Multipole method specialized to IC geometries
3. Approximate geometry

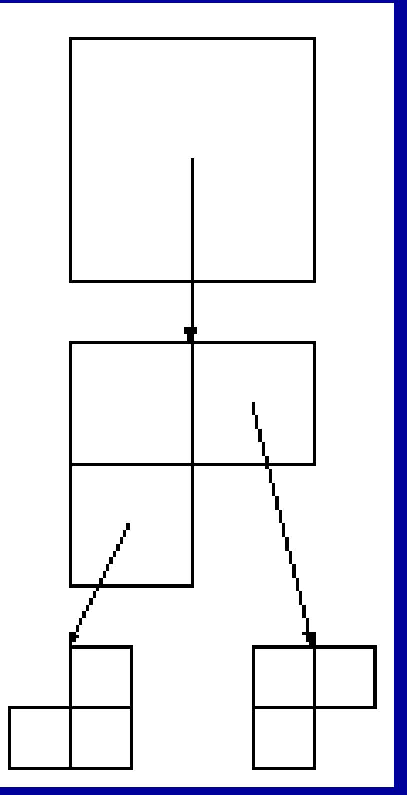
Nebula

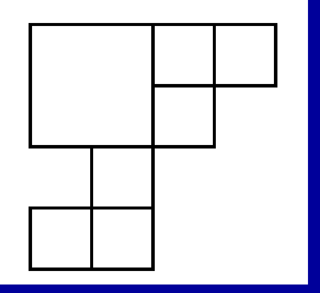
- IES^3 is typically used for single a small ensemble of components. Inadequate for large structures
- Chip level capacitance calculation
- The scale of the geometric description is overwhelming
- *Billions* of geometric features



Use a variant of the fast Multipole method

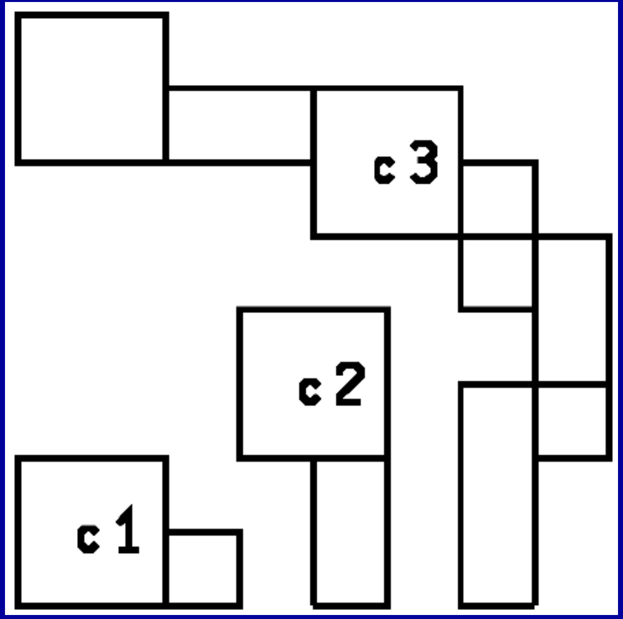
- Subdivide space in an octtree
- Interactions between all leaves
- Close interactions done directly
- Far interactions are done via a legendre expansions (multipole expansion) of the Green's function
- Precompute all interaction matrices with a given Green's function
- 10x-50x faster than IES^3



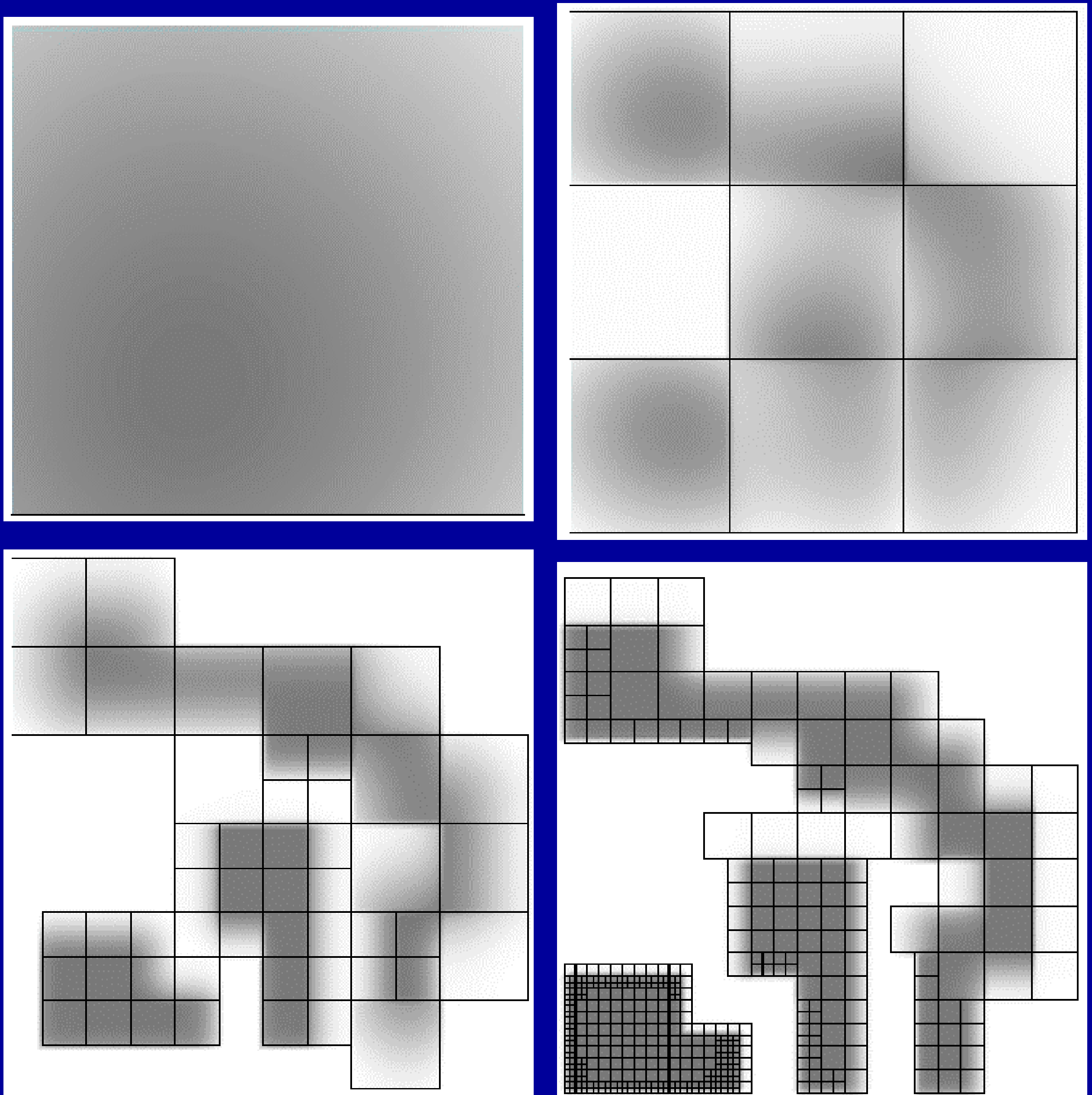


Coarse representation of geometry

Approximate characteristic
function of
geometry with moments



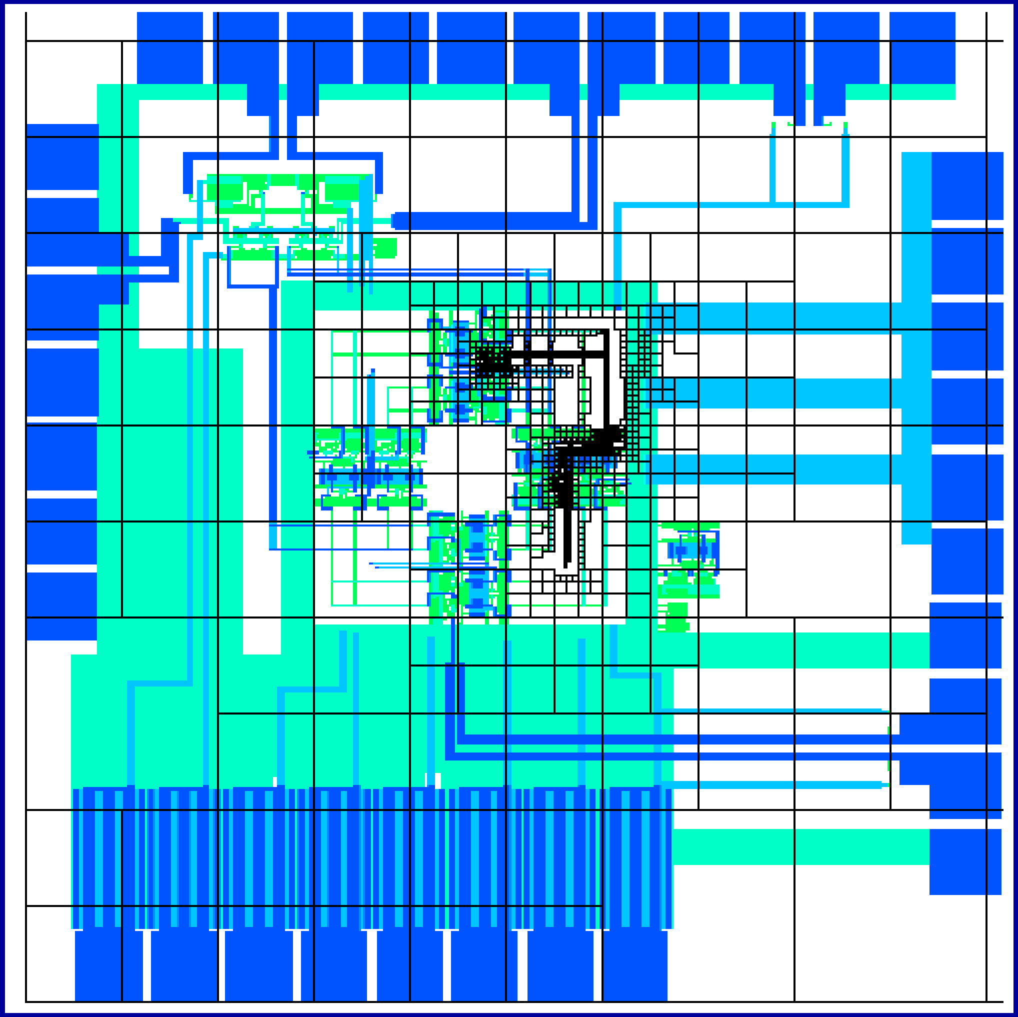
Only a few numbers are
needed to capture the far
field interactions



RF Chips

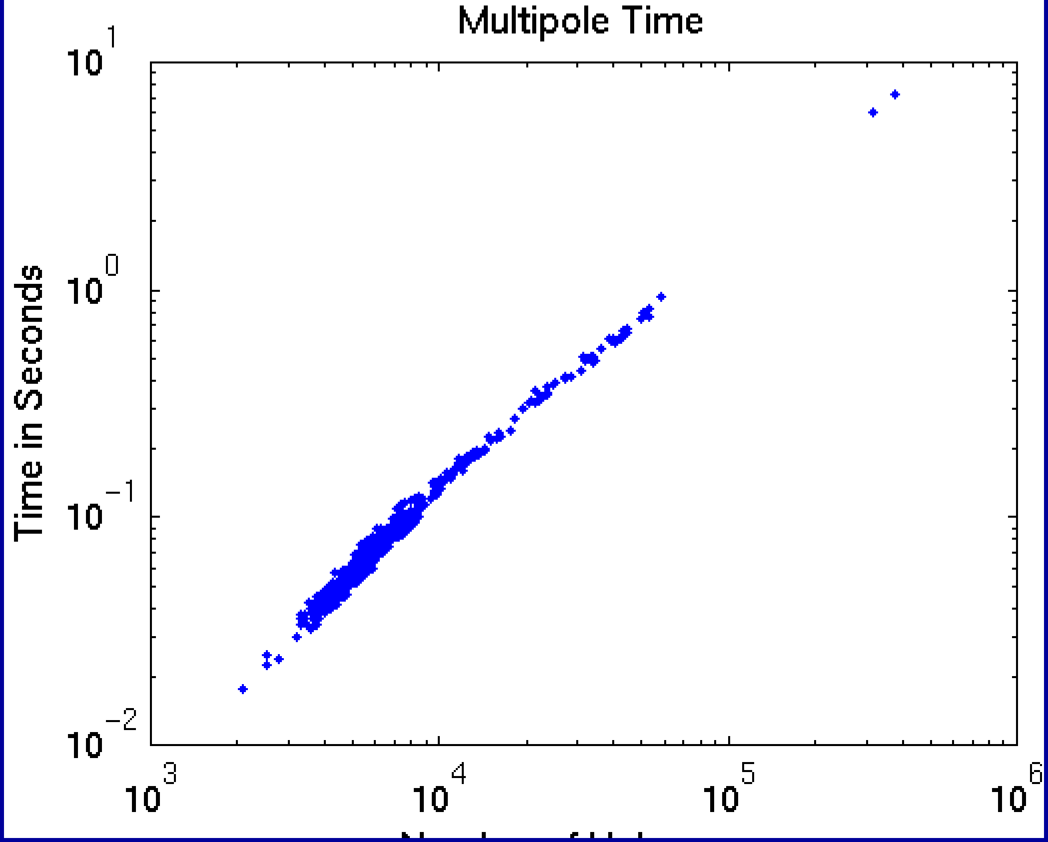
- 1.3mm on a side
- 92,000 rectangles
- Boxes show typical discretization for an individual net using Nebula
- Far away boxes have hundreds of conductors

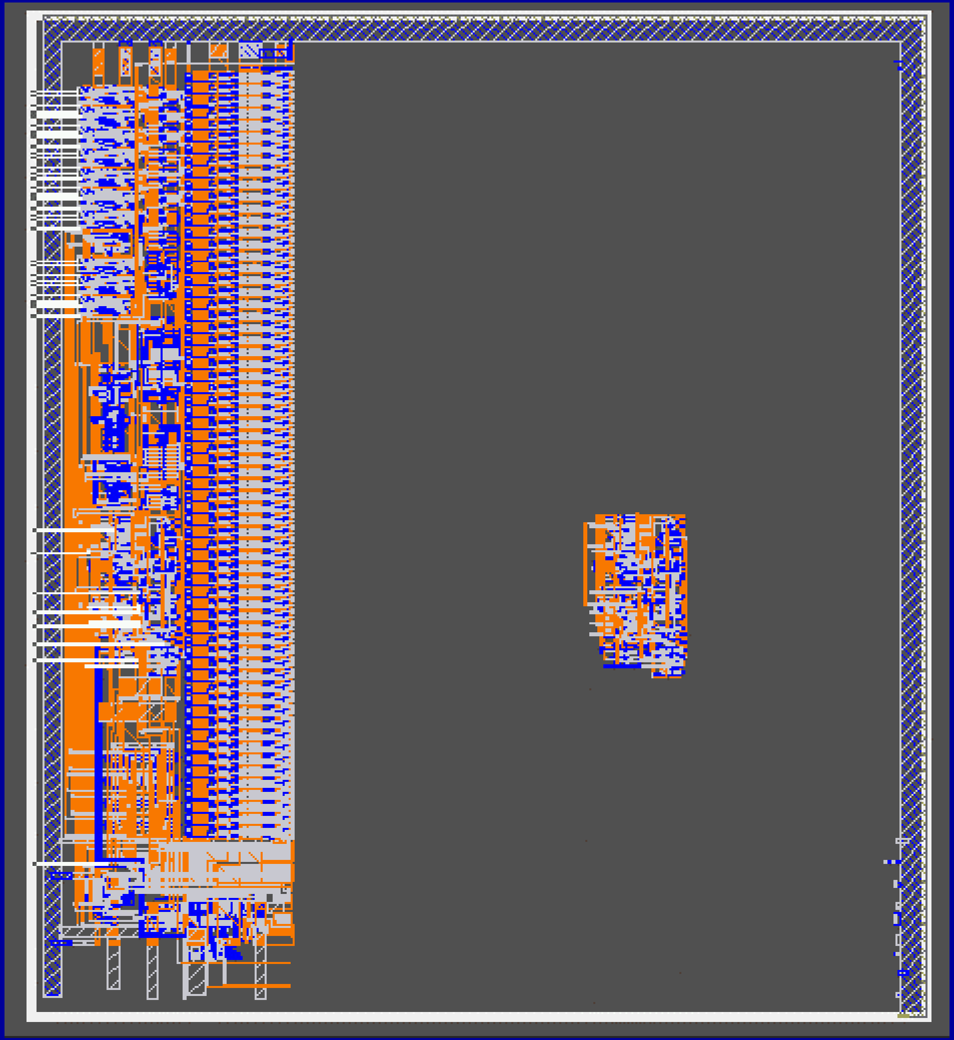
	Time
QC 5%	3min
QC 2%	8min
QC 1%	20min
QC 0.5%	72min
Nebula	10min



Section of digital chip

- *258,000 rectangles, 838 nets*
  0.5mm on a side





Efficiency issues

- Even with all advances field solving approach is very slow compared to pattern matching approaches
- Always trying to come up with better discretizations
- Adaptive refinement is too conservative and slow
- Many heuristics, basically guessing form of the solution put into mesh generation

What constitutes a good answer?

- 1% accuracy compared to measurement is considered excellent
- Simulation accuracies are usually set to 1%
- How does this make sense if process variation can be up to 20%?
- Often in circuit design the absolute number does not matter but a relative number is more important
- Differential design and symmetry can further isolate errors due to process variations

New directions

- Modeling for optical circuits
  - In the future there will be a need for optical circuit simulators
  - Lasers take the role of transistors
  - Waveguides/Filters take the role of passives (RLC)
- Accelerating Nebula using FPGAs

Optical structure modeling

- Integrated optics will require accurate modeling of optical structures (e.g., waveguides, filters, etc.)
- In the future when dielectric differences become large it will be possible to construct sophisticated passive optical components on a chip
- Methods such as beam propagation and FDTD will not work in such an environment
- Preliminary research into making such a tool

Integral formulation

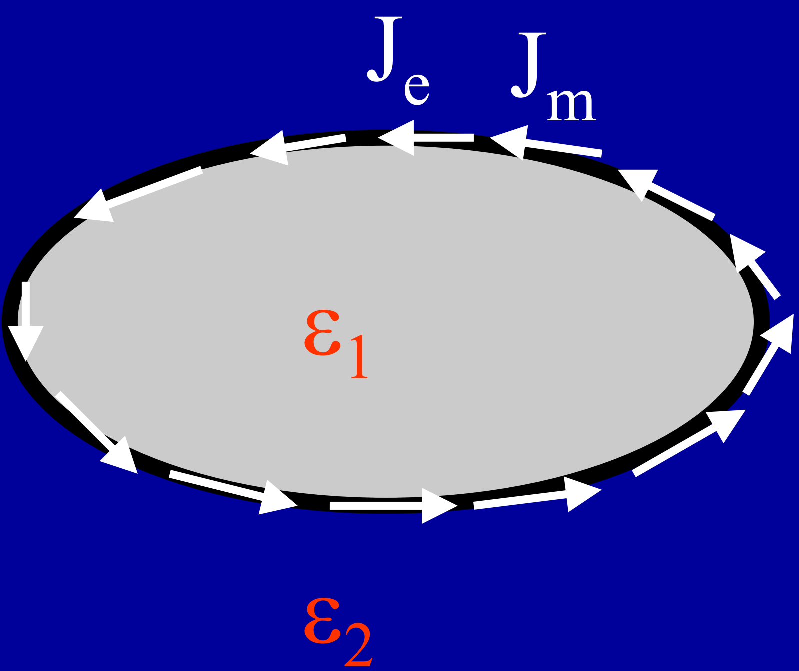
- Representation in terms of Electric and Magnetic currents at interfaces

$$E = \frac{1}{4\pi}\int_F (j\omega\mu J_e\phi + W_0 J_m \times \nabla'\phi - \frac{\rho_\varepsilon}{\varepsilon}\nabla'\phi)dF'$$

$$H = \frac{1}{4\pi}\int_F (j\omega W_0 J_m\phi + J_e \times \nabla'\phi - \frac{\rho_m}{\mu}\nabla'\phi)dF'$$

$$\beta = \sqrt{k^2 - k_c^2}$$

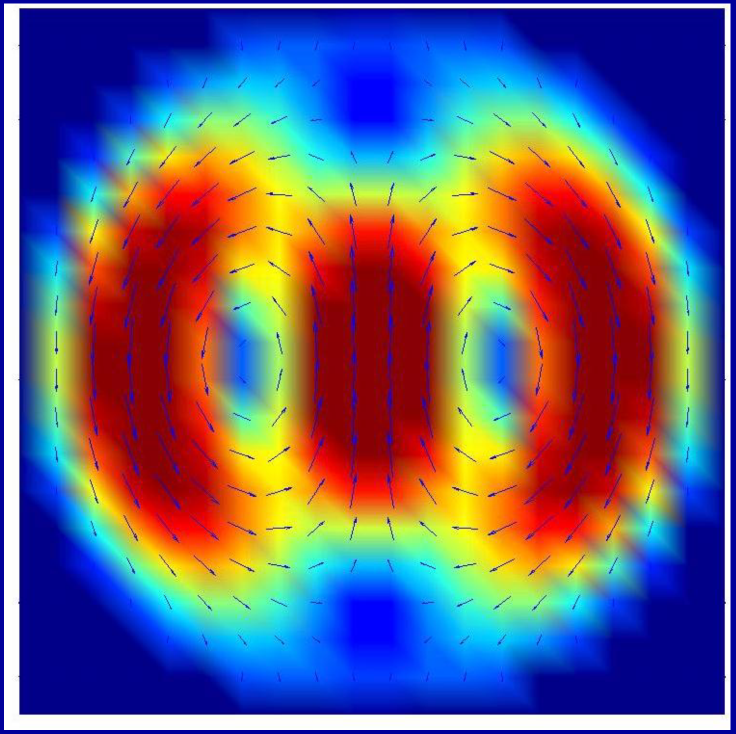
- Construct an integral-equation operator describing interactions between currents

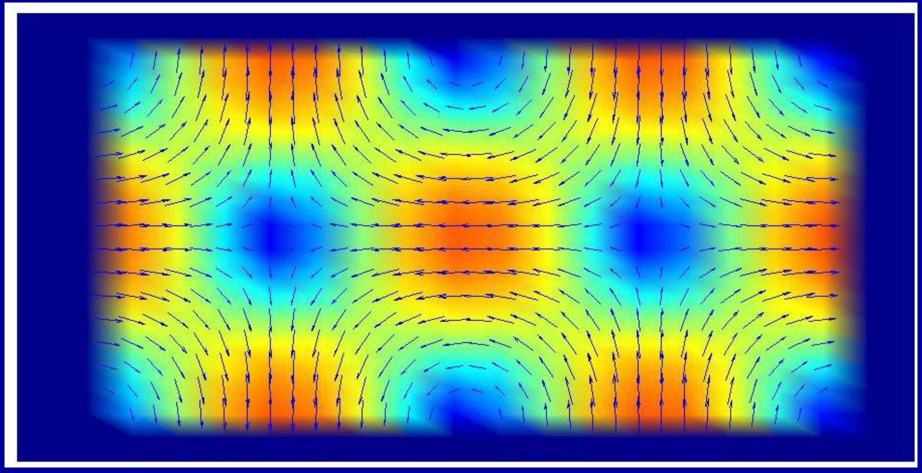


$$A(k_c) = 0$$

Currently…

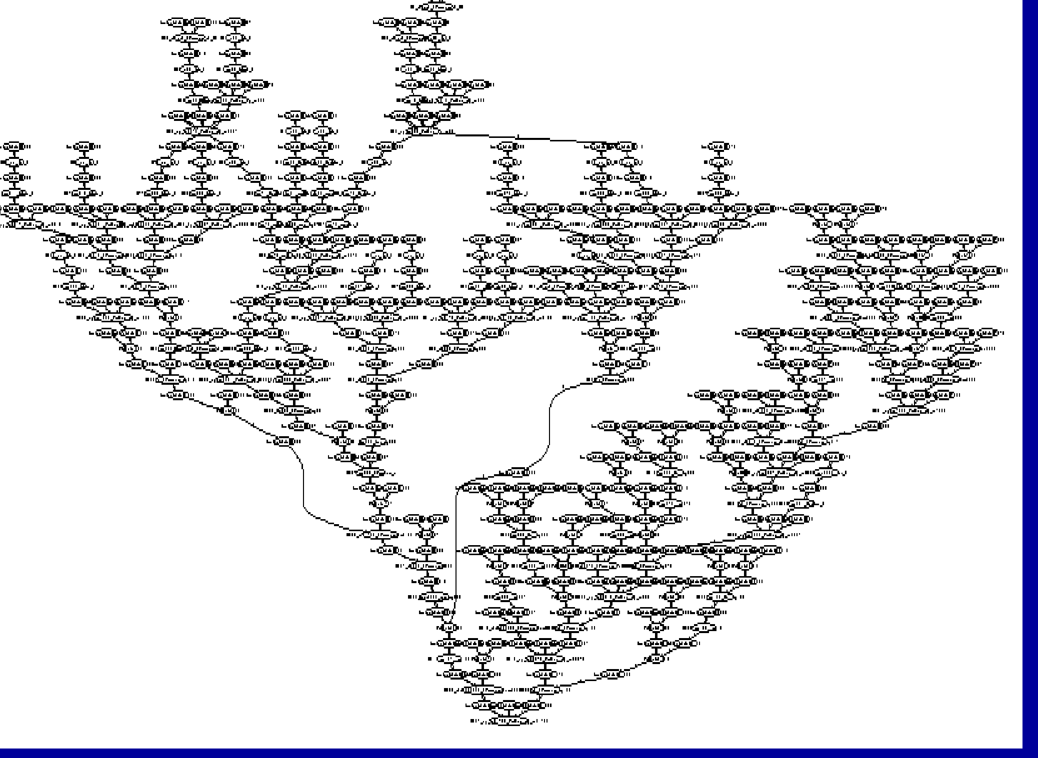
- Setting up the infrastructure…
  - Formulation, numerical discretization, eigensolution method
- Works surprisingly well for solving for eigenmodes of a metallic and dielectric waveguides
- Integrated with both IES^3 and a high frequency FMM





Accelerating Nebula with FPGAs

- Oskar Mencer (Bell Labs)
- Has a methodology for accelerating floating point computations using FPGAs
- A bottleneck in Nebula is the computation of certain double integrals (50% of the time is currently spent doing this)
- The double integral is mapped to an FPGA and run on a PCI board
- Potential 100x speedup over software



Conclusion

- Integral equation methods coupled with iterative methods and Fast Matrix vector products have been successful in modeling interconnect and devices
- Orders of magnitude faster than traditional BEM methods and FE/FD methods
- Acceleration schemes for chip level calculations
  - Specialized FMM methods
  - Complex conductor geometries hierarchically summarized by few numbers

People we work(ed) with

- Designers: P. Kinget, H. Wang, R. Frye, R.Melville
- Measurement: P. Smith, M. Frie, S. Moinian
- ALC: K. Singhal, J. Finnerty R.Gupta
- Cadence: C-Lo, S. Nahar
- Ansoft: R. Hall, D. Zheng
- Summer students: J. Zhao, F. Ling
- External: L. Greengard, V. Rokhlin (Yale)
- Friendly competition: (MIT) J. White, J. Phillips, K. Nabors, etc.