Project:
- Automatic Mixed-Signal Circuit Layout Optimization and Regeneration

Goal:
12/6/02 - Be able to run Extraction, Optimization, Regeneration, and Inductor part of one analog layout example (Adam's VCO). Finish a paper for DAC.

Weekly Progress:
- Active area (drain/source) resizing code is done.
- Start coding on transistor possible width/length range finder, in order to input into the synthesis tool.

Next Week Plan:
- Get the synthesis tool, so we can understand the input/output interface.
- Finish coding on possible transistor range, so Sam and I can print the correct output to the synthesis tool.
- Poly resizing (based on width and length).
- Interfacing code of synthesis output to resizing part.