Minutes of meeting held at the University of Washington (EE/CS Building, Room 206) on Thursday, 26 September 2002 at 1:00 pm

Present

From Boeing:

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GARY NELSON started by stating that to his knowledge UW develops CoSMoS tool, which would compete with Cadence tools and be able to do analog/ RF/parasitics. Each of UW Mixed-signal CAD lab researchers is responsible for a part of it.

SCOTT DAVIS asked whether CoSMoS would be a comprehensive tool that would make end-to end IC design possible without touching Cadence and would be enough to open a design house.

SAMBUDDHA BHATTACHARYA answered that this is not quite the case. UW focuses on simulation, especially on its areas that have not received enough attention in industry, such as behavioral level simulation with SPICE accuracy. Tasks such as layout, synthesis, or RF modeling are currently not included into CoSMoS.

RODNEY BONEBRIGHT asked to define RF frequencies.

PAVEL NIKITIN said that RF includes 300 KHz to 30 GHz. Wireless frequencies of common interest are 2.4 GHz and 5.8 GHz.

RICHARD SHI added that extremely high frequencies include the region up to 300 GHz. Another UW researcher, Vikram Jandhyala, is working in this area.

GARY NELSON reminded that the most important part of this meeting is to discuss what will be submitted to DARPA on 30 September, 2002.

RICHARD SHI demonstrated slides from the summer CoSMoS review that took place in August 2002, Providence, RI and mentioned that the material submitted to DARPA will be based on the abbreviated and perhaps enhanced version of the slides presented.

He said that the project goal is to develop modeling and simulation capabilities for giga-scale mixed-signal systems (develop the language as well as compilation/simulation capabilities); develop advanced EM solving capabilities; and, finally, demonstrate & validate modeling and simulation capabilities in DoD EDA design.

He mentioned that the scope of CoSMoS covers both digital (Verilog/VHDL), analog (Verilog/AMS, VHDL/AMS) and RF designs, combined in one simulator. He said that a lot of progress has been made since the project inception last year. Students can run CosMoS and Cadence tools concurrently, which allows comparison of the results.

SCOTT BILLINGS inquired whether VHDL-AMS being developed by the team is compatible with the standard VHDL?

RICHARD SHI said that VHDL-AMS could be used together with the standard VHDL. He also said that time domain simulation in CoSMoS is similar to Cadence AMS designer. The frequency domain simulation in CoSMoS would include EM modeling. The slide was demonstrated that illustrated the vision of the parasitic extraction process in CoSMoS.

SCOTT DAVIS pointed that Cadence tools also do parasitic extraction.

RICHARD SHI agreed but pointed that CoSMoS parasitic circuit extractor will be a tool that is not currently available in industry and will connect directly with the behavioral modeler.

SCOTT BILLINGS mentioned that Boeing that a comprehensive library is definitely needed for behavioral modeling since, e.g., Boeing has sixteen different flavors of flip-flops.

RODNEY BONEBRIGHT asked what is parasitics.

SAMBUDDHA BHATTACHARYA answered that it includes capacitance, inductance, and resistance associated with traces, vias, ground, and interconnects.

RODNEY BONEBRIGHT pointed that speed is the issue and asked if the goal is to make the tool faster than other available tools

RICHARD SHI agreed and added that not only faster but also more precise.

RODNEY BONEBRIGHT said that Lawrence Livermore National Lab had problems with the mesher and the mesher is typically the bottleneck for the parasitic extractor.

SCOTT BILLINGS said that it is difficult to catch a human mistake ("if the error is between the chair and the keyboard") and so the extractor must be able to identify the parasitics that a human might miss.

RODNEY BONEBRIGHT mentioned that for analog AC & small signal analysis a subcircuit may be replaced with a four-port model but for a digital simulation it must be replaced with interconnects.

SCOTT BILLINGS inquired if the main idea is to have a unified tool for RF/analog/mixed.

RICHARD SHI confirmed that it is precisely so.

RODNEY BONEBRIGHT asked if the analog simulation is SPICE-based.

RICHARD SHI confirmed that it is.

RODNEY BONEBRIGHT commented that it is difficult to use SPICE beyond 5-6 GHz. One of the reasons is that transmission lines start exhibiting dispersion. Would CoSMoS handle this?

RICHARD SHI confirmed that it would.

RODNEY BONEBRIGHT stated that the user should not worry about the frequency range and decide which specific tool to use.

SCOTT BILLINGS agreed that such a decision should be made transparent to the

user.

RICHARD SHI said that this is a long-term research goal.

RODNEY BONEBRIGHT inquired if CoSMoS parasitic extractor is circuit function-aware. A designer doesn't need to simulate everything because, e.g., sensitivity to parasitics is very different at AC and DC.

RICHARD SHI said that the performance extraction is certainly an important area to be addressed, including parasitic aware digital behavioral modeling. It is, essentially, new technology, and is a current research problem.

GARY NELSON stated that UW and NeoLinear are very competitive since they are attacking the same market and presented the following comparison:

NeoLinear	***UW CoSMoS***
Use existing simulators on multiple machines	Develop its own fast simulator
Seek speed by parallelizing	Seek speed by integrating
Matlab graphs of multiple simulator results	Symbolic sensitivity analyzer
Standard parasitics	Enhanced parasitics
Optimize circuit elements	Same + library model selection
Active automated layout	No layout generation but layout analysis
Limits are set by SPICE	Beyond commercial limits
Each wire is a point node in SPICE	Wires are modeled as transmission lines
NeoLinear commercializes their tools	Orora commercializes UW tool

RODNEY BONEBRIGHT inquired about the role of Orora Design Technologies.

RICHARD SHI explained that Orora Design Technologies is a part of UW NeoCAD. The participation of a company is required by DARPA to transfer the technology.

RODNEY BONEBRIGHT said that UW is capable of doing things that they (Boeing) can't do, like simulation of RF/analog/digital coupling.

GARY NELSON mentioned a previous project based on 0.25um technology. The project had been re-fabricated 4 times because of the design difficulties.

RODNEY BONEBRIGHT agreed that coming up with a good demo test case is important and difficult. The #1 reason for second spins is the substrate coupling.

SCOTT BILLINGS said that a large micro controller without a behavioral model is difficult and slow to simulate since all it has is a standard VHDL description.

RODNEY BONEBRIGHT inquired how is CoSMoS solving the problems that designers currently have (or will have)?

RICHARD SHI answered by demonstrating slides on CoSMoS applications.

Slide #1 was titled “CoSMoS Application Demonstration-1: Model in a day concept”. Using SPICE for a project may involve 1 day of testing, 20 days of debugging and 30 days of coding wheres with CoSMoS 1 day is spent on each of debugging & testing and coding.

He also said that the future plan is to write an API for commercial simulators (Cadence) to be compatible with our designs.

Slide #2 was titled “CoSMoS Application Demonstration-2: Beast of parasitics and beauty of behavioral modeling”.

Slide #3 was titled “CoSMoS Application Demonstration-3: A/D converter design”.

RODNEY BONEBRIGHT commented that main problems arise from substrate coupling and power supply. The fact that the problem is too big makes a designer to decide what not to simulate. Automating this process (optimization) is important. He emphasized that fastness is not the main advantage since CPU's become cheaper and cheaper. New capabilities are important (new algorithms vs. using more processors).

GARY NELSON posed the question - what exactly needs to be done before December?

RICHARD SHI said that trying out a big realistic design from Boeing would be extremely useful.

GARY NELSON said that Boeing has a design for an auto-zero amplifier with approximately 50 transistors, which needs to be moved from Bi-CMOS to CMOS to reduce unwanted sensibility to radiation.

SCOTT DAVIS added that there are other designs as well.

RICHARD SHI said that he would try to integrate all given suggestions into the three slides to be submitted to DARPA.

RODNEY BONEBRIGHT mentioned that he has a few designs with inductors that he can email to UW researchers. Boeing currently uses EM package Sonnet to simulate those designs. To be productive, a designer must be able to finish simulation in 2-3 hours. Full wave simulation is not always needed for solving the problem since circuit performance is typically limited by transistors.

GARY NELSON said that the goal is usually to make a quick, cheap, and good product, but only two out of those three points can typically be achieved at the same time.

MEETING SUMMARY

1) Material to be submitted to DARPA was approved.
2) It was decided that more close interaction between UW and Boeing is required, including realistic design cases passed on to UW.