A FULLY DRY SELF-ASSEMBLY PROCESS WITH PROPER IN-PLANE ORIENTATION

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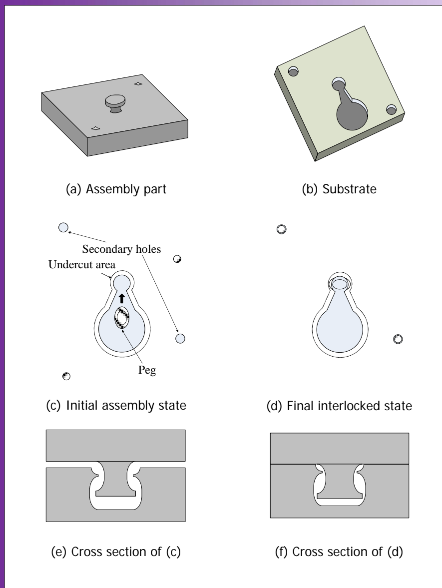
Abstract

A fully dry self-assembly method for chip-to-wafer stacking is developed in this paper. The assembly elements and substrate have complementary and interlocking features that place the assembly parts in the designated binding sites on the substrate. Proper in-plane orientation is achieved by deploying secondary features on the parts and substrate. These features are fabricated by a series of silicon deep RIE, sidewall passivation coating and isotropic etching. Experimental results show 100% assembly is accomplished on substrates with 2cm diameter, and 95% of assembly is done within 1 minute.

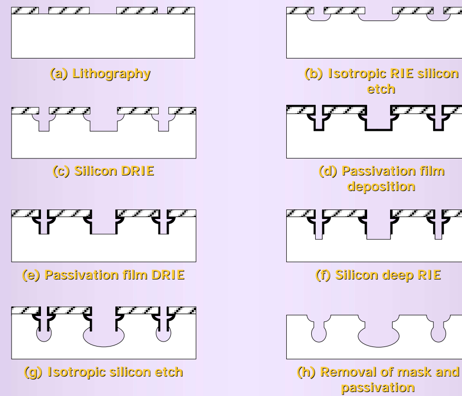
Motivation

- 3-D integration can:
  - provide larger packing density by vertically stacking several chips.
  - improve the performance and reduce the power consumption by eliminating long horizontal wiring.
- 3-D integration based on wafer-to-wafer bonding method is only applicable to devices with high process yield.
- Chip-to-wafer bonding strategy with parallel self-assembly is necessary for high throughput.

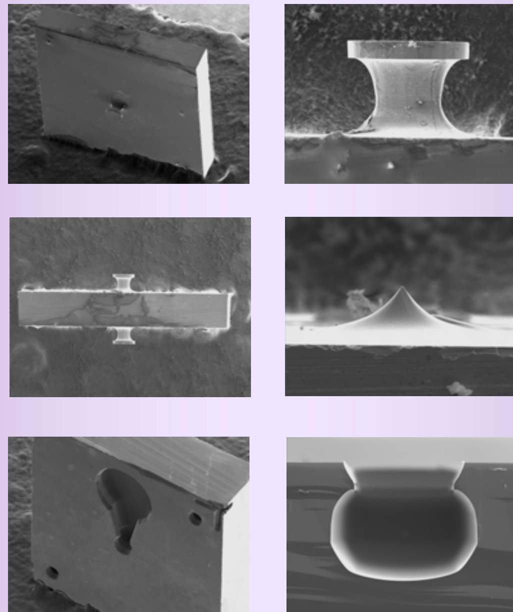
Design of Assembly System



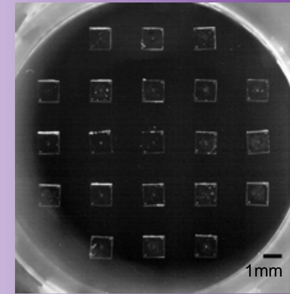
Fabrication



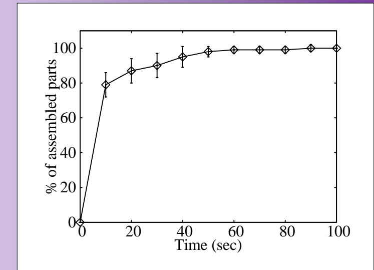
Fabrication Results



Experimental Results



- Self-assembled parts on substrate. The maximum orientation error is 1.7 degrees and the maximum translational error is ± 5 μm.



- Plot of assembly rate. The error bars indicate the standard deviation. The data are averages of 10 iterations. 95% of assembly is reached within 1 minute of vibration.

Conclusion

- A fully dry self-assembly method for chip-to-wafer stacking was developed.
- A high assembly yield and a high assembly rate were achieved as well as proper in-plane orientation of the parts.
- Multiple stacking of various elements in a designated order can be implemented.

Acknowledgments

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- Please also have a visit to our group's work on micro self assembly, "Catalyst Enhanced Micro Scale Batch Assembly," poster no. 223.