A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth

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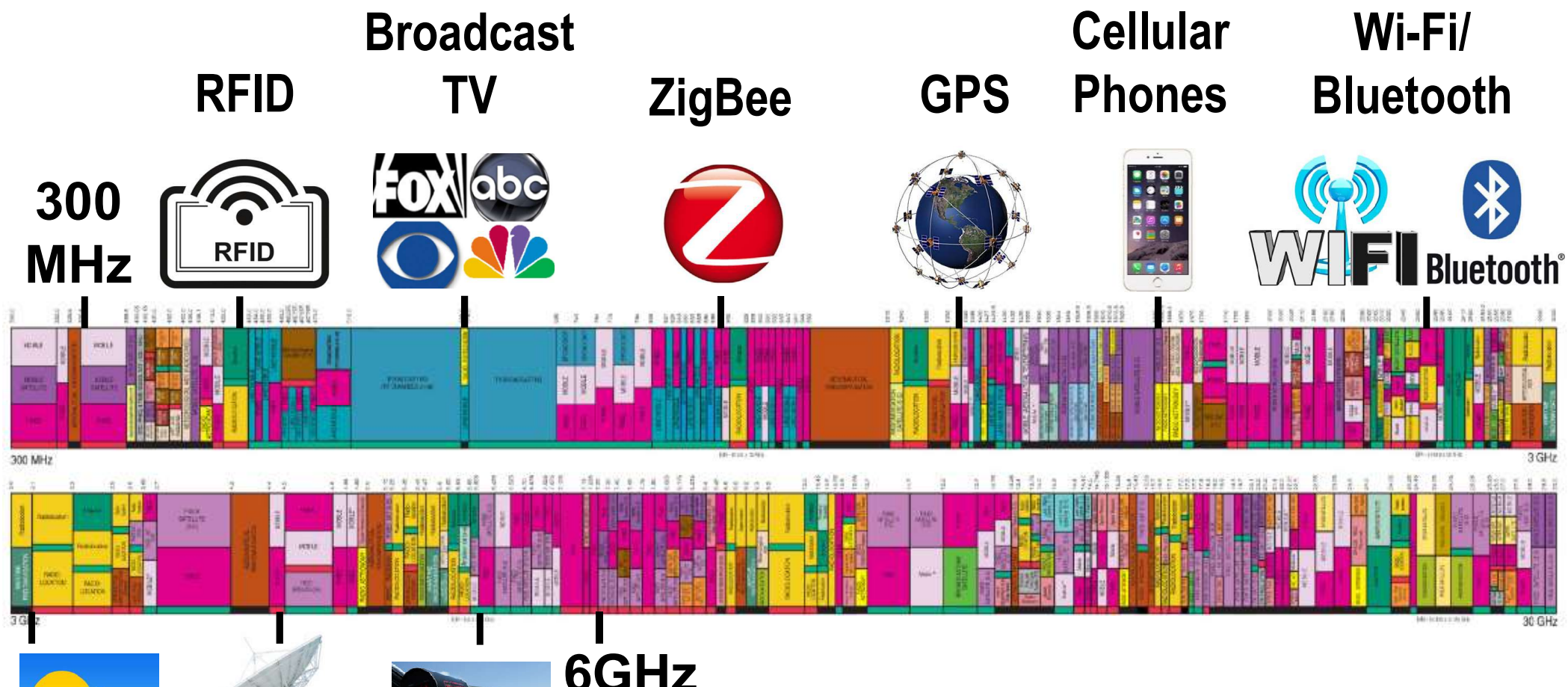
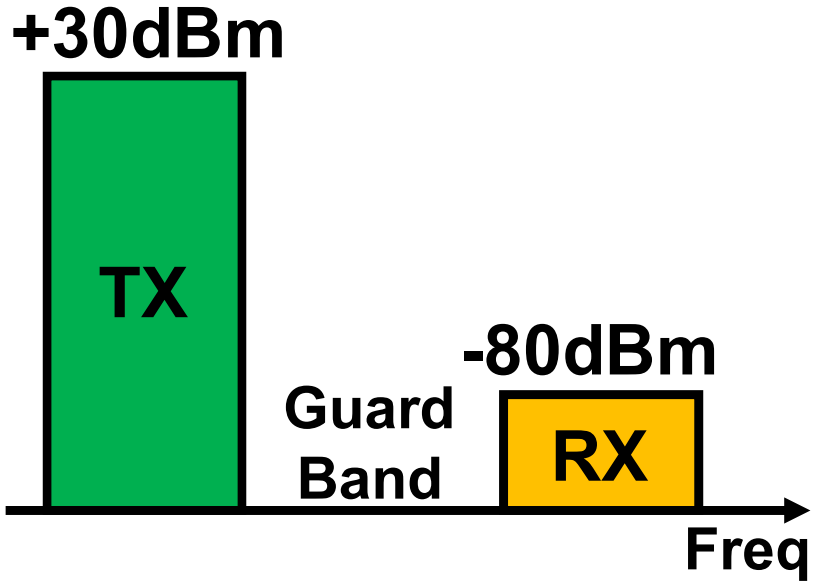
Very Crowded RF Spectrum



RF spectrum has become saturated w/ standards.

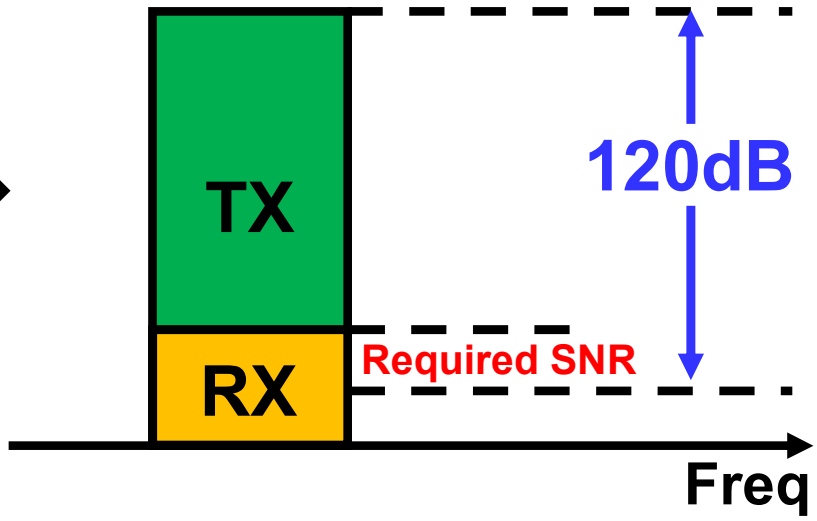
Full-Duplex (FD) Communication

Frequency Division Duplex （FDD)



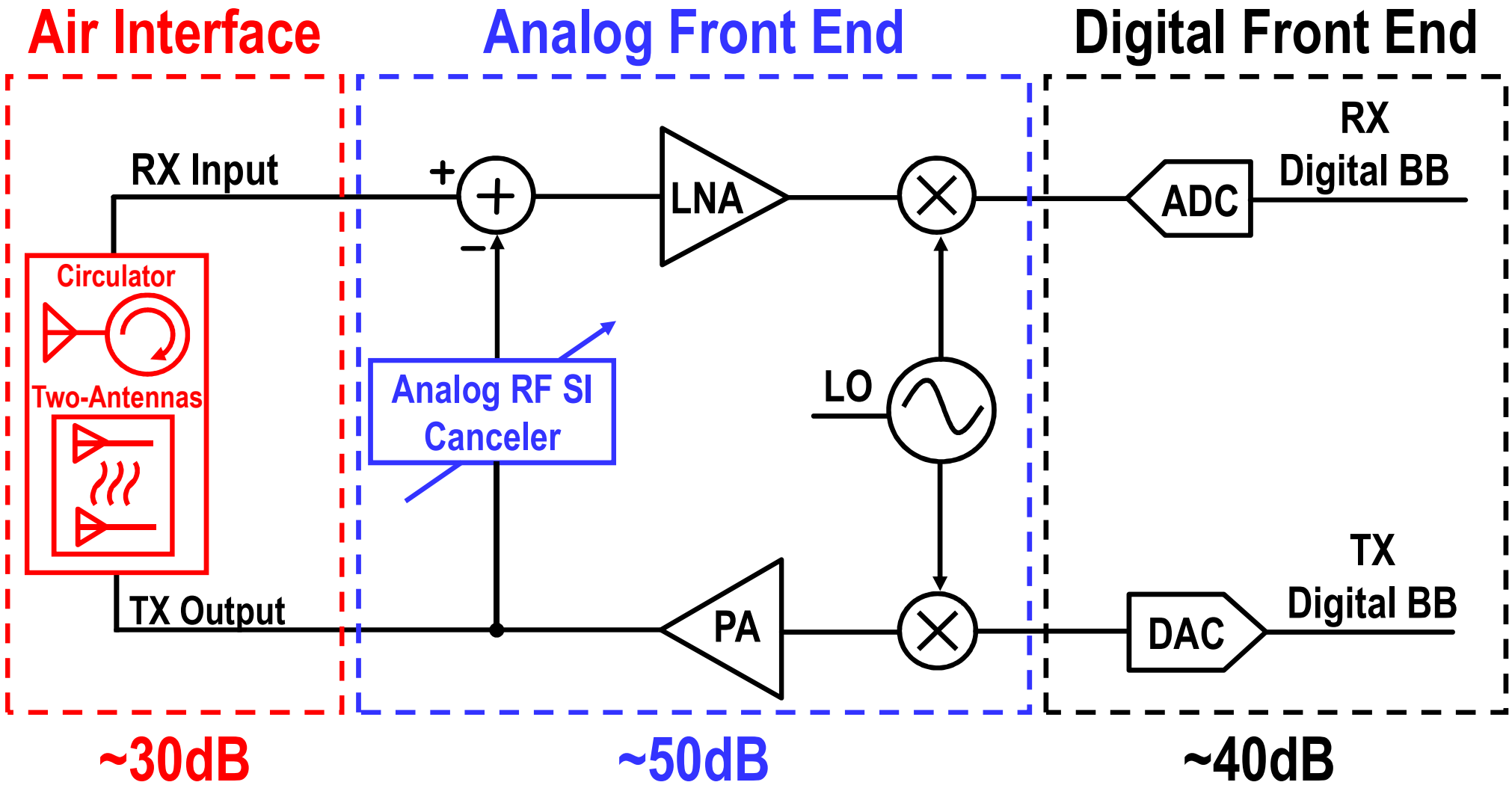
Higher Spectral η

In-band Full-Duplex (FD)



FD communication potentially improves spectral efficiency up to 2X.

Assumed SI Cancellation Distribution

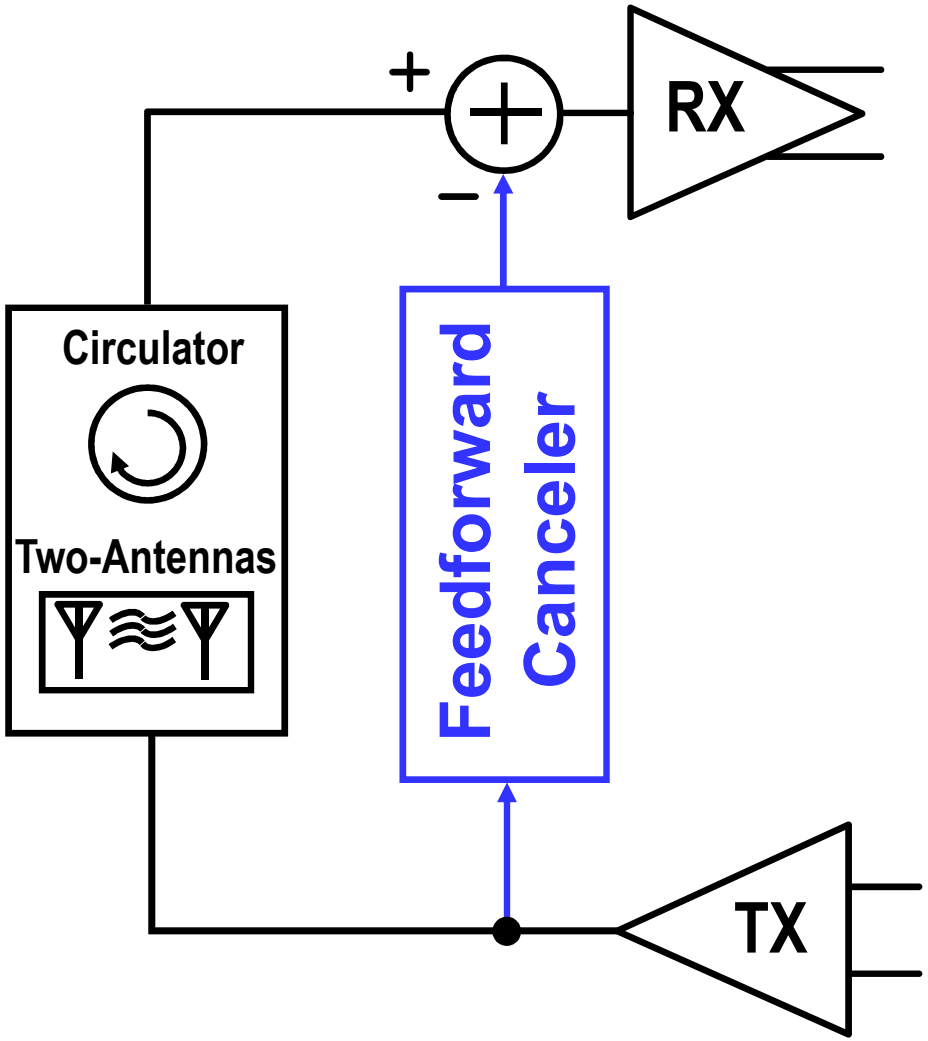


This analog front-end chip targets 50dB SI Cancellation over a 42MHz BW

Outline

- Wideband SI Cancellation Challenges
- Proposed Dual-path Canceler
- A Prototype 40nm CMOS FD Radio
- Measurement Results
- Conclusion

Self-Interference Cancellation (SIC) in FD Radio

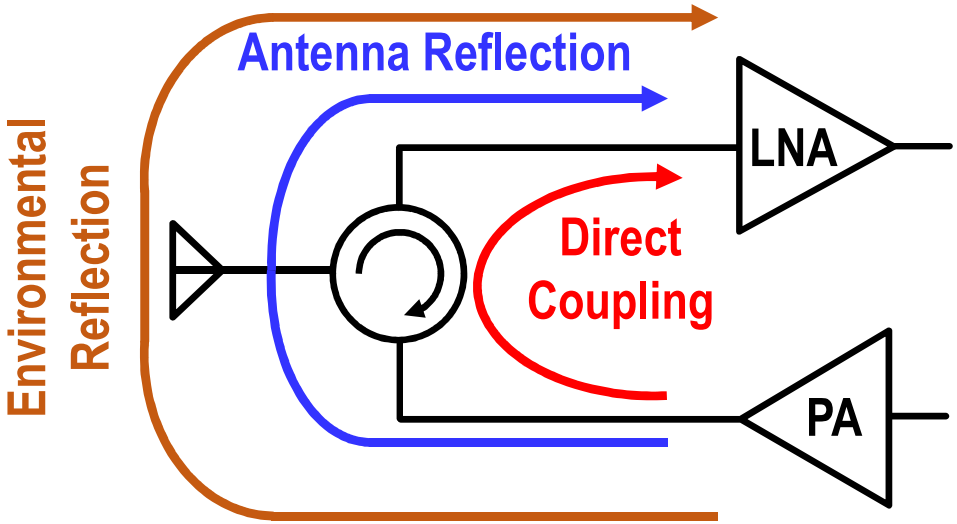


Ideal SI Canceler

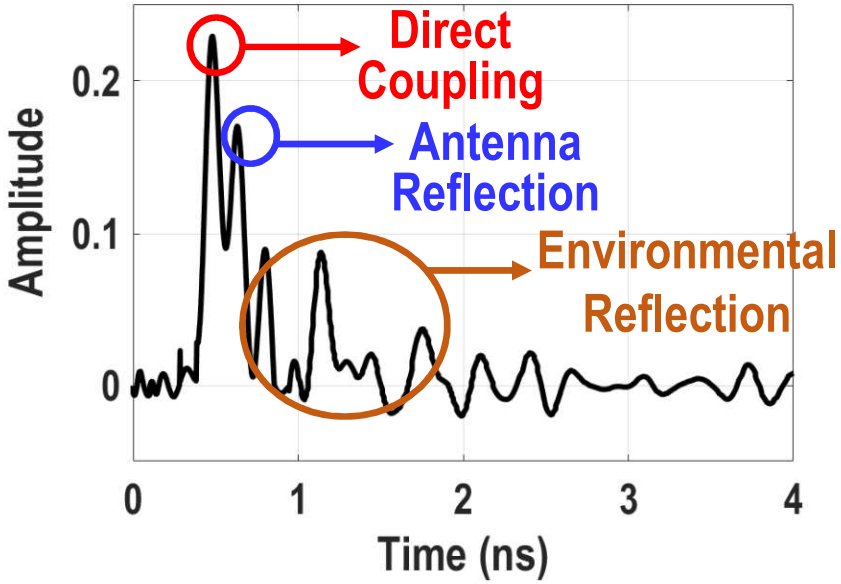
- Cancel @ RX input
- Wide cancellation BW
- Minimal noise, power, area
- High linearity
- Large In/Out impedance

Leakage Path Channel Response

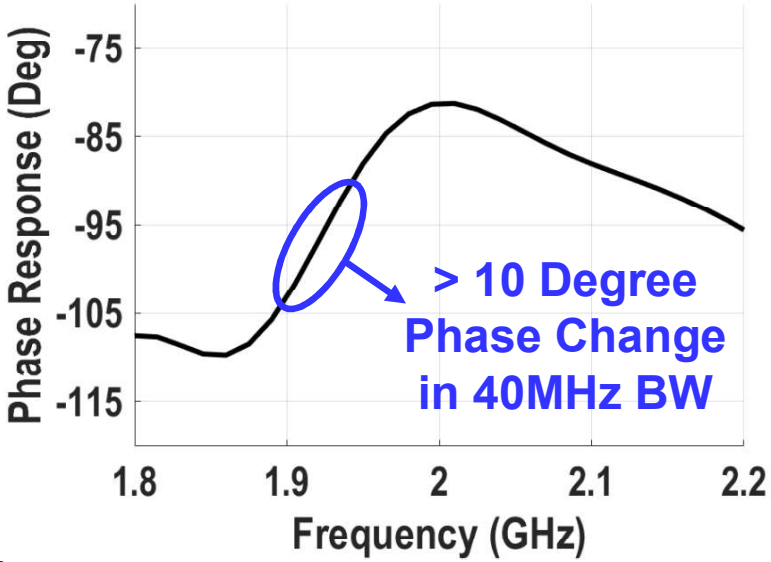
Time Delay Versions of Leakage Signal



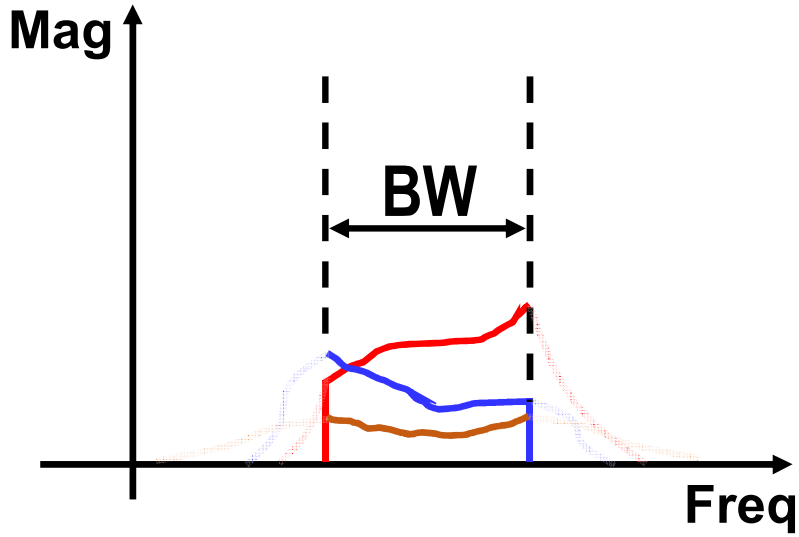
Circulator Impulse Response



Circulator Phase Response

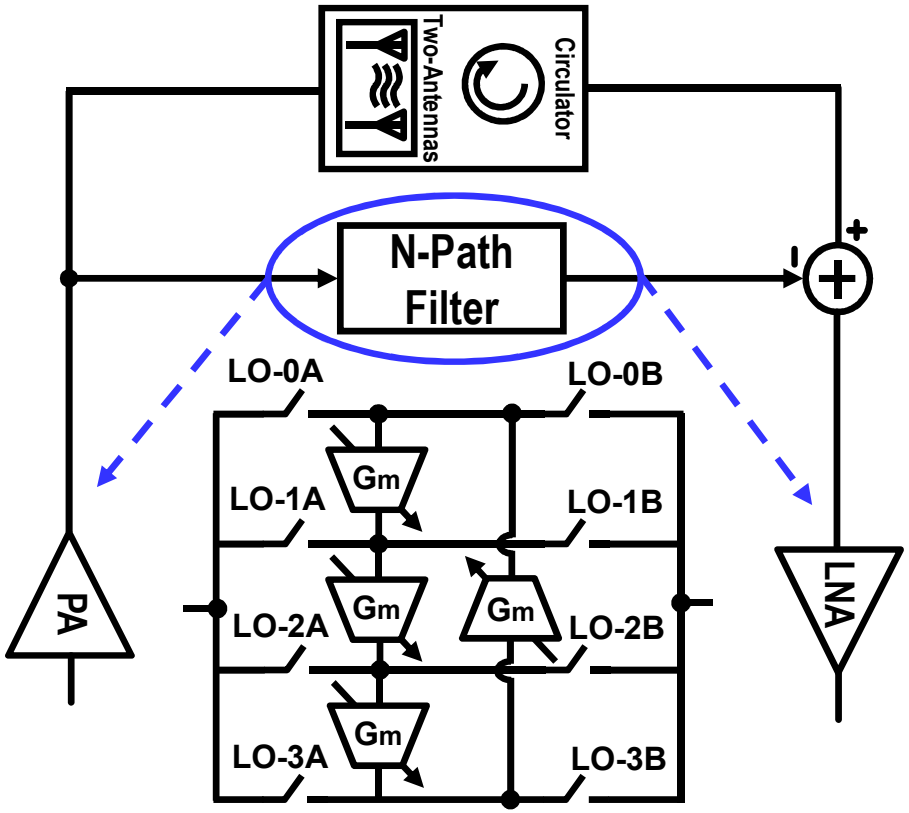


Leakage Path Channel Response



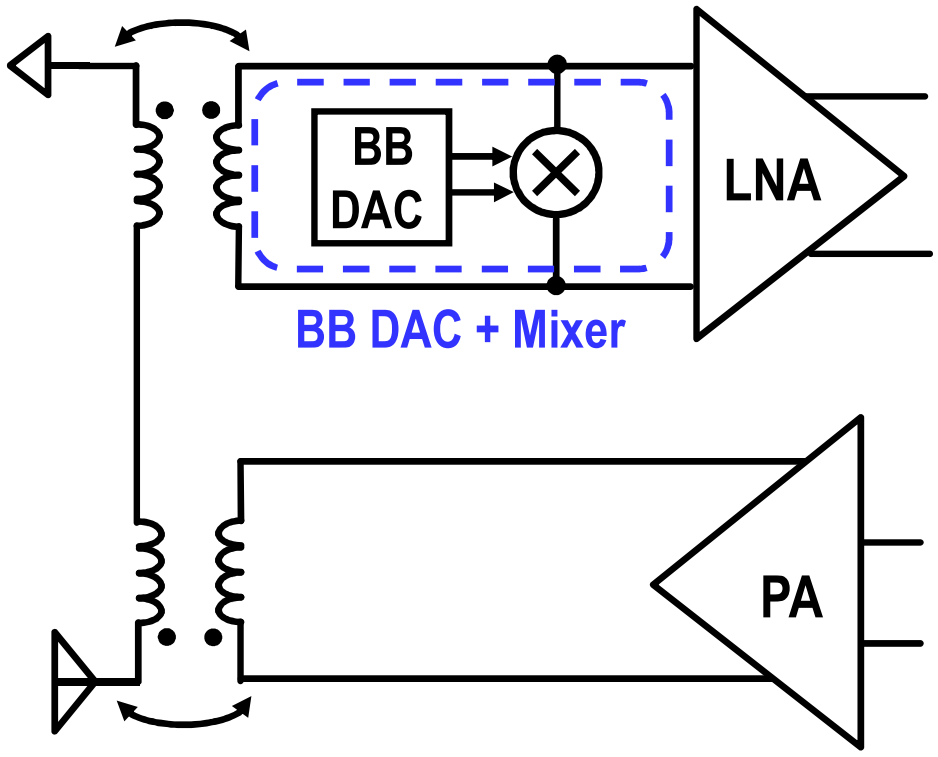
Wideband SIC Prior-Art

RF Frequency Domain Equalization



J. Zhou et al, ISSCC 2015

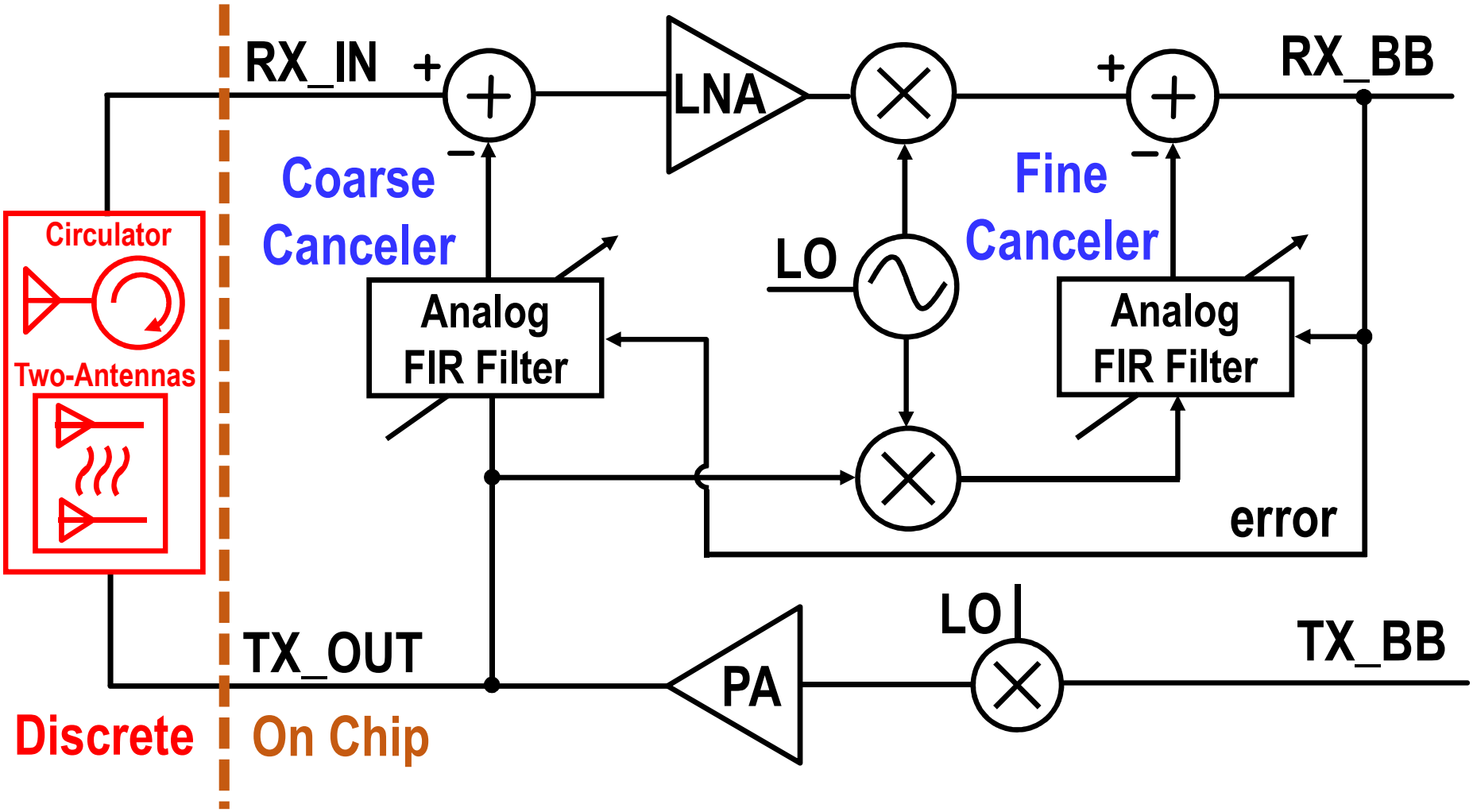
High Speed Current DAC Synthesizes Inverse TX



S. Ramakrishnan et al, VLSI 2016

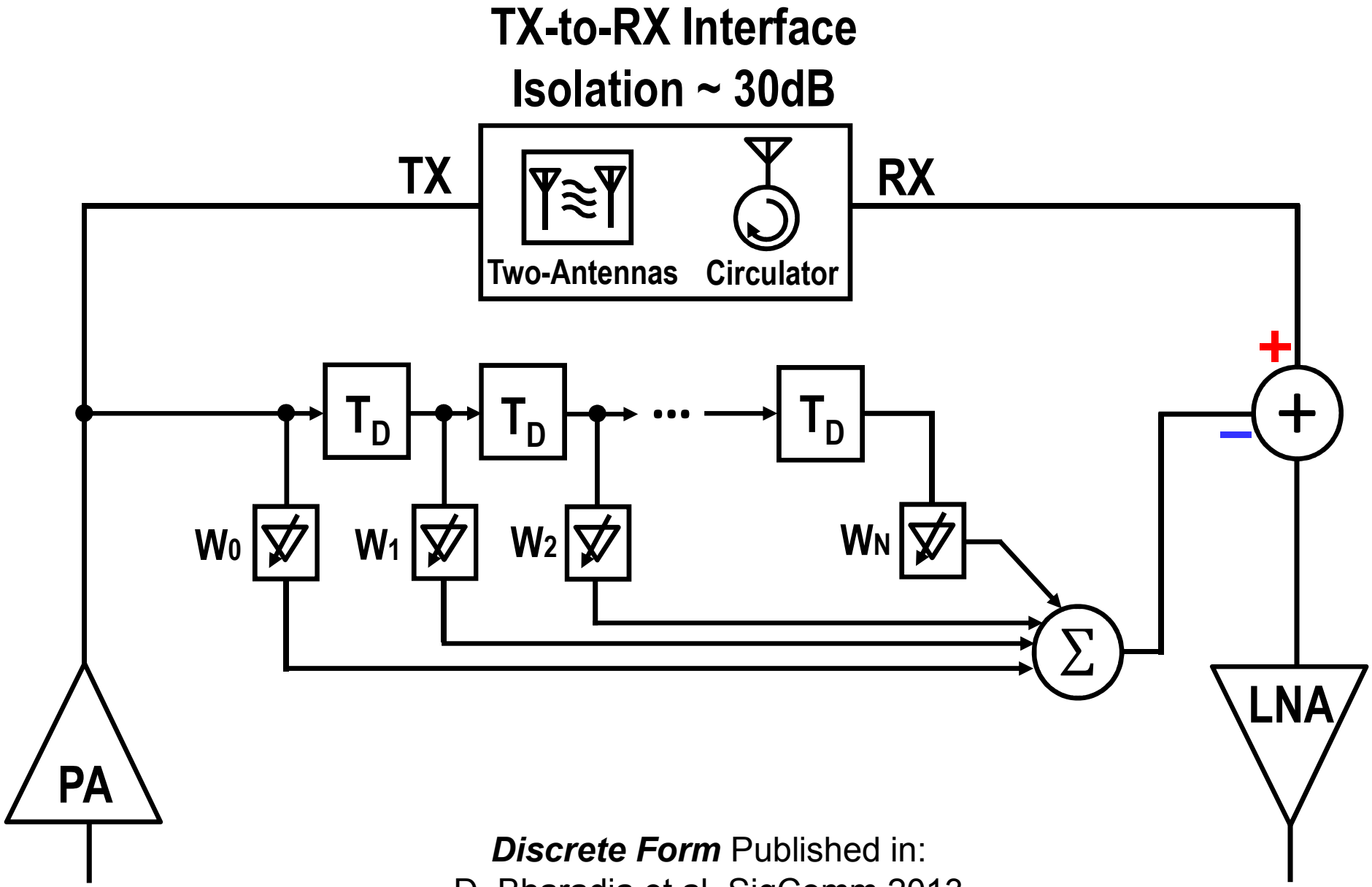
Challenging to design a single path broadband, high SI canceler

Dual-Path Self-Interference Architecture



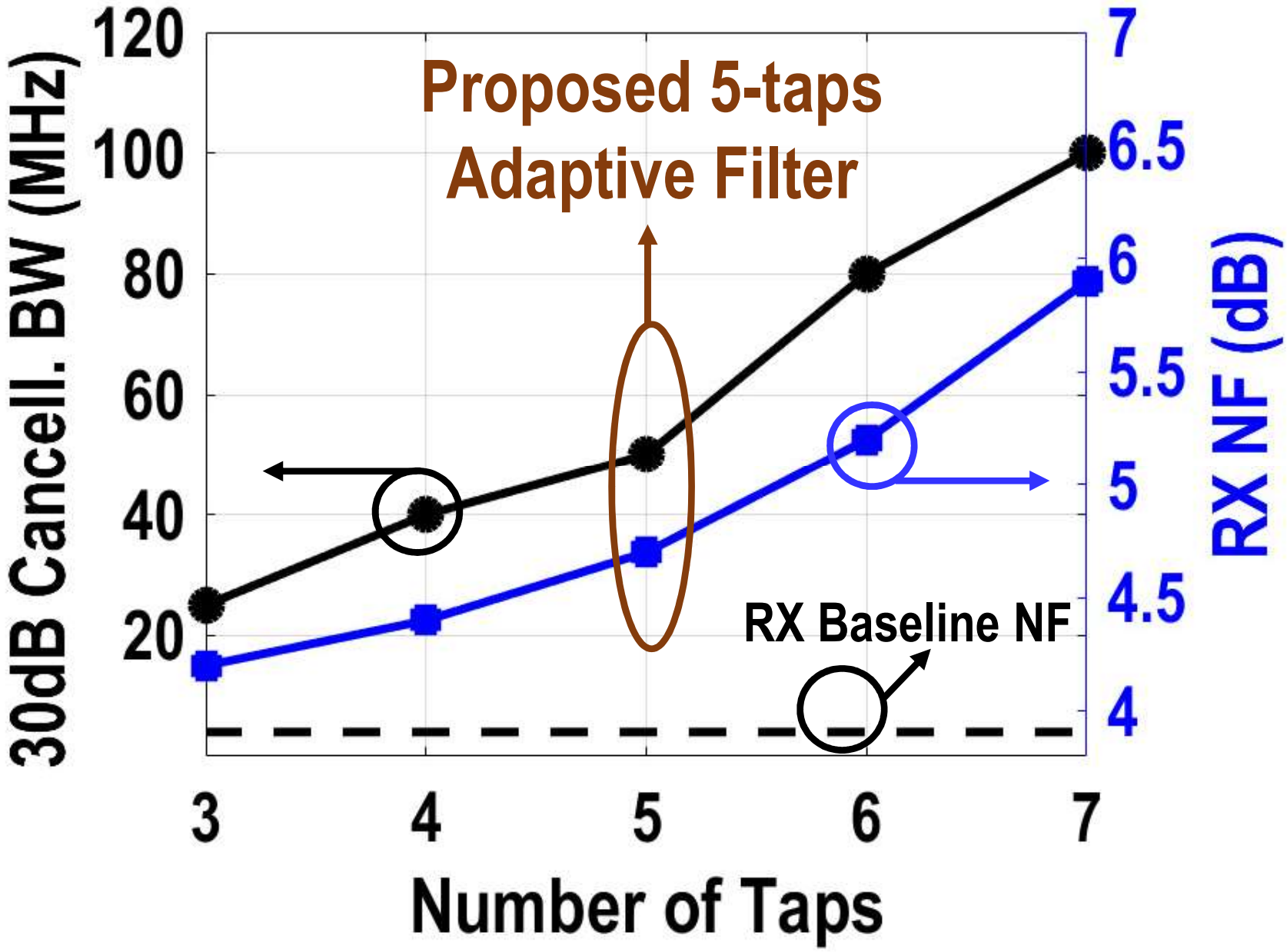
- Two cancellation paths, at RF and Baseband
- Enhance the SI cancellation depth and BW

RF Canceler Top Level Diagram

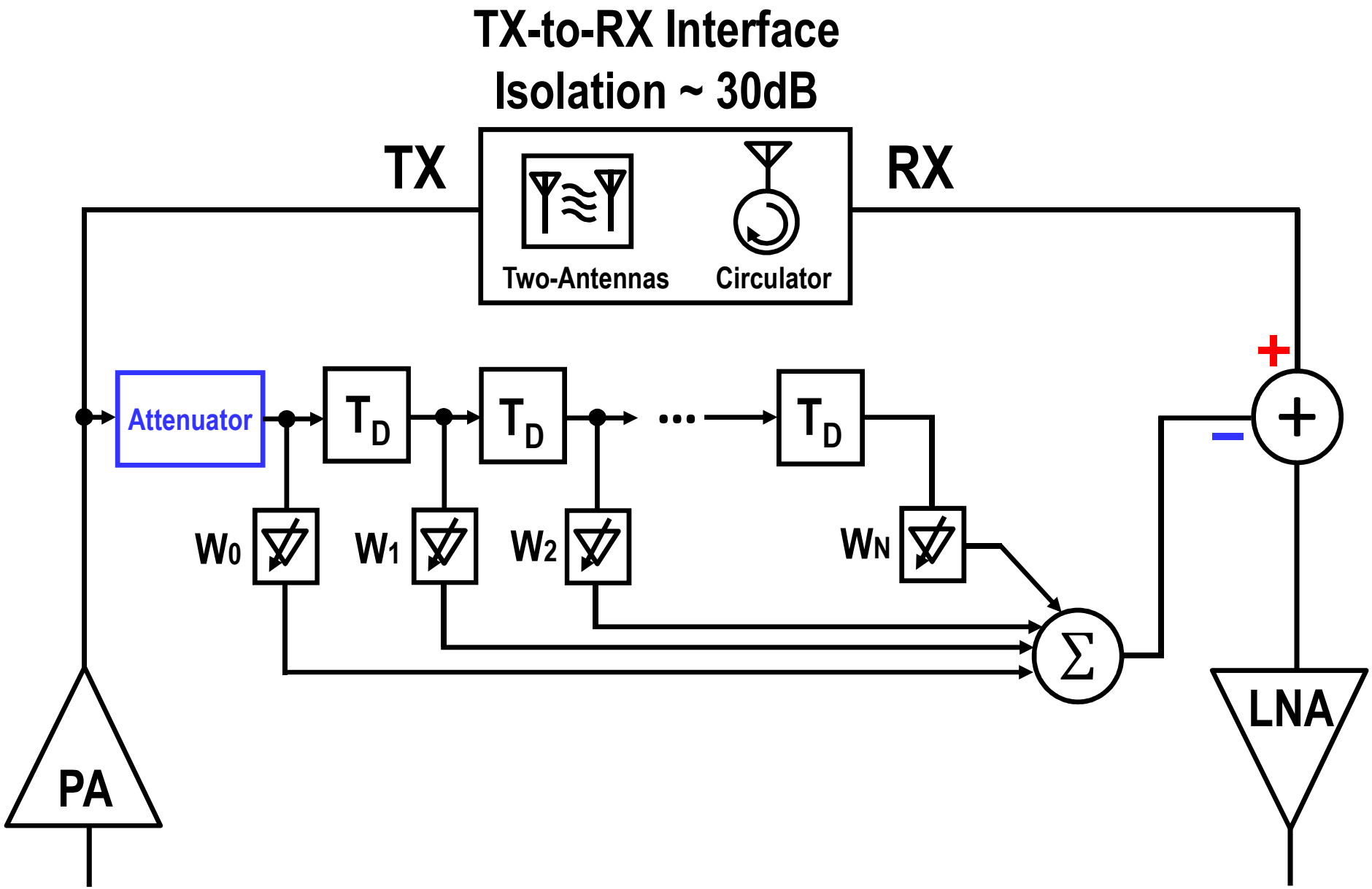


Discrete Form Published in:
D. Bharadia et al, SigComm 2013

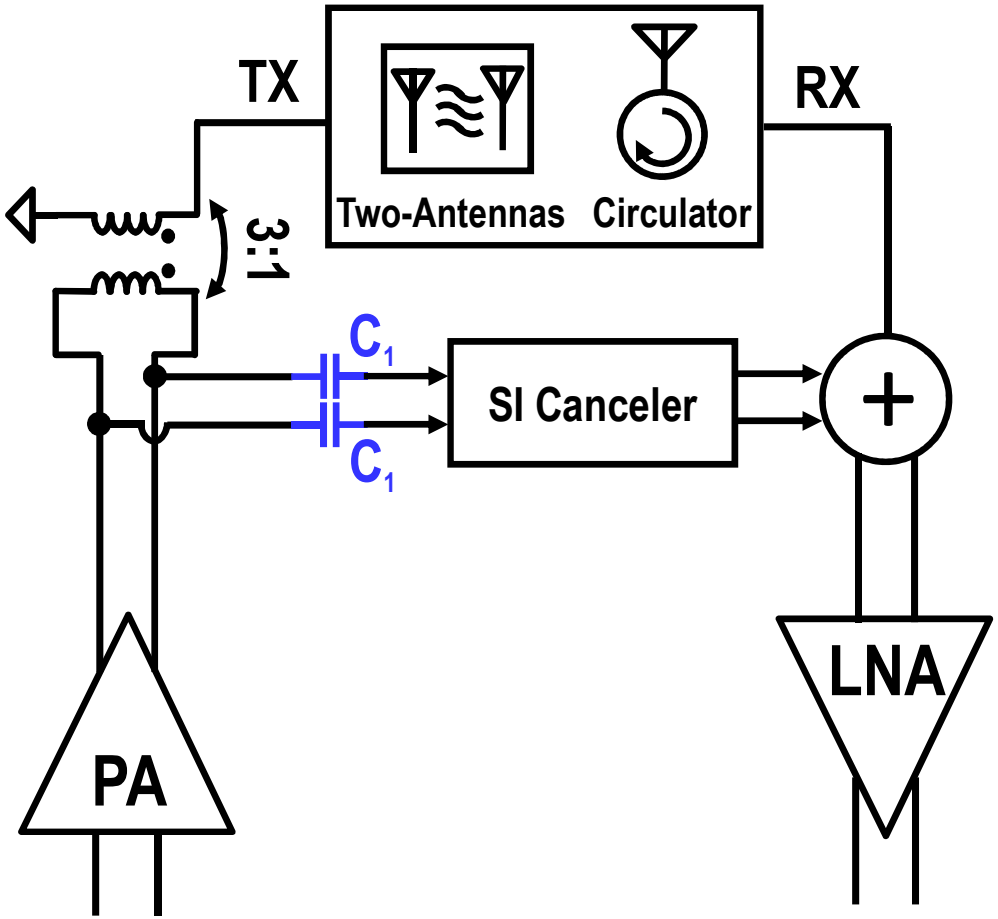
Canceler Noise - BW Tradeoffs



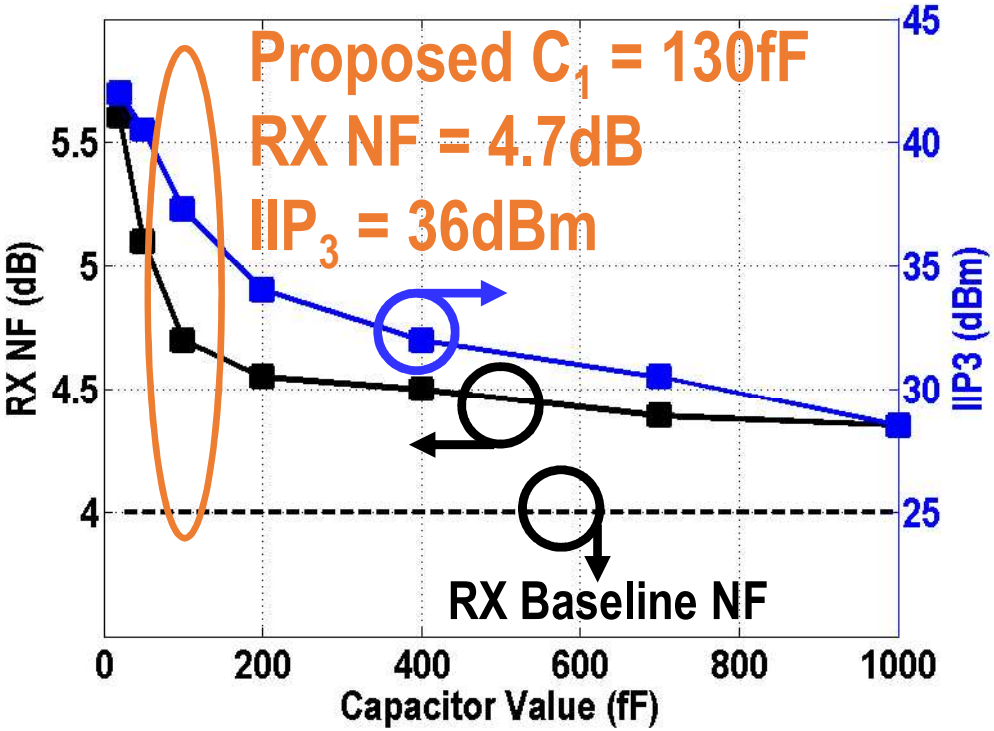
Linearity of the RF Canceler



RF Canceler Linearity vs C_1

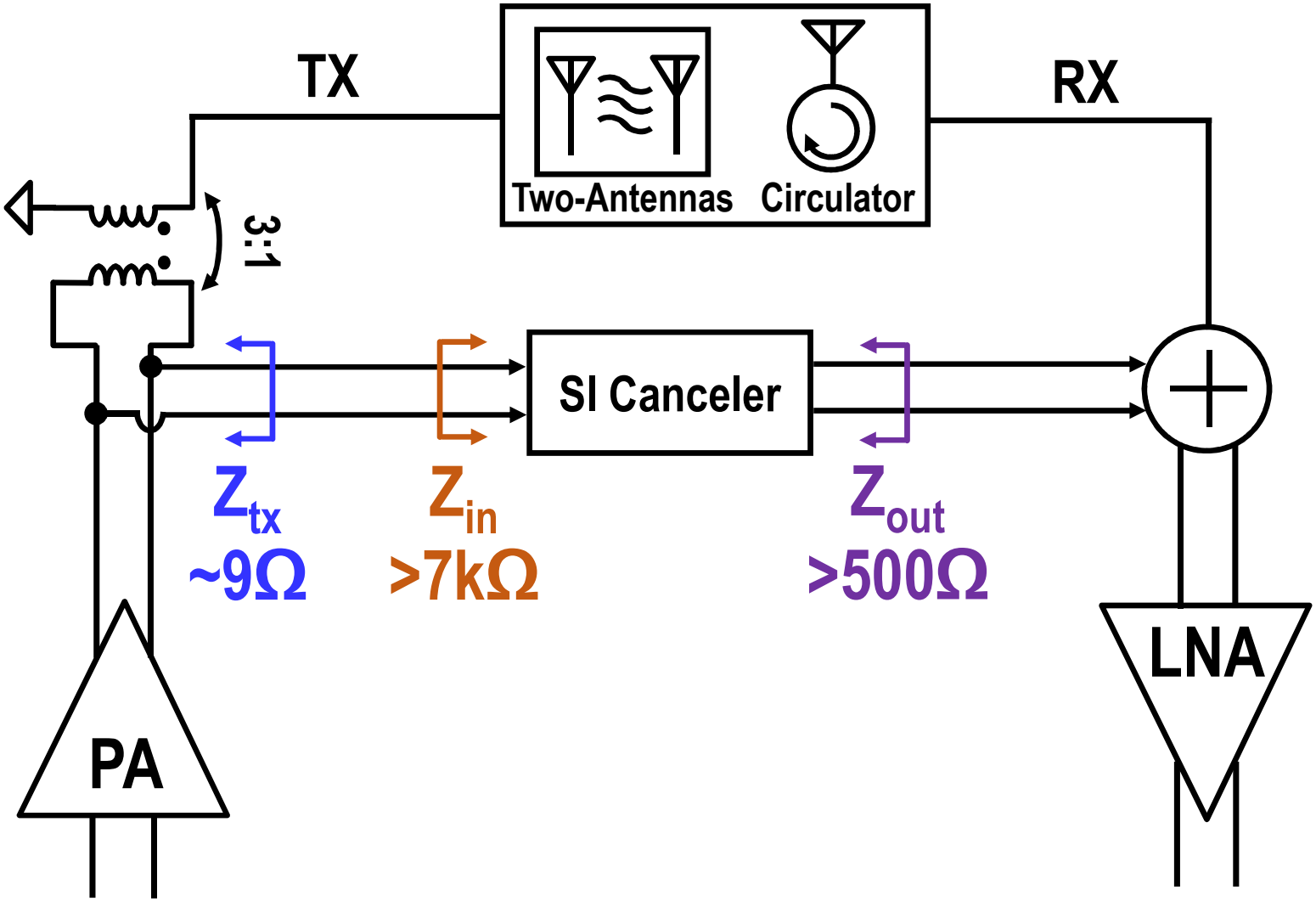


Canceler Linearity, RX NF versus C_1



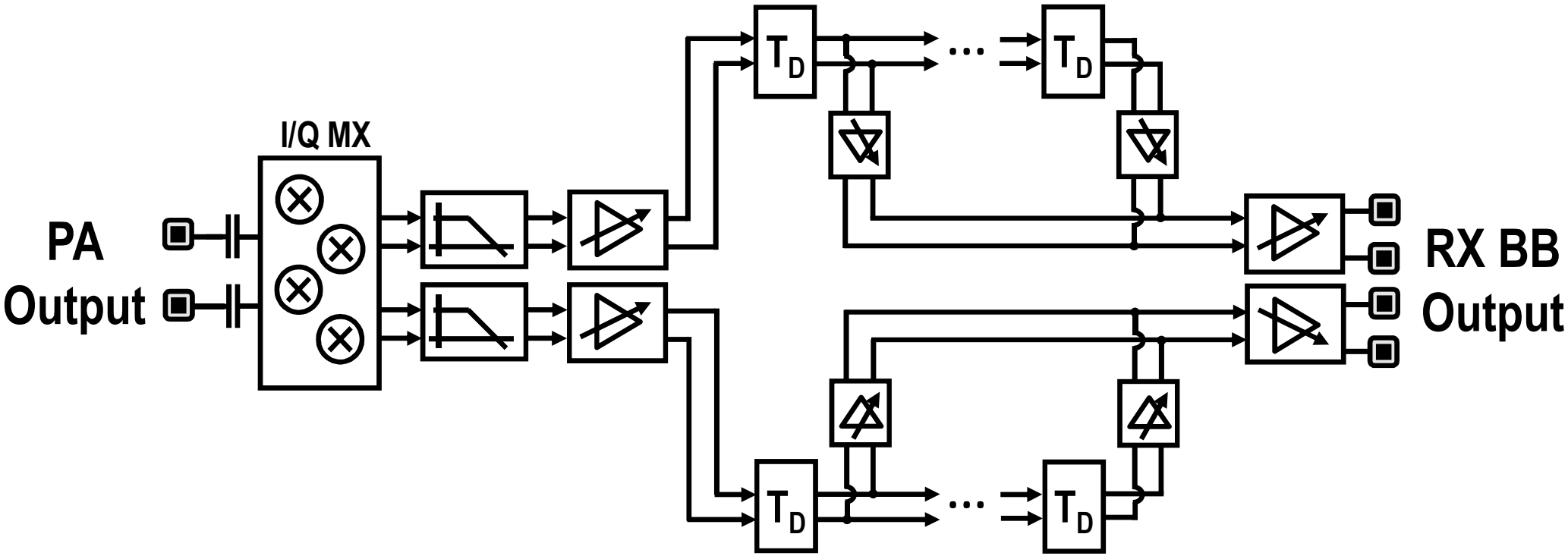
C_1 provides attenuation to improve canceler IIP_3

RF Canceler Linearity vs Z_{tx}



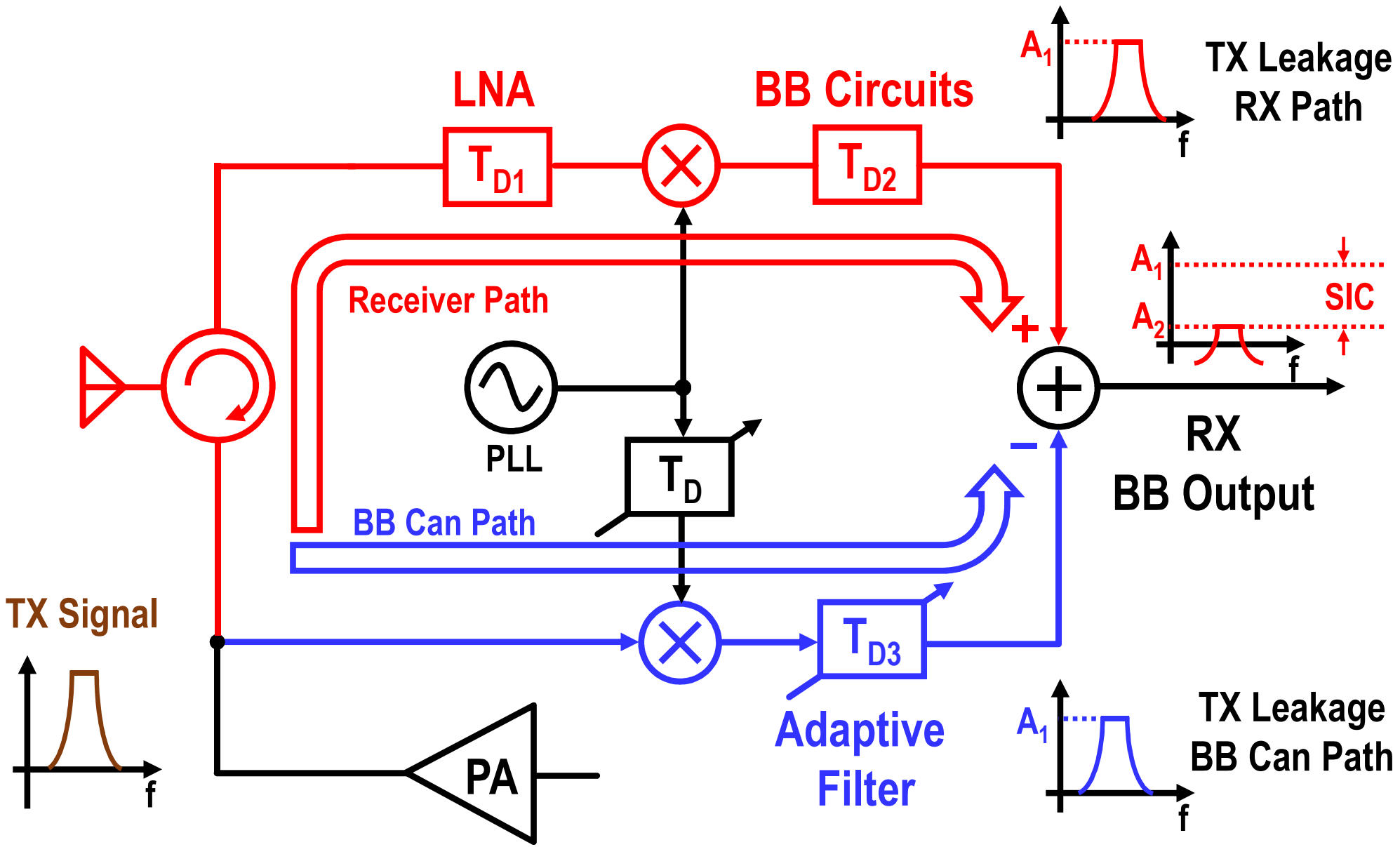
- Low Z_{tx} reduces input voltage swing of the SI canceler
- Large Z_{in} / Z_{out} relax loading for PA/LNA matching network

BB Canceller Top Level Diagram



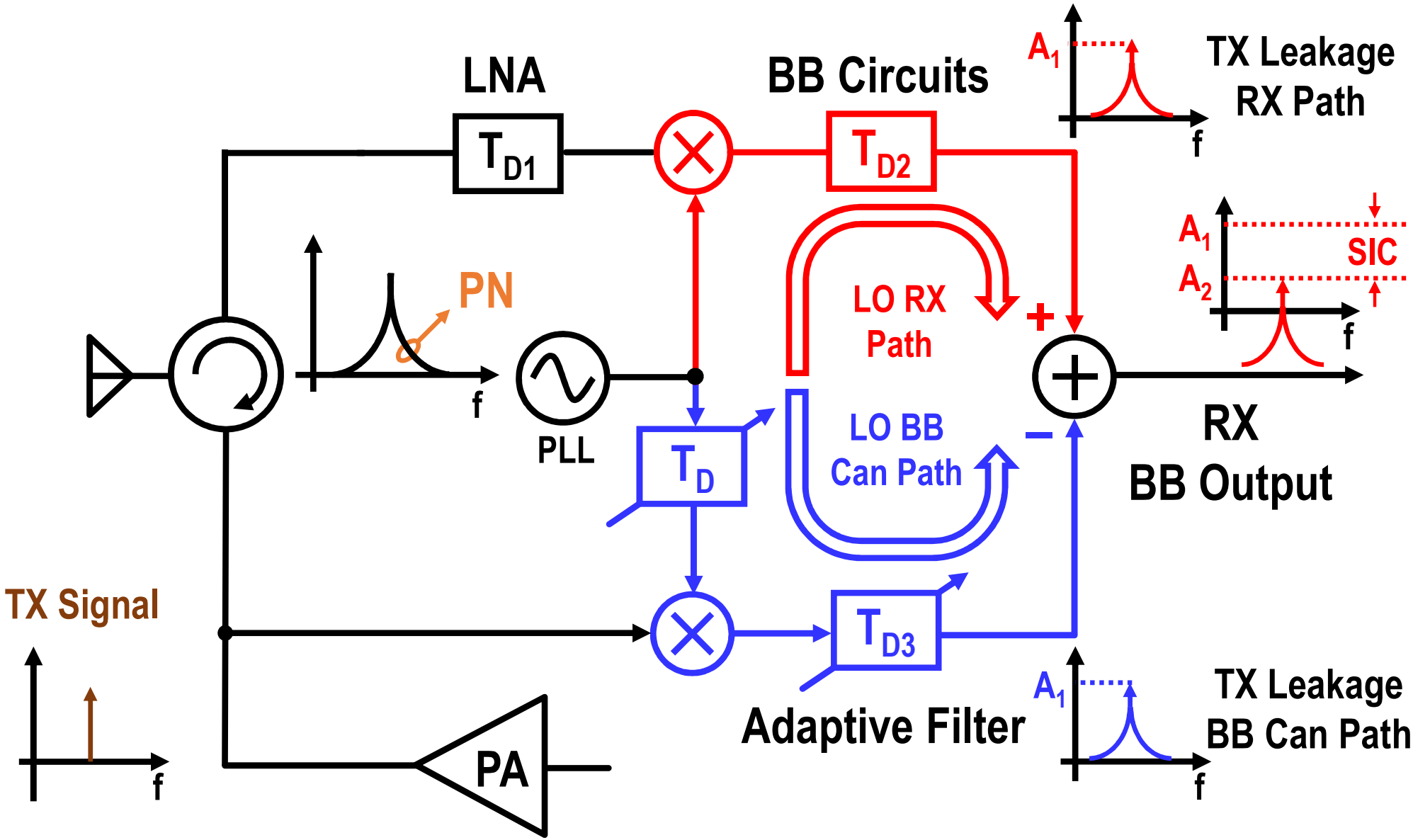
- Canceller path includes down-conversion mixer
- Design methodology similar to RF canceller

Baseband Path Delay Compensation



Delay Match between RX & BB Cancellation Path for TX Carrier

TX SI Phase Noise Cancellation



Cancellation of TX leakage reciprocal mixing with LO PN in RX

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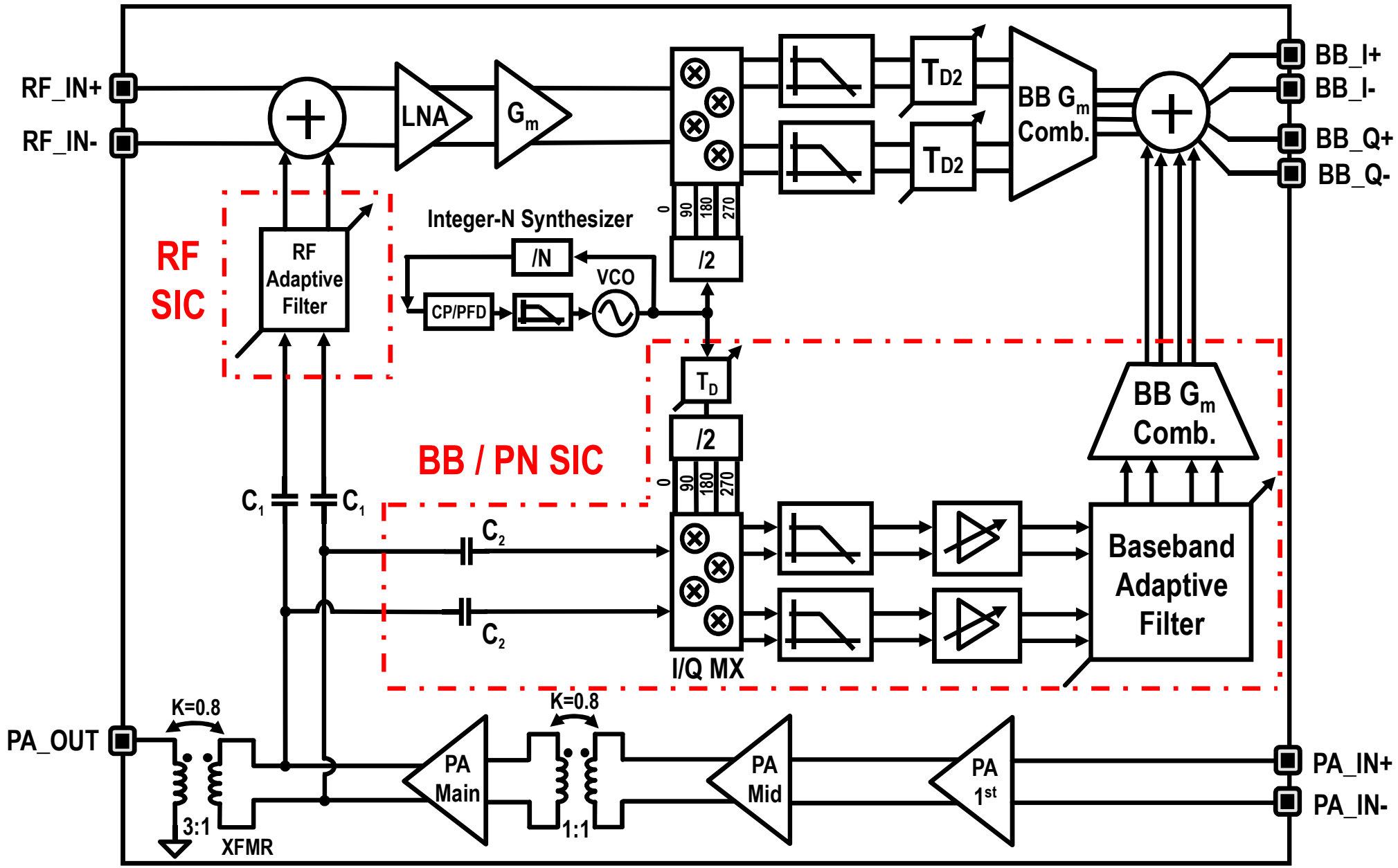
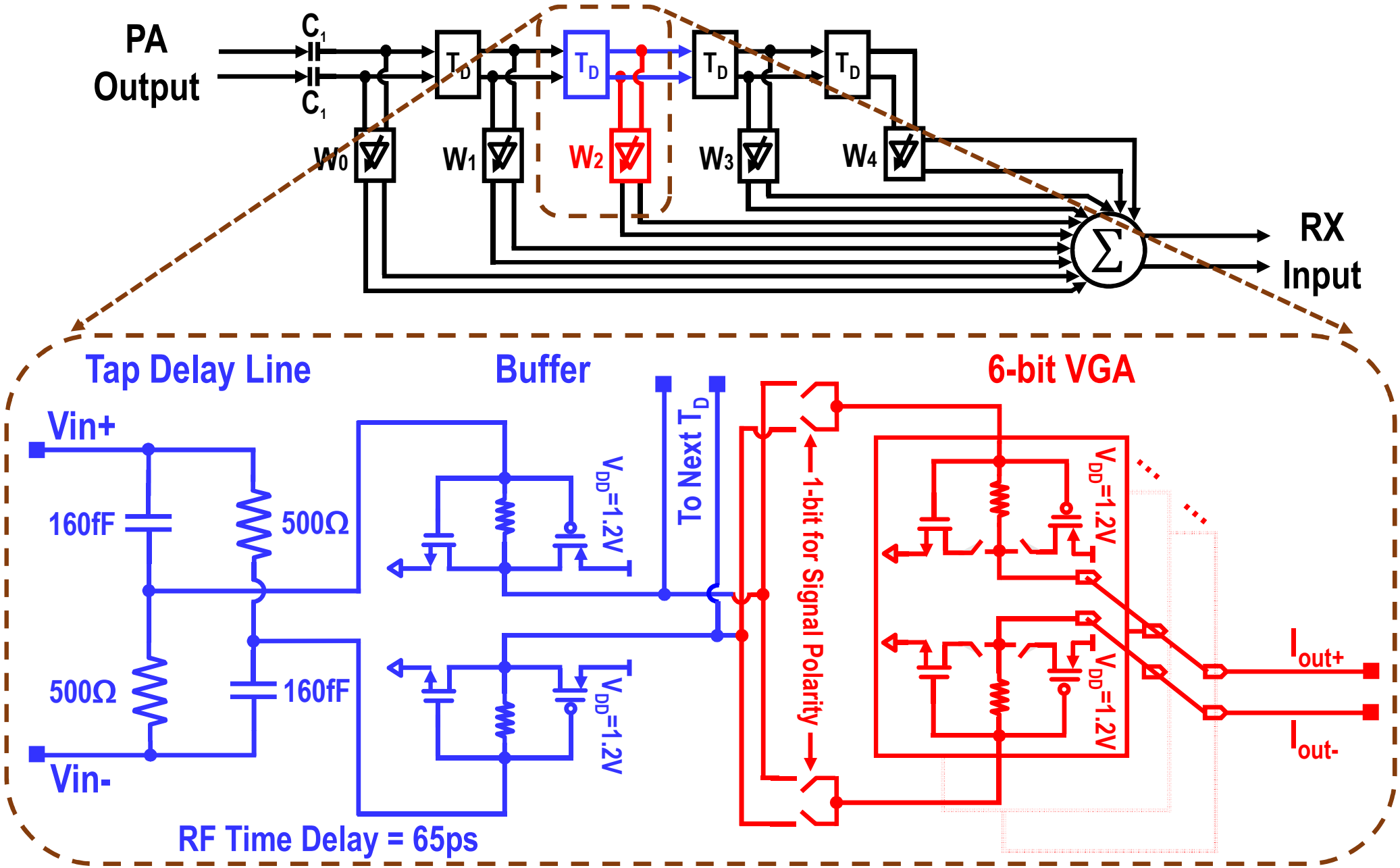
A 40nm CMOS Implementation of Proposed FD System

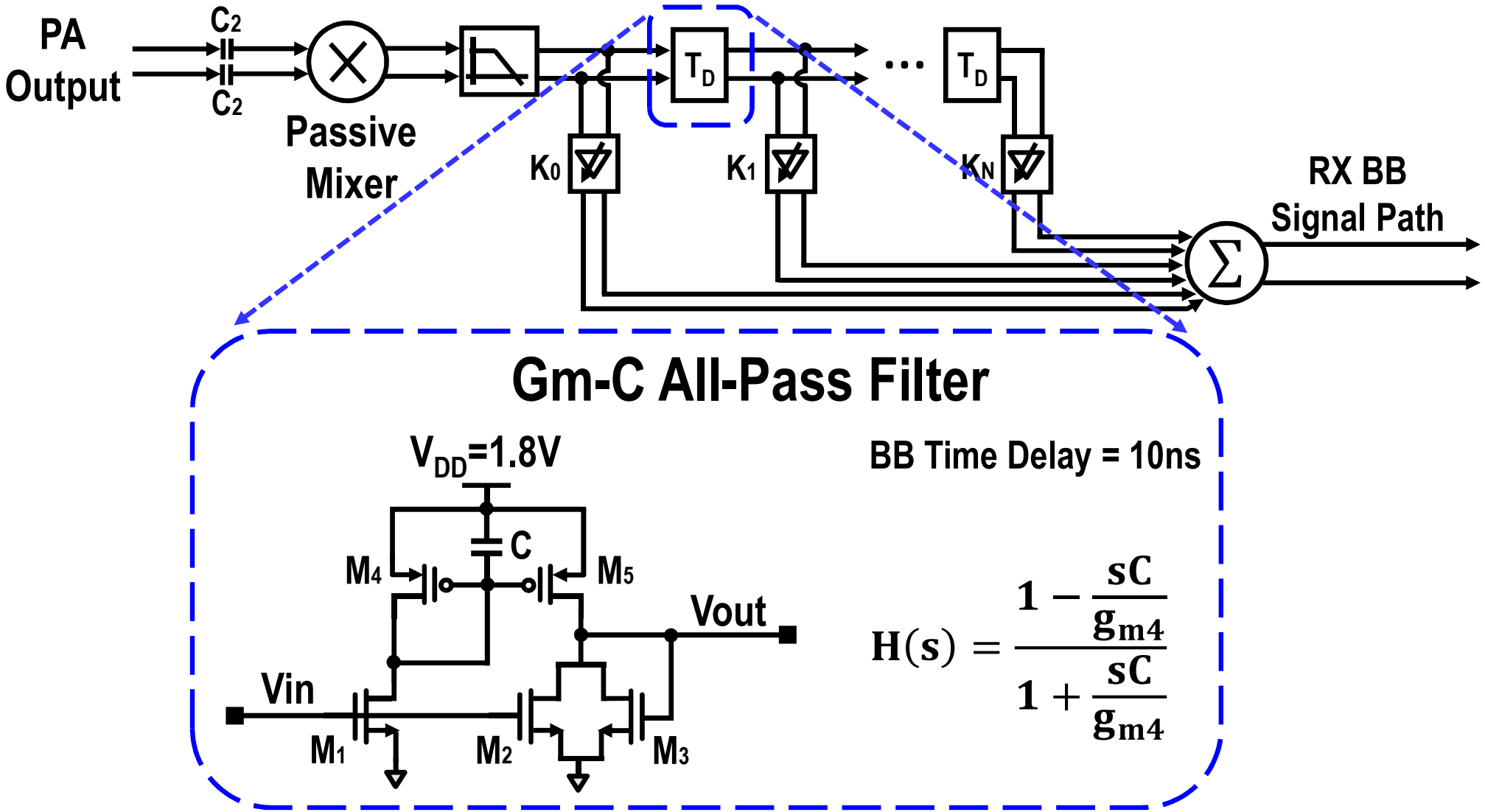


RF Analog FIR-Based Canceller



RF Canceler P_{-1dB} = 27dBm, IIP_3 = 36dBm

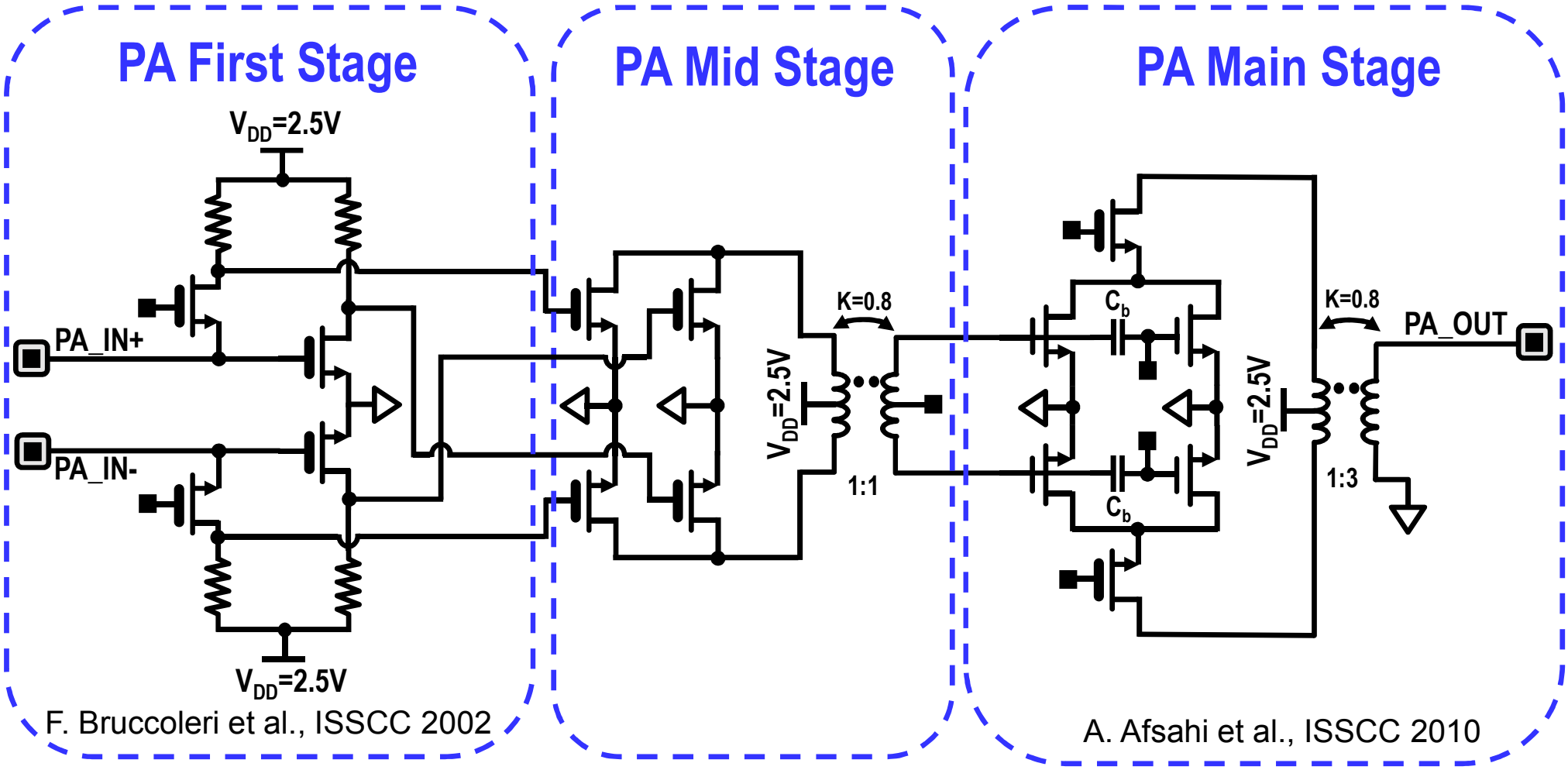
BB Analog FIR-Based Canceller



BB Canceler P_{-1dB} = 26.5dBm, IIP_3 = 34.5dBm

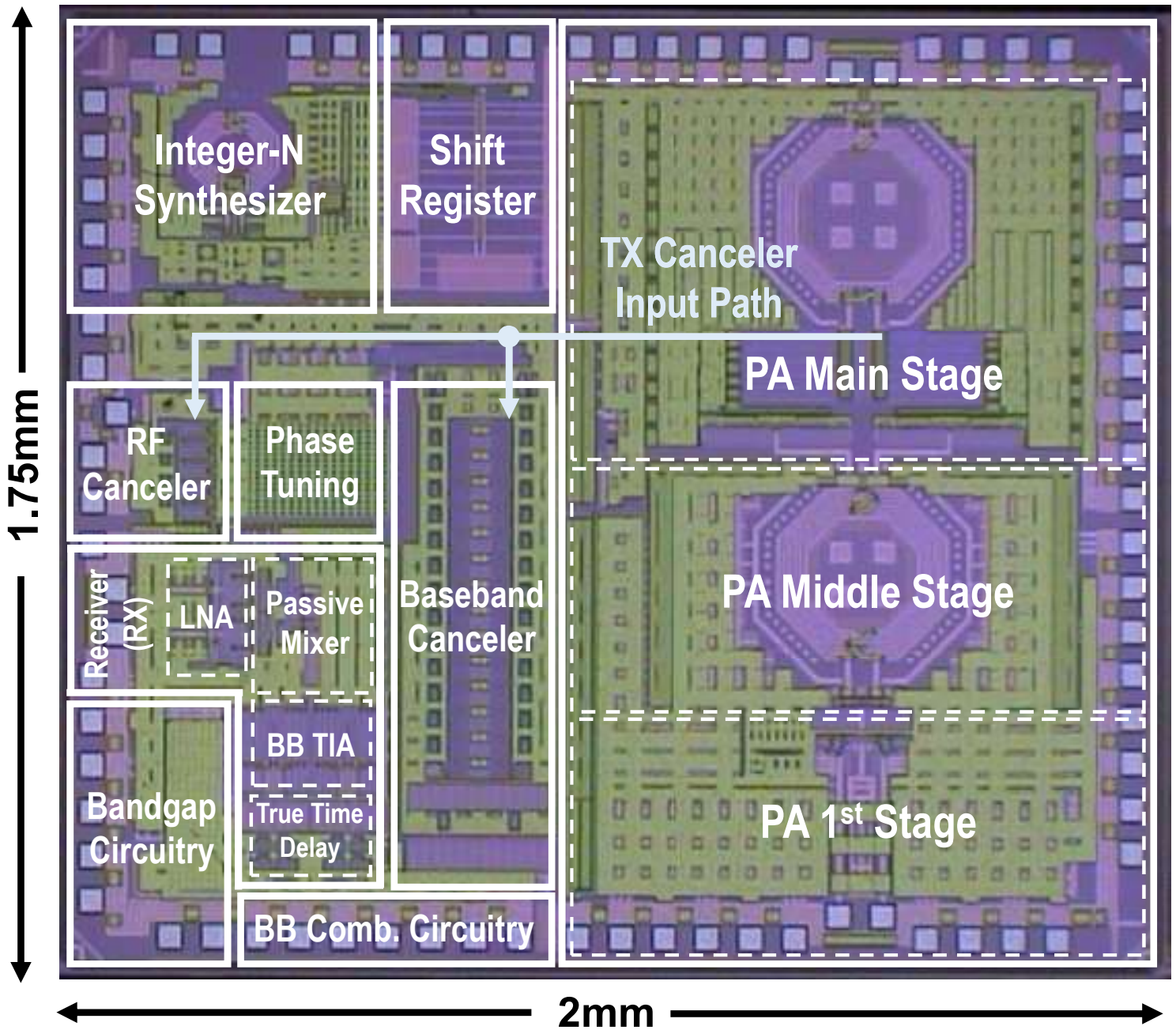
S. K. Garakoui et al., JSSC 2015

Power Amplifier Topology



- First Stage uses noise-cancelling topology to reduce output noise floor
- Main Stage uses G_m linearization technique to improve linearity

TSMC 40nm Prototype Chip Die Photo



Process Details

- TSMC 40nm
- 6 Metal Stack
- 1 UTM Layer
- Total Area: 1.75mm×2mm

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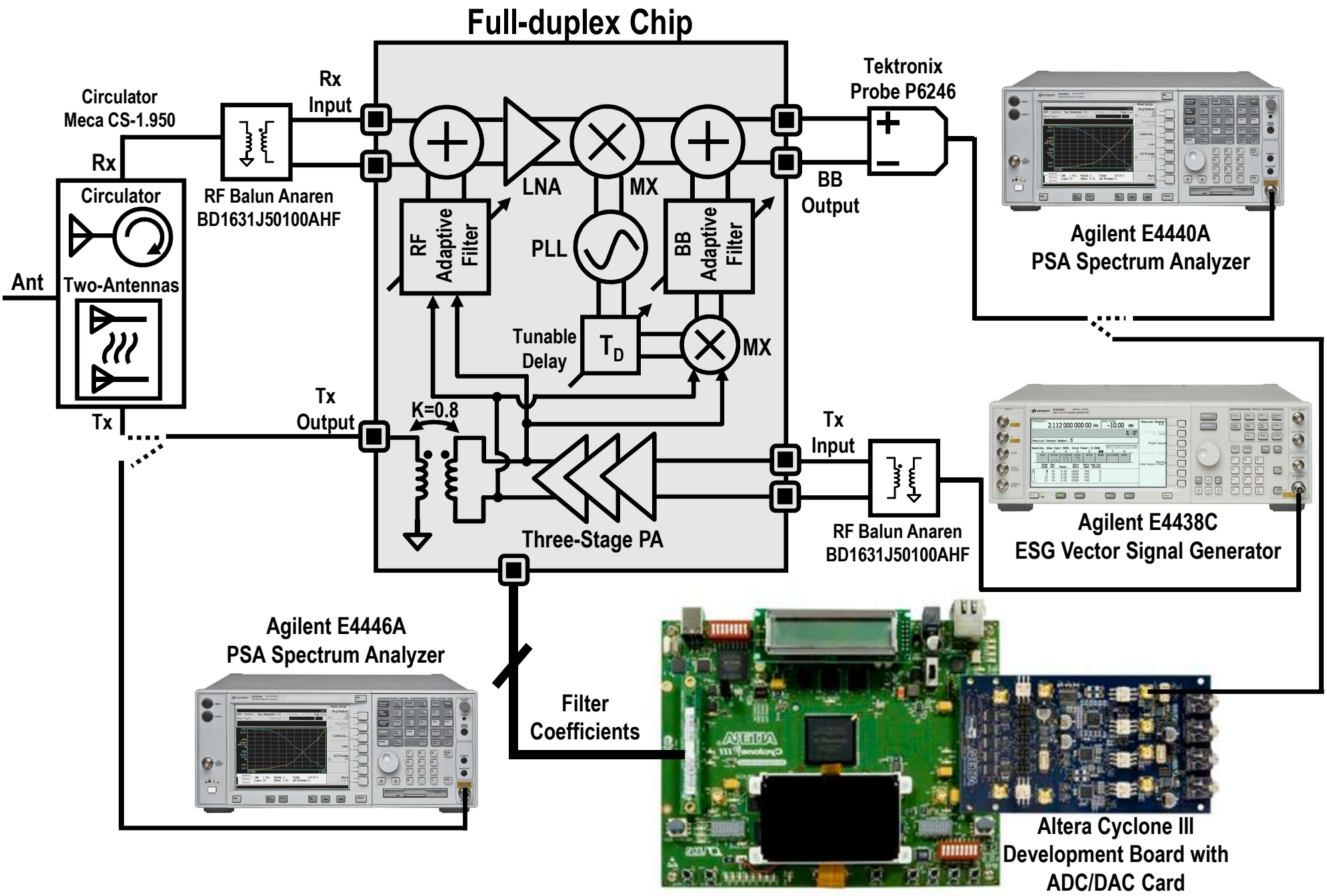
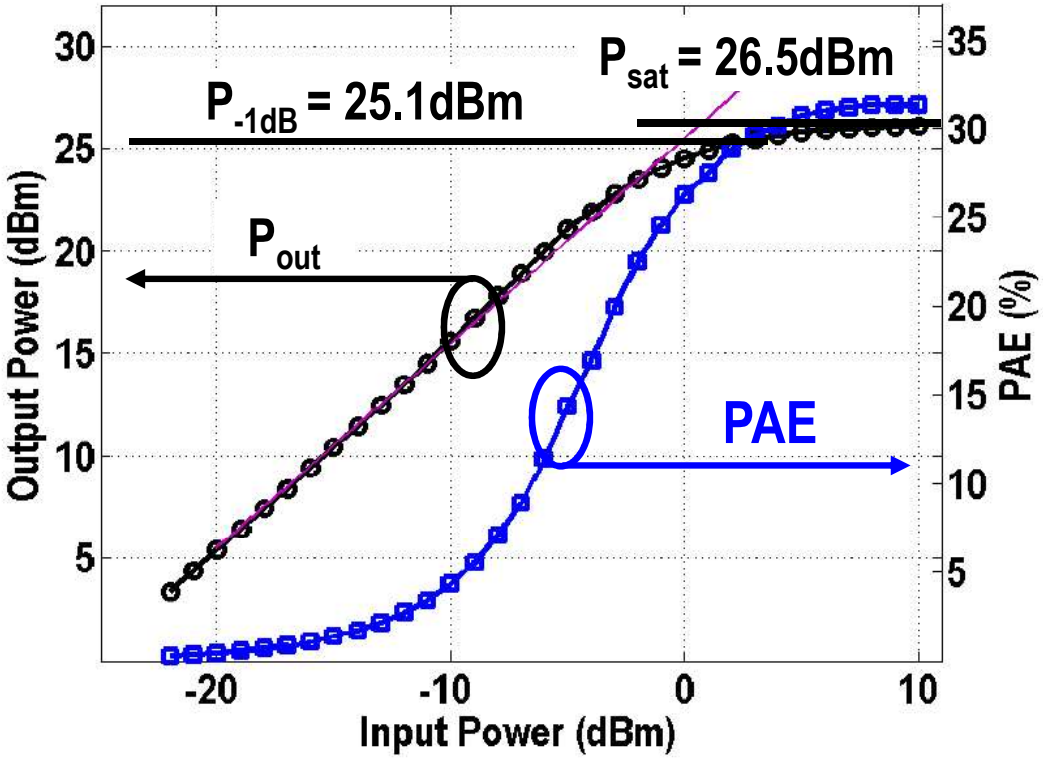
Measurement Setup

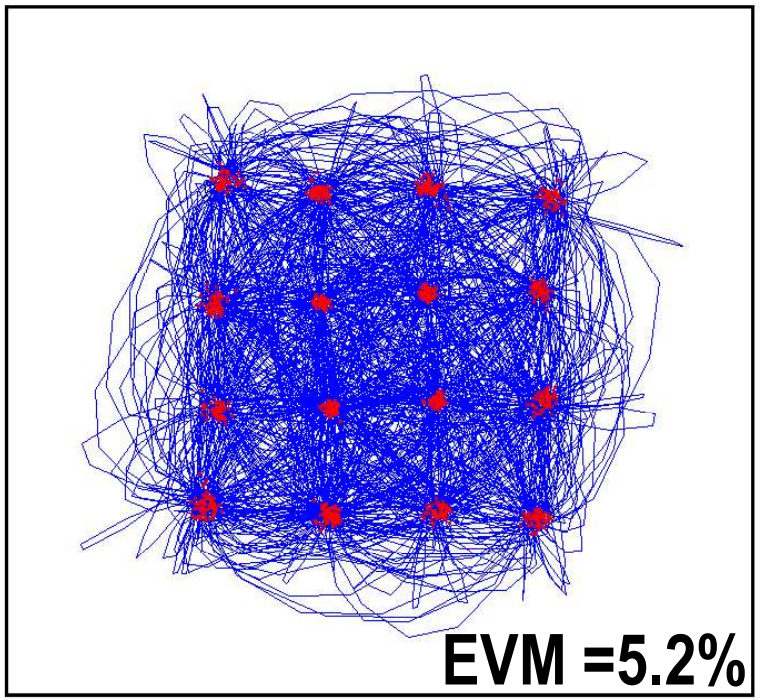


Measured PA Power, EFF and EVM

PA Output Power & Efficiency @ 1.96GHz

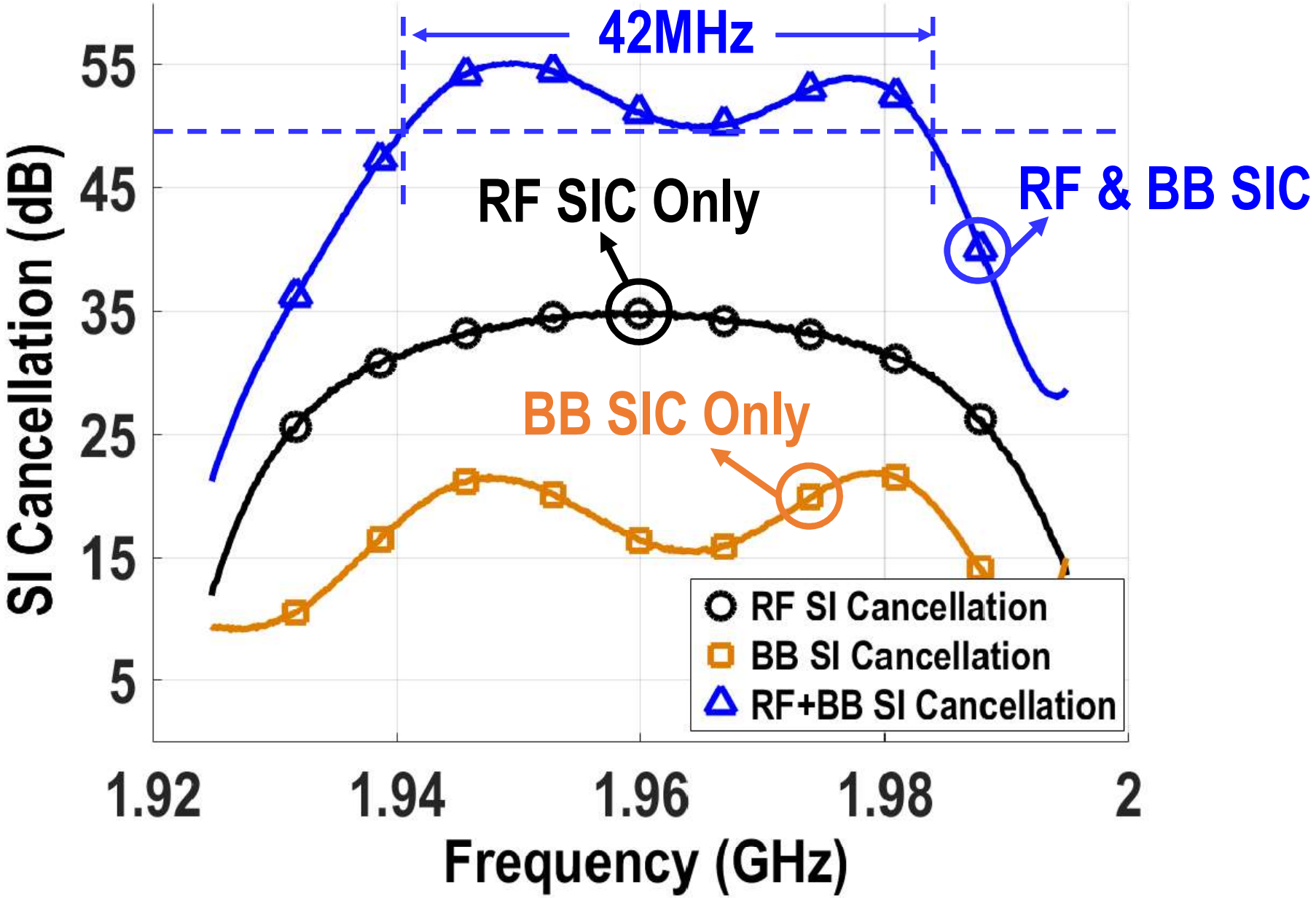


40Mbp/s 20dBm 16QAM Signal @ 1.96GHz

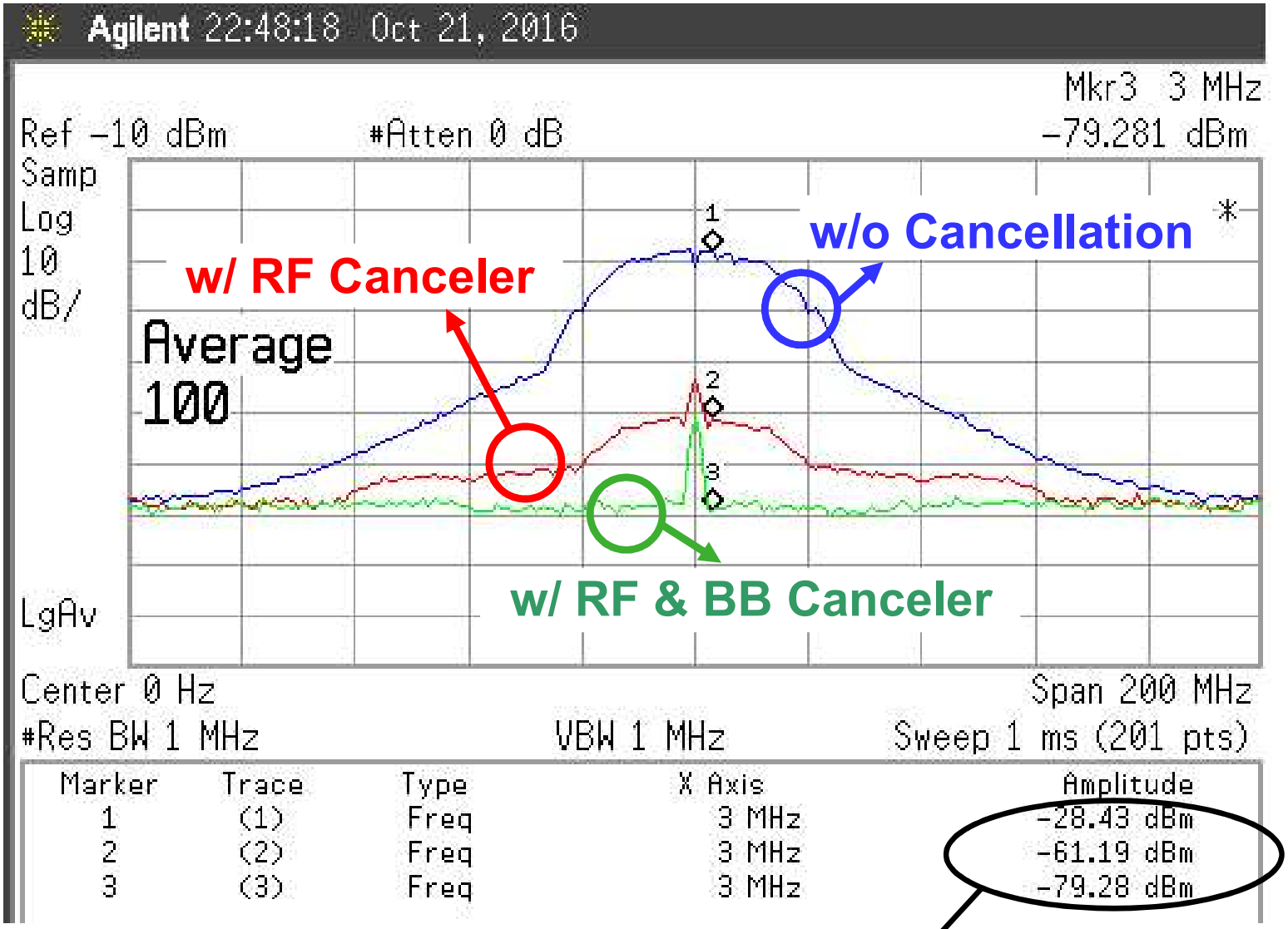


P_{-1dB} = 25.1dBm, P_{sat} = 26.5dBm, Max PAE = 32%

Measured TX Suppression vs. Bandwidth

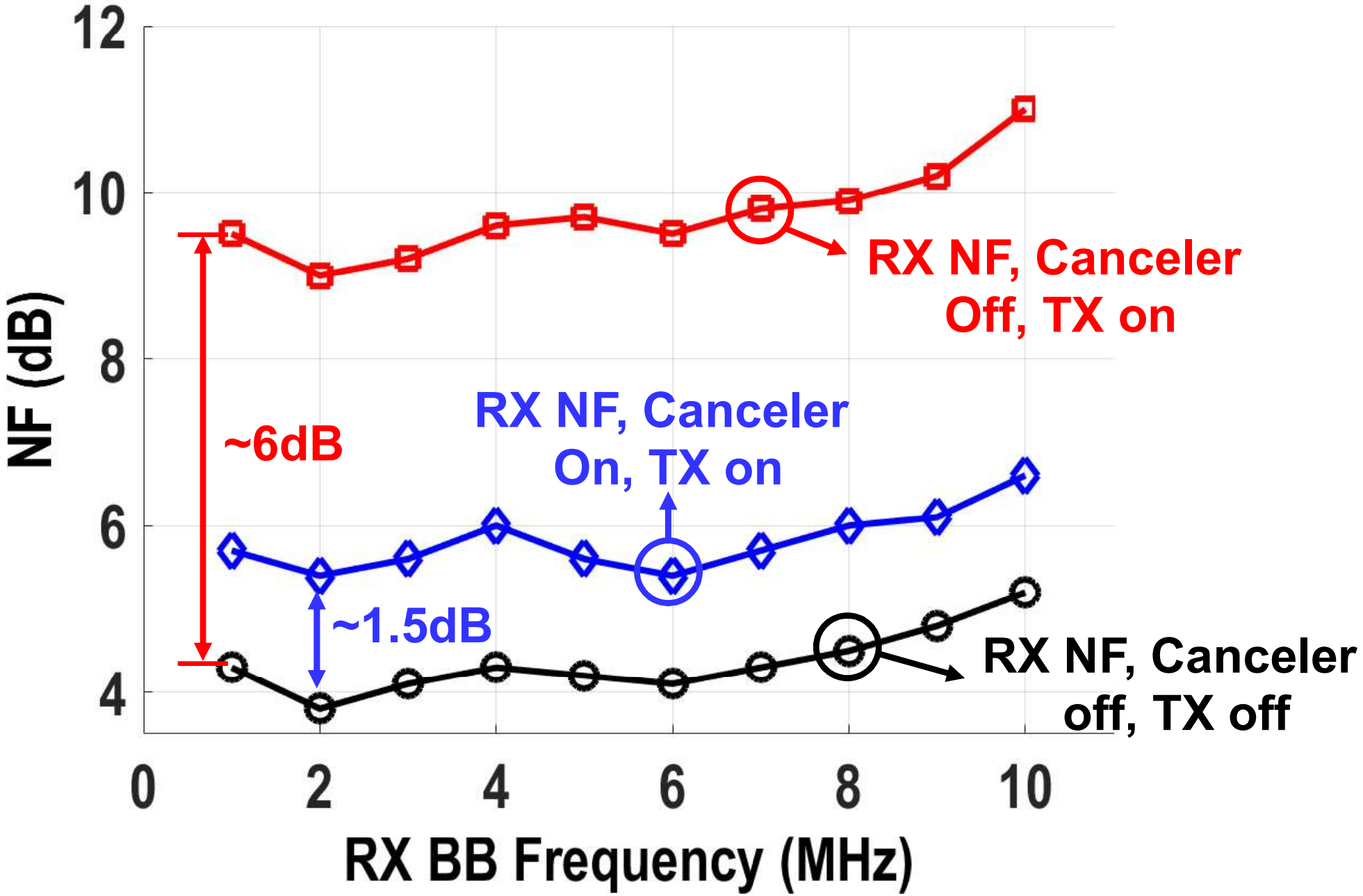


Measured Suppression w/ 40MHz 16 QAM Signal



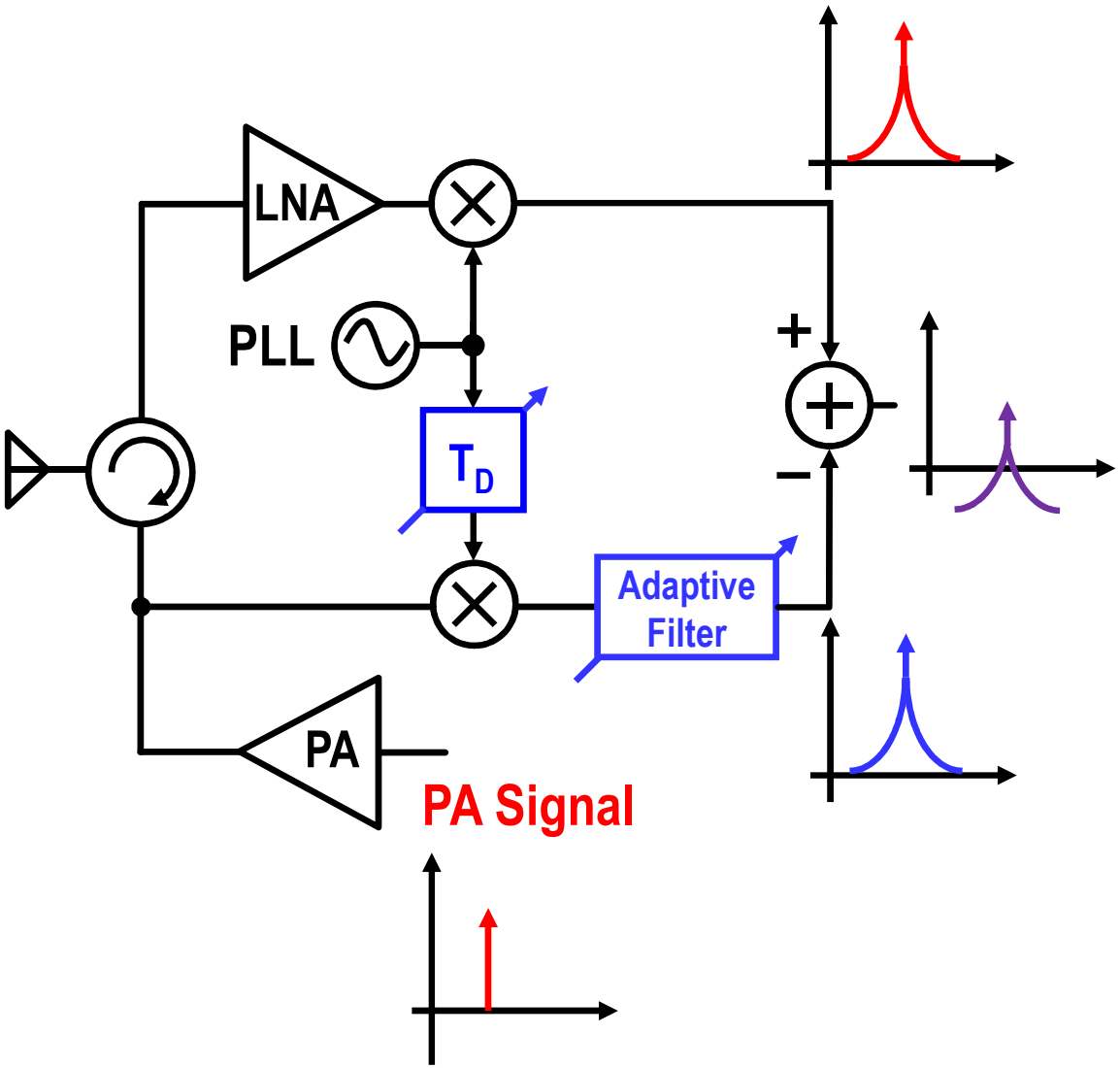
Cancellation = -28.43- (-79.28) = 50.85dB

RX NF w/ and w/o Cancellation

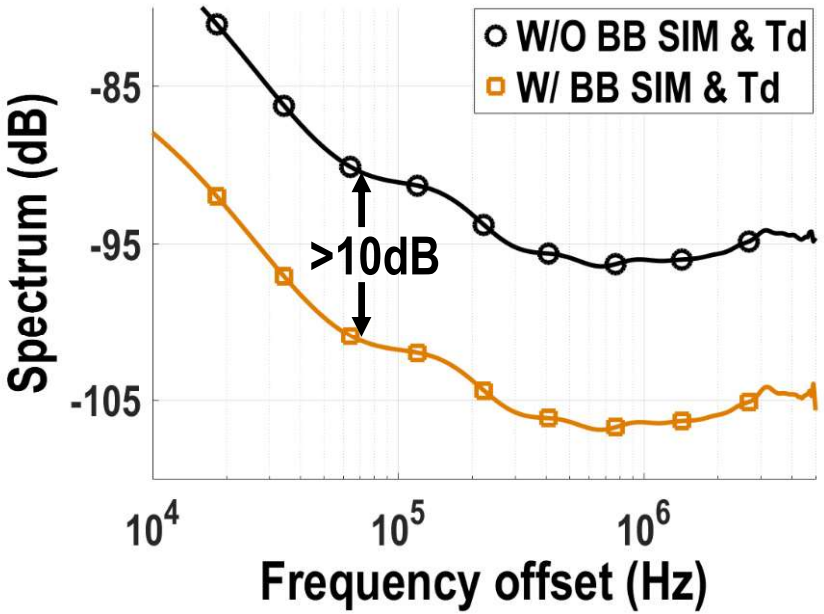


TX SI PN Cancellation

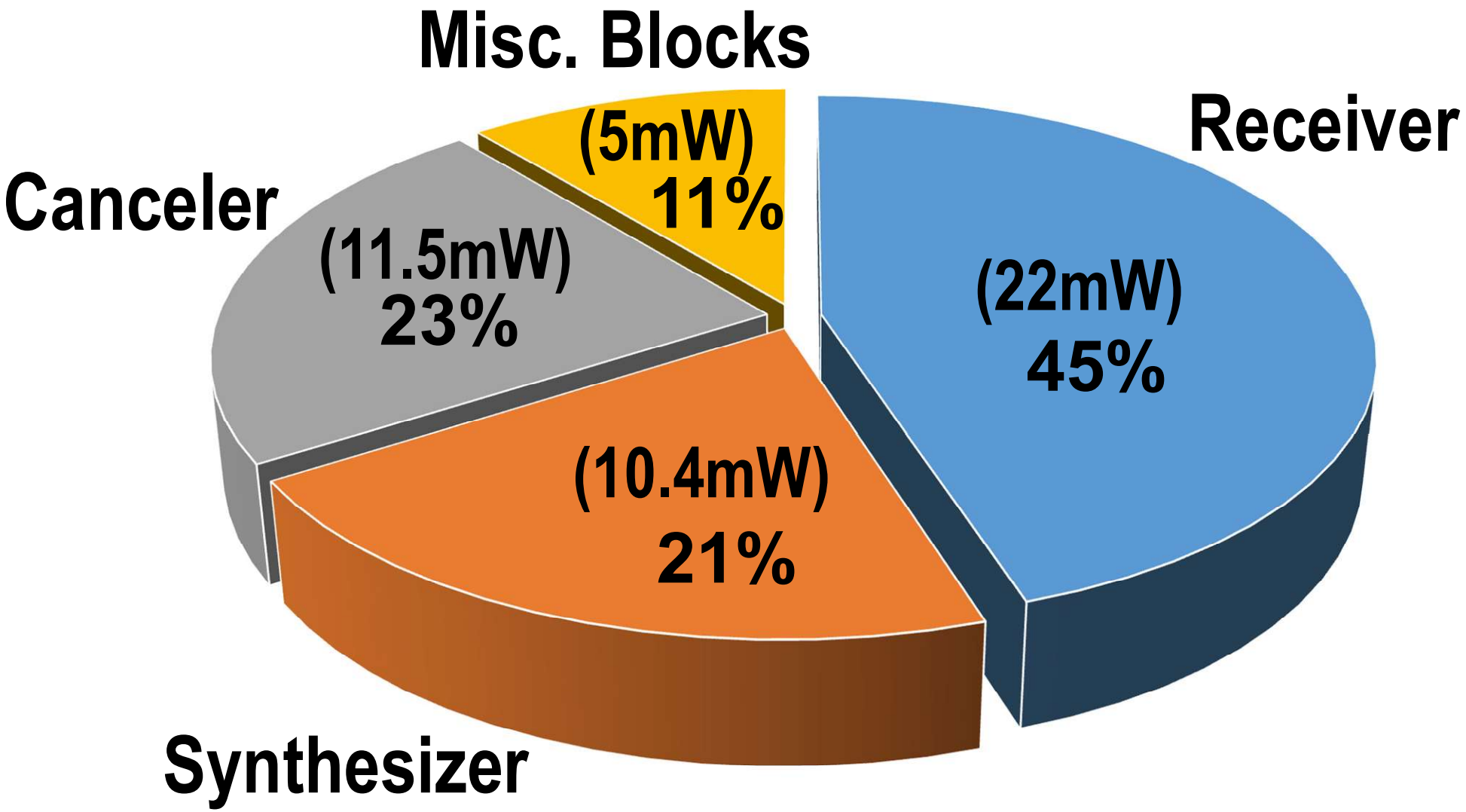
Measurement Setup



Measured Results



System Power Breakdown



Power consumption of the PA is not included.

Comparison Table

		J. Zhou ISSCC' 2015	Van Dan Broek ISSCC' 2015	D. Yang JSSC' 2015	J. Zhou ISSCC' 2016	This Work
Architecture		FD Equalization	VM-Downmixer	Duplexing LNA	Circulator+ BB SIC	Dual-path + Adaptive Filter
Technology		65nm	65nm	65nm	65nm	40nm
RX Frequency (GHz)		0.8-1.4	0.15-3.5	0.1-1.5	0.6-0.8	1.7-2.2
TX_{out}-to-RX_{in} Iso. (dB)		30-50	N/A	N/A	N/A	30-35
Integrated PA		No	Yes	Yes	No	Yes
Integrated PLL		No	No	No	No	Yes
SI Max Suppress. (dB)		N/A	27	33	N/A	***55***
Cancel. BW	**Cancel. (dB)**	20	27	33	42	***50***
	BW (MHz)	15 / 25	16.25	0.3	12	***42***
Canceller Power (mW)		44-91	N/A	N/A	30	***3.5 (RF) +8 (BB)***
SIC NF Degradation (dB)		0.9-1.2	4-6	N/A	5.9	***1.05 (RF)+0.5(BB)***
RF Canceller Area (μm^2)		N/A	N/A	N/A	N/A	203 ×124
BB Canceller Area (μm^2)		N/A	N/A	N/A	N/A	925 ×350
Canceller IIP_3 (dBm)		N/A	N/A	N/A	N/A	36 (RF) / 34.5 (BB)
Canceller P_{-1dB} (dBm)		N/A	N/A	N/A	N/A	27 (RF) / 26.5 (BB)
TX SI PN Suppress. (dB)		N/A	N/A	N/A	N/A	10
Active Area (mm^2)		4.8	2	1.5	1.4	3.5

Conclusion

- **Dual-path SI cancelling architecture is proposed for full-duplex radios.**
- **This SI canceller performance achieves:**
  - **Wideband SIC (50dB >42MHz BW)**
  - **Low power (11.5mW)**
  - **Modest noise figure degradation (1.55dB)**
  - **High Linearity (36dBm/34.5dBm IIP_3)**
- **Feasibility of a highly integrated CMOS full-duplex transceiver operating at 1.7-2.2 GHz has been demonstrated.**

Acknowledgements

- National Science Foundation (1408575)
- CDADIC
- Google Incorporated
- Marvell for chip fabrication
- Advice of Visvesh Sathe and Li Lin