Highly-Integrated CMOS Interface Circuits for SiPM-Based PET Imaging Systems

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***Abstract*–Recent developments in the area of Positron Emission Tomography (PET) detectors using Silicon Photomultipliers (SiPMs) have demonstrated the feasibility of higher resolution PET scanners due to a significant reduction in the detector form factor. The increased detector density requires a proportionally larger number of channels to interface the SiPM array with the backend digital signal processing necessary for eventual image reconstruction. This work presents a CMOS ASIC design for signal reducing readout electronics in support of an 8x8 silicon photomultiplier array. The row/column/diagonal summation circuit significantly reduces the number of required channels, reducing the cost of subsequent digitizing electronics. Current amplifiers are used with a single input from each SiPM cathode. This approach helps to reduce the detector loading, while generating all the necessary row, column and diagonal addressing information. In addition, the single current amplifier used in our Pulse-Positioning architecture facilitates the extraction of pulse timing information. Other components under design at present include a current-mode comparator which enables threshold detection for dark noise current reduction, a transimpedance amplifier and a variable output impedance I/O driver which adapts to a wide range of loading conditions between the ASIC and lines with the off-chip Analog-to-Digital Converters (ADCs).**

I. Introduction

THE recent realization of Silicon Photomultiplier (SiPM) devices as solid-state detectors for Positron Emission Tomography holds the promise of improving image resolution, integrating a significant portion of the interface electronics, and potentially lowering the electronic power consumption. High quantum efficiency, high gain, operation at low bias voltages, insensitivity to magnetic fields, excellent timing resolution, robustness and compactness are some of the advantages offered by these solid-state devices in comparison to the traditional vacuum photomultiplier tubes (PMT) used for low-level light detection. In addition, this technology facilitates the interconnection between the detector and the read-out electronics.

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With respect to readout circuits for SiPM detectors in PET applications, a majority of the circuits have been derived from previous discrete or integrated implementations developed for PMTs [1-3]. In contrast, there have been a number of recent efforts on ASIC's dedicated for SiPM detectors used in PET applications [4-6]. However, a number of challenges exist for highly integrated front-end detectors. Specifically, the reduced size offered by SiPM devices implies a corresponding increase in the detector density, resulting in a proportional rise in the number of channels interfacing a SiPM array with the digital backend. At the University of Washington, the Radiology Department working in conjunction with the Department of Electrical Engineering, has been exploring novel analog and mixed-signal electronic systems to simplify and reduce the required channels between the individual elements in the SiPM array and the backend digital electronics. Our lab has previously reported on novel board-level readout electronics for an 8x8 (SiPM) array featuring row/column summation technique to reduce the hardware requirements for signal processing [7]. The goal now is to implement a monolithic chip for readout ASIC replacing the discrete board [8]. This work describes the design of a high speed current amplifier with a quadruple output stage, core to our CMOS implementation of the frontend readout electronics. One amplifier supplies multiple outputs, implying a minimal loading at the SiPM amplifier interface, further improving speed while reducing power. Specifically, three of the four outputs supply addressing information by performing row, column, and diagonal summation similar to what is done in memory cells. The fourth amplifier output supplies pulse timing information. Thus, the single current amplifier approach allows both timing as well as positioning information used by the Pulse-Positioning architecture. The row/column/diagonal summation circuit approach significantly reduces the number of required channels, reducing the cost of subsequent digitizing electronics. In addition, this approach helps to significantly relax the bandwidth required for each of the address summation channels, thus relaxing the analog-to-digital (ADC) requirements. Additional design work will take place over the coming months to realize the full system for eventually fabricate and interface with the Phase II MiCES FPGA data acquisition [9] boards currently under development at the University of Washington. These components will be realized in a standard-digital 130 nm STMicroelectronics CMOS technology and combined with other features including channel offset calibration and threshold detection circuitry to improve noise immunity. Our program seeks to eventually

integrate the readout electronics either in the same package as the SiPM devices or on the same silicon substrate. By integrating all the electronics in the same package or silicon die, the SiPM could potentially produce a digital code which represents both location and intensity of a detected photon event.

This paper will first discuss a system level design of the front end ASIC. This is followed by a section on the high speed current amplifier. Lastly, a brief summary of the ideas on the current comparator and the line drivers has been provided as part of the future work in this project.

II. ASIC ARCHITECTURE

At present, our front-end readout electronics is situated in close proximity to the SiPM array. A differential interface then runs from the output of the front-end amplifiers to the input of a set of ADCs and the subsequent digital signal processing chip. As such, a significant motivation exists to reduce the number of channels and the corresponding cabling between the front and back end. This ASIC is being designed with the intent of reducing the number of channels between the SiPM array and the backend digital signal processing. A row/column/diagonal summation architecture [8], shown in Fig. 1, helps to reduce the number of channels between the front and backend while producing pulse timing information.

Some of the proposed electronics between SiPM and line driver are shown in Fig.2. A low input impedance, high-output impedance current amplifier interfaces the SiPM device and produces a current which is shared with other SiPM devices along a row, column, or diagonal line. The current amplifier is designed to produce the lowest input impedance possible to improve the bandwidth at the SiPM-Current Amplifier interface. Each amplifier has an additional high-speed current output that supplies a common timing signal.

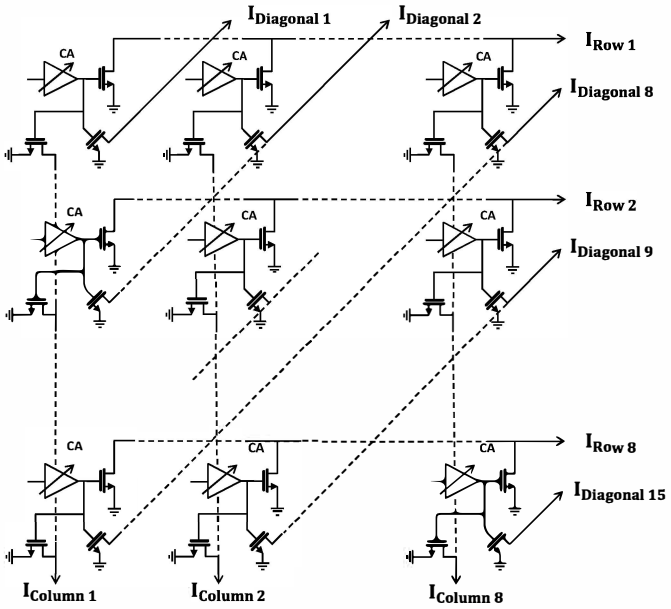

Fig. 1. Row-Column-Diagonal Pulse Positioning Architecture

A current comparator is used in a parallel with the main signal path and either enables or disables the output of the current amplifier. This comparator output goes high, and enables the current amplifier when the SiPM output reaches a predetermined threshold. This is done to minimize the accumulation of "dark current" noise produced by the SiPM devices along a single row, column, or diagonal line. Compared to a single-channel readout of an individual SiPM device, the accumulated noise associated with combining numerous detectors on a similar row line, for example, can increase the possibility of a detecting a false event. A transimpedance amplifier acts as the interface between the summing lines and the off-chip ADC and FPGA by converting the single-ended current signal to a differential voltage. Analog line drivers are used to tune the channel output impedance over a range of loading conditions (50Ω - 200Ω) presented by a variation in the differential driver lengths, shape, etc, all of which influence the load impedance presented to the ASIC output.

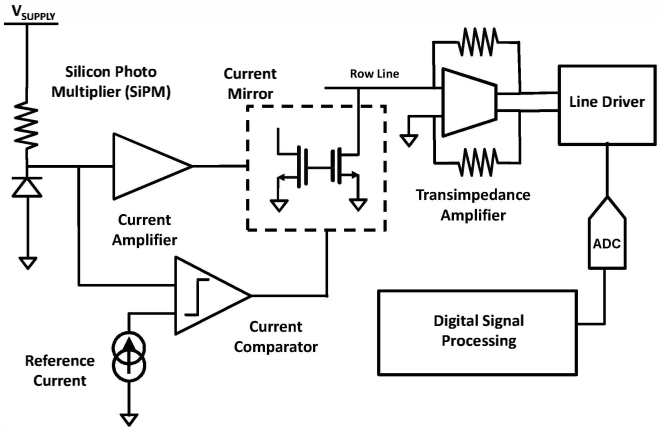

Fig. 2. Schematic Architecture of the Analog Front End Channel

III. CURRENT AMPLIFIER

As stated in the last section, use of current amplifiers is motivated by the need to present low input impedance to the SiPM current output, and the desire to maximize the bandwidth at the SiPM-amplifier interface. The current amplifier, shown in Fig. 3, consists of a transimpedance amplifier followed by a transconductance stage, M4 [10].

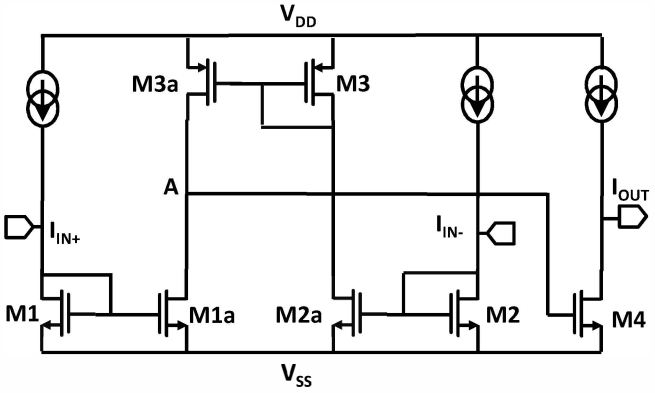

Fig. 3. Current Amplifier Topology

The applied small-signal differential input current is converted into a voltage mode signal through the use of a transimpedance stage using devices M1a and M3a. The transconductance stage then converts this voltage into a current signal at the output of the amplifier. A small-signal analysis of the current amplifier reveals that the open loop gain is given by,

$$\boldsymbol{A = \frac{g_{m4}}{g_{ds1a} + g_{ds3a}}}$$

where g_{m4}, gds_{1a}, and gds_{3a}, represent the transconductance of M4, and the output conductance of M1a and M3a, respectively. The current gain is increased by increasing the impedance at node A, which can be done by employing cascode stages for the input and PMOS stages. The current-gain is also increased by increasing g_{m4} of the output transistor. Therefore, one observes the classic tradeoff between power consumption, die area, and gain.

A transistor schematic of the current amplifier design was realized using models from a 130nm PDK. The closed-loop implementation of the amplifier using a feedback and load resistor is shown in fig. 3. The closed loop gain is determined by the ratio of resistors values, thus facilitating the realization of variable gain by modulating the value of R_L which is easily done by realizing a switched-resistor array network. Amplifier noise, linearity and bandwidth were optimized to meet the desired performance given in [8]. A simulated input impedance of 70 Ω with a bandwidth of 500 MHz was obtained by doing a tradeoff between the open-loop gain and the dc power consumption.

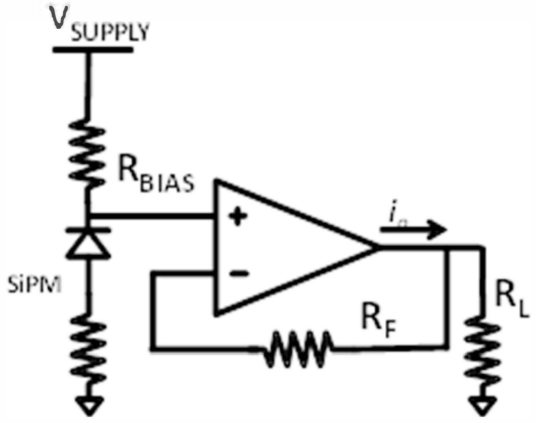

Fig. 4. Closed-Loop Operation of Current Amplifier

IV. Future Work

Additional design work will take place over the coming months to realize the full system consisting of the current comparator and the analog line drivers to eventually fabricate a chip which provides an interface with the Phase II MiCES FPGA board. The current comparator design is challenging as it needs to be fast relative to the leading edge of a SiPM current pulse event. High-speed low-input impedance current comparator architectures with positive feedback and slew rate enhancement circuits [11] are now being explored to minimize the loss of SiPM pulse energy while allowing threshold detection to remove unwanted dark current noise events. .

Differential lines are used as the interface between the ASIC and the off-chip ADC in the Phase II MiCES FPGA board. To minimize the possibility of reflections due to a load mismatch, the source and load impedances of the cable must be equal to the characteristic impedance of the cable. An adaptive line driver [12] will tune the ASIC output impedance to match the impedance of the next stage. This has the primary advantage of adapting the ASIC output impedance over PVT, and variety of cable loading characteristics.

V. Conclusion

This work presents the initial design of a new front-end readout ASIC dedicated to PET imaging systems which facilitates the integration of the SiPM with the front-end electronics. The proposed pulse-positioning architecture reduces the number of channels between the SiPM array and the backend signal processing. Additional design work will take place over the coming months to realize the full system to eventually fabricate the front-end SiPM interface electronics with data acquisition boards which are currently under development at the University of Washington. Our program seeks to eventually integrate the readout electronics either in the same package (SIP) with the SiPM devices, or on the same silicon substrate, allowing sophisticated calibration methods to

address mismatch, process variation and non-idealities in the readout electronics

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