A 12b 200MS/s Frequency Scalable Zero-Crossing Based Pipelined ADC in 55nm CMOS

Soon-Kyun Shin[1,2], Jacques C. Rudell[1], Denis C. Daly[2], Carlos E. Muñoz[2], Dong-Young Chang[2], Kush Gulati[2], Hae-Seung Lee[3], and Matthew Z. Straayer[2]

[1]Department of Electrical Engineering, University of Washington, Seattle, WA, USA
[2]Cambridge Analog Technologies, Inc., Chelmsford, MA, USA
[3]Massachusetts Institute of Technology, Cambridge, MA, USA

***Abstract*- A 12-bit 200MS/s zero-crossing based pipeline ADC is presented. A coarse phase followed by a level-shifted fine phase is employed for higher accuracy. To enable high frequency operation, sub-ADC flash comparators are strobed immediately after the coarse phase. The ADC occupies 0.276mm^2 in 55nm CMOS and dissipates 28.5mW. 62.5dB SNDR and 78.6dBc SFDR with a 99.6MHz input signal at 200MS/s are achieved for a FOM of 131fJ/step. The reference buffer, bias circuitry, and digital error correction circuits are all implemented on chip.**

I. INTRODUCTION

As technology scaling continues, there are increasing demands for higher speed and high resolution analog-to-digital converters in telecommunication systems and battery-powered mobile applications. In order to integrate a large system-on-a-chip (SoCs), power consumption and area are limiting factors. Zero-crossing based circuits (ZCBC) have been introduced as a power-efficient alternative to op-amps for achieving precise gain in switched capacitor circuits [1-4]. The largest source of nonlinearity in ZCBCs is the nonlinearity of the ramp caused by finite output resistance of the current sources. Previously, a dual ramp approach was proposed which improves the ZCBC linearity [5]. To improve speed, a time-interleaved ADC with four single channel ADCs is used with ZCBC [6]. In this paper, we present several techniques to improve the speed, linearity, and frequency scaling.

II. ADC ARCHITECTURE

The functional block diagram of the proposed ZCBC pipelined ADC is shown in Fig. 1. The ADC consists of 4 stages and a final 4 bit sub-ADC. The first stage is composed of a 9-level sub-ADC and MDAC with gain of 4. The second stage and the third stage are scaled down by a factor of 2 from the first stage and the second stage, respectively. The fourth stage is identical to the third stage. Redundancy for over-range protection is used to relax offset constraints in both the bit decision comparators and the residue amplification. The reference buffer, bias circuitry, and digital error correction circuits are all implemented on chip.

One of the key challenges in high speed pipelined ADC design is that the time required for the bit decision comparators to evaluate occupies a large percentage of the clock period, resulting in a reduction of time for charge transfer. To address this problem, the dual ramp is leveraged, whereby the sub-ADC flash comparators are strobed immediately after the coarse phase rather than waiting until the fine phase is completed. Thus, the time required for the bit decision comparators to evaluate does not result in a reduction of charge transfer time. For the presented ADC, this approach allows for an increased charge transfer time of approximately 20%.

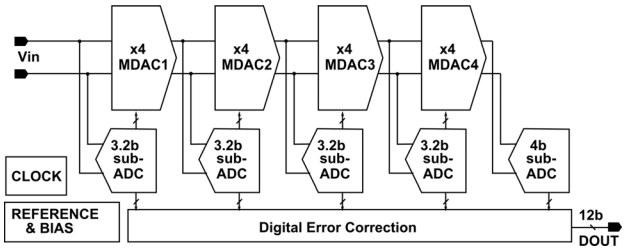


Fig. 1.Block diagram of the proposed pipelined ADC.

In this work, we also improve the dual ramp technique by sampling the coarse output voltage across a level shifting capacitor. The level shifting capacitor is placed in series with the current source during the fine phase [7]. This largely removes the voltage variation across the fine phase current source, greatly improving the linearity, even at high sampling rates. There is virtually no penalty in speed or power consumption, and the additional die area for the level shifting capacitor is very modest. An analogous technique was introduced for op-amp based circuits to reduce the finite gain effects [8]. Finally, the zero-crossing ADC is designed to be able to operate over a very broad range of sampling frequencies; at low frequencies the zero-crossing detector and ramp currents are shut down after the appropriate zero-crossing is reached. At high frequencies, bias currents are increased proportionately in order to enable faster operation.

III. CIRCUIT IMPLEMENTATION

A. ZCBC Pipeline Stage

A simplified schematic of a ZCBC pipelined ADC stage is shown in Fig. 2. Each stage has switched-capacitor circuits with a sub-ADC, a zero-crossing detector (ZCD), coarse and fine current sources, level shifting capacitors C_{LS}, and amplification capacitors C_a. A timing diagram is shown in Fig.

978-1-4673-1556-2/12/$31.00@2012 IEEE

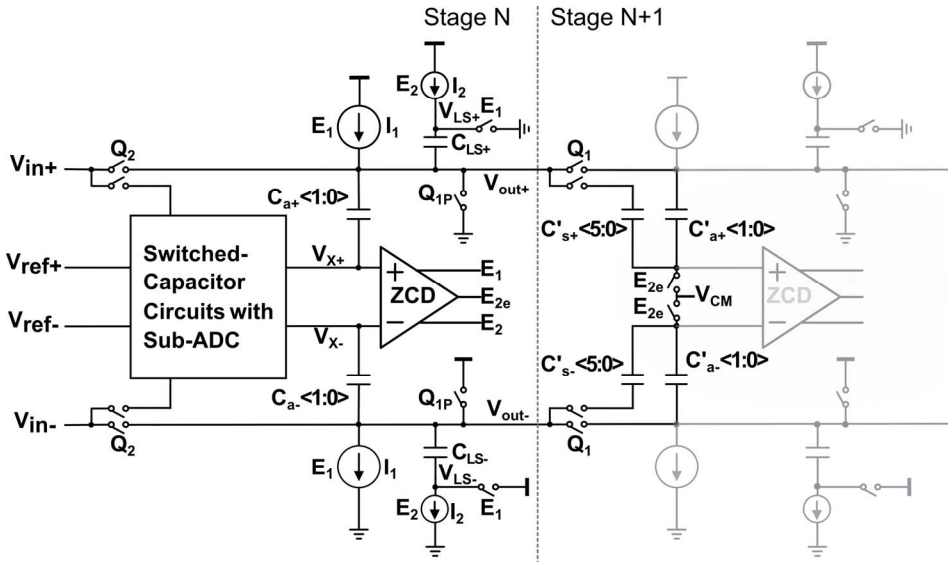
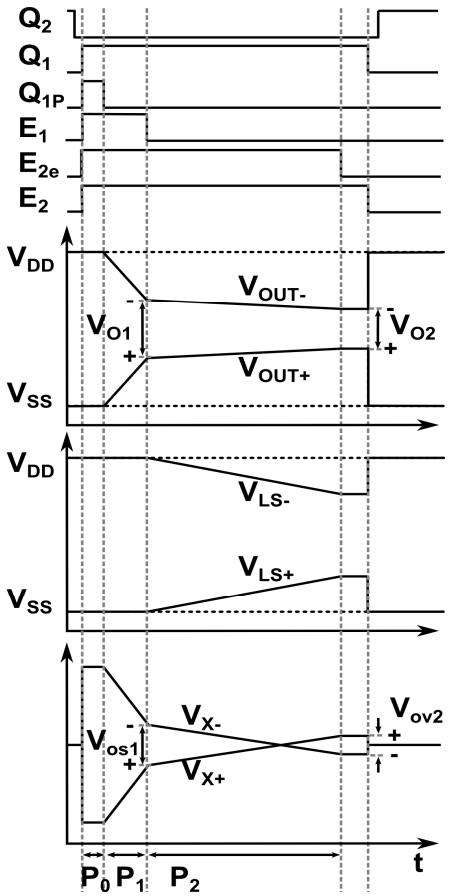


Fig. 2. Simplified schematic of a ZCBC pipeline ADC stage.

3. The input voltage is sampled during the sampling phase (Q_2). In the preset phase (P_0), a short preset signal Q_{1P} sets V_{OUT+} to V_{SS} and V_{OUT-} to V_{DD}. This ensures that the differential input to ZCD starts from negative at the start of the coarse phase (P_1). At the beginning of preset phase, E_1 and E_2 also turn on in order to reduce transient effects in the transition of the coarse phase and the fine phase. After Q_{1P} turns off, the coarse phase begins. The E_1 controls the coarse phase and coarse current I_1 charges V_{OUT+} and discharges V_{OUT-} at a fast rate until V_{x+} and V_{x-} cross the offset voltage V_{OS1}. At this point, next stage's sub-ADC strobes output voltage V_{O1} and begins to make a decision. E_1 also sets V_{LS+} to V_{SS} and V_{LS-} to V_{DD} until the coarse phase ends. After the coarse phase, E_1 disconnects V_{LS+} from V_{SS} and V_{LS-} from V_{DD} so the fine phase (P_2) current I_2 through level shifting capacitor C_{LS} begin to charge V_{OUT+} and discharge V_{OUT-} at a slow rate. When V_{x+} crosses V_{x-}, the sampling signal E_{2e} falls to open the sampling switches. The output voltage V_{O2} is accurately sampled on the next stage capacitors $C`_S$ and $C`_a$ at that instant. Because the ZCD has a finite delay, I_2 turns off shortly after V_{x+} crosses the V_{x-}, so this delay combined with the ramp rate causes a relatively constant overshoot (V_{OV2}). The correlated level shifting described in Section C greatly reduces variation of this overshoot and its associated nonlinearities.

B. Sub-ADC

The sub-ADC consists of reference resistor ladders with offset voltage and eight switched-capacitor comparators for a nine level (3.2bit) flash sub-ADC. The availability of distinct ramp phases makes it natural to trigger the sub-ADC comparators at the end of the first ramp phase allowing more time for the sub-ADC thus ensuring overall faster ADC conversion. The timing diagram of the sub-ADC N+1 with stage N and stage N+1 is shown in Fig. 4. After the coarse phase completes, the sub-ADC strobes the V_{O1} (T_0) and begins to make a decision (T_1). However, there is an offset voltage



3. Timing diagram of charge transfer phase.

between the coarse phase output voltage V_{O1} on which the sub-ADC comparators are strobed versus the final output voltage. Note that variation of the offset voltage V_{O2-1} between V_{O1} and V_{O2} is small compared to the sub-ADC resolution

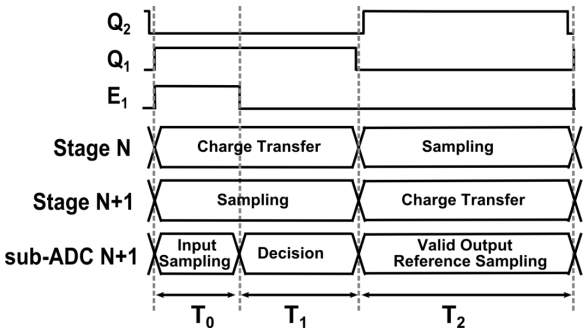


Fig. 4.Timing diagram of sub-ADC.

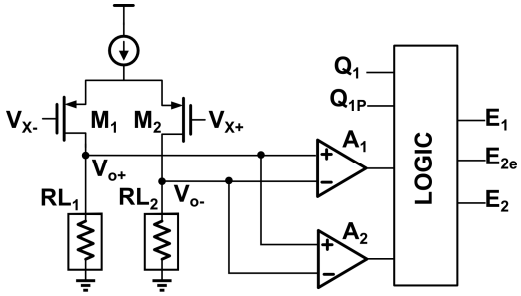


Fig.5. Simplified schematic of zero-crossing detector.

because the zero-crossing decisions at the end of each phase are relatively precise. This constant offset voltage is canceled out by subtracting a systematic offset equal to $V_{O2\text{-}1}$ in the sub-ADC comparators to prevent the correction range from being used to cover the offset. When stage N+1 is in charge transfer phase (T_2), the sub-ADC N+1's output is valid and it also samples reference voltage at the same time for next bit decision.

C. Correlated Level Shifting

A split-CLS technique is introduced [8] to create high effective gain but it uses a linear settling with feedback. However, ZCBC is inherently open-loop, so there are no constraints with respect to feedback stability. In the coarse phase, capacitors C_{LS}, as shown in Fig. 2, sample the coarse output voltage V_{O1} against V_{SS} and V_{DD} for the positive and negative polarities, respectively. Then in the fine phase, C_{LS} appear in series with the fine current sources I_2, which effectively level shifts the fine phase current source outputs. At the beginning of the fine phase, V_{LS+} and V_{LS-} always start from V_{SS} and V_{DD} respectively, regardless of the output voltage. This feature gives the fine current sources maximal headroom for a given supply voltage, allowing for simple cascode implementation. In addition to the benefit of operating the current source in a very comfortable region, the variation in the voltage seen by the fine current source is significantly reduced compared to a single ramp architecture. To explain, the small output voltage error from the coarse phase decision is approximately equal to the entire voltage variation seen by the fine ramp current sources. Since the precision of the coarse phase is greater than 7-8 bits, overall the variation in the current source output voltage is significantly less than the entire output residue range. Therefore, the linearity of the ZCBC is greatly improved even at high speeds.

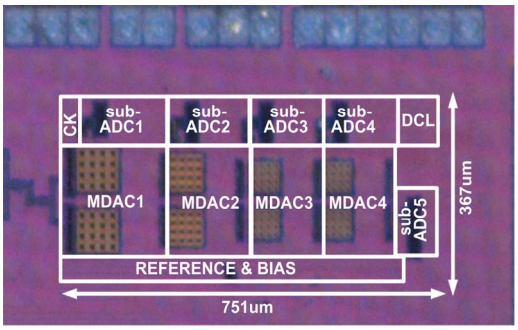


Fig. 6. Chip micrograph.

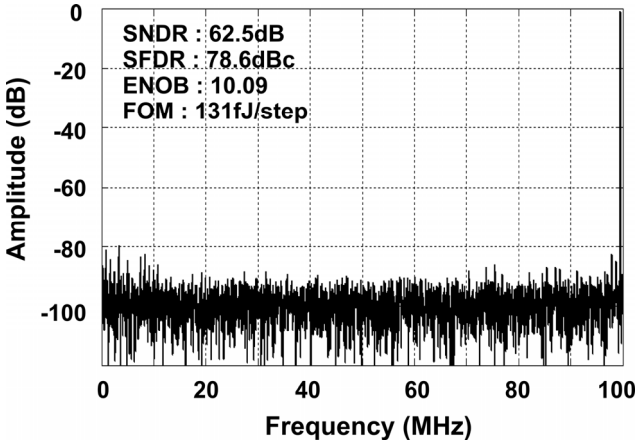


Fig. 7. Measured FFT spectrum with input frequency of 99.6MHz.

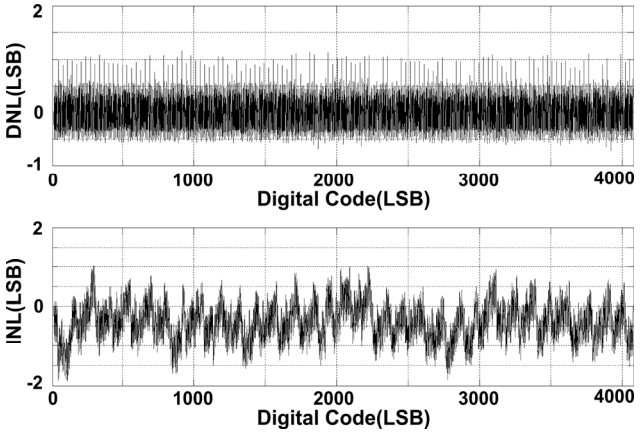


Fig. 8. Measured DNL and INL.

D. Zero-Crossing Detector

The ZCD indicates the crossing of V_{x+} and V_{x-} at the end of the fine phase, and E_{2e} turns off the sampling switch in the following stage which completes the charge transfer. A simplified schematic of the ZCD is shown in Fig. 5. It is composed of a main pre-amplifier (M_1, M_2, RL_1, and RL_2), a coarse threshold detector A_1 and a fine threshold detector A_2,

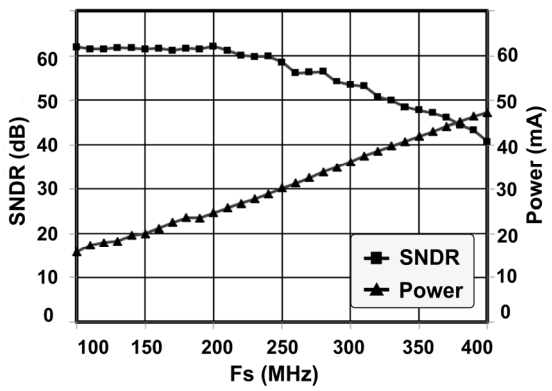


Fig. 9. Measured results of SNDR and power consumption versus sampling frequency (fin=99.6MHz).

TABLE I
PERFORMANCE SUMMARY

Technology	55nm CMOS 1-Poly 6-Metal
Supply voltage	1.1V
Resolution	12b
Conversion rate	200MS/s
Input voltage Range	$2V_{p-p}$ (differential)
Die area	$0.276mm^2$
Power consumption	28.5mW
DNL	+1.16 / -0.72LSB
INL	+1.02 / -1.89LSB
SFDR	76.1dBc (fin=34.9MHz) 78.6dBc (fin=99.6MHz)
SNDR	63.7dB (fin=34.9MHz) 62.5dB (fin=99.6MHz)
FOM	114fJ/step (fin=34.9MHz) 131fJ/step (fin=99.6MHz)

and simple digital logic for creating the appropriate timing signals. The power consumption of the core ZCBC is proportional to the sampling rate due to the dynamic operation [3], with the exception of the bias circuitry which consumes a small amount of constant power. For high-speed operation and sampling frequency scalability, the ramp currents I_1 and I_2, as well as the ZCD bias current are designed to track the primary current generated from a bias control circuitry. These bias and ramp currents are then increased proportionally to the sampling rate. This ensures that the ramp slope is sufficiently fast such that it can cover the entire desired residue range in the available time and the ZCD power consumption is optimal at a given sampling rate from a bandwidth and noise perspective.

IV. MEASURED RESULTS

The proposed frequency-scalable ZCBC pipelined ADC was fabricated in a 55nm CMOS process. The active die area of the ADC is $0.276mm^2$ as shown in Fig. 6. The measured spectrum of the ADC with input frequency of 99.6MHz at 200MS/s is shown in Fig. 7. DNL and INL are +1.16/-0.72LSB and +1.02/-1.89LSB as shown in Fig. 8, respectively. Both the DNL and the INL are limited by much larger-than-expected random offset in the last stage's flash comparators, which also translates to an increased noise floor. At 200MS/s with a 34.9MHz input frequency, the SNDR is 63.7dB (10.29 ENOB), and the SFDR is 76.1dBc. With a 99.6MHz input tone, the SNDR is 62.5dB (10.09 ENOB), and the SFDR is 78.6dBc. Table I shows the performance summary. The total ADC power consumption including the on-chip reference buffer is 28.5mW, resulting in 114fJ/step and 131fJ/step FOM with input frequency of 34.9MHz and 99.6MHz respectively. The measured SNDR and power consumption versus sampling frequency with a 99.6MHz input frequency are shown in Fig. 9. Note that the SNDR is flat for a wide range of sampling rates before degrading gradually as the sampling frequency increases above the 200MS/s design target. The SNDR remains above 40dB even at 400MS/s.

V. CONCLUSION

The frequency-scalable ZCBC pipelined ADC has been presented. The ADC exploits a sub-ADC decision after the coarse phase to maximize charge transfer time. A level-shifted fine phase current source is also adopted for higher accuracy and high speed operation. The ADC includes all necessary ancillary circuits including bias circuitry, a reference buffer, and digital error correction logic. With the ramp rate and bias current tracking the sampling rate, the ADC remains functional at frequencies well over the maximum target frequency and the performance degrades gradually. Typically, op-amp based ADC performance degrades catastrophically if the circuit is clocked significantly beyond the target sampling rate. In contrast, zero-crossing based circuits allow tunability to a much broader range of sampling rate. Similar to digital circuits, the power consumption is nearly proportional to the sampling frequency.

REFERENCES

[1] L. Brooks and H.-S. Lee, "A zero-crossing-based 8b 200MS/s pipelined ADC," in *IEEE Int'l Solid-State Circ. Conf. Dig. Tech. Papers*, Feb. 2007, pp.460-461.

[2] S.-K. Shin et. Al., "A fully differential zero-crossing-based 1.2V 10b 26MS/s pipelined ADC in 65nm CMOS," in *IEEE Symp. on VLSI Circ. Dig. Tech. Papers*, Jun. 2008, pp.218-219.

[3] L. Brooks and H.-S. Lee, "A 12b 50MS/s fully differential zero-crossing based ADC without CMFB," in *IEEE Int'l Solid-State Circ. Conf. Dig. Tech. Papers*, Feb. 2009, pp.166-167.

[4] J. Chu, L. Brooks, and H.-S. Lee "A zero-crossing based 12b 100MS/s pipelined ADC with decision boundary gap estimation calibration," in *IEEE Symp. on VLSI Circ. Dig. Tech. Papers*, Jun. 2010, pp.237-238.

[5] S. Lee, A. Chandrakasan, and H.-S. Lee, "A 12b 5-to-50MS/s 0.5-to-1V voltage scalable zero-crossing based pipelined ADC," in *Proc. European Solid-State Circuits Conf.*, 2011, pp.355-358.

[6] J. Chu and H.-S. Lee, "A 450 MS/s 10-bit time-interleaved zero-crossing based ADC," in *Proc.IEEE Custom Integrated Circuits Conf.(CICC),* 2011, pp.1-4.

[7] M. Guyton, "A low-voltage zero-crossing-based delta-sigma analog-to-digital converter," Ph.D. dissertation, Massachusetts Institute of Technology, 2010.

[8] B. Hershberg, S. Weaver, and U. Moon, "Design of a split-CLS pipelined ADC with full signal swing using an accurate but fractional signal swing opamp," *IEEE J. Solid-State Circuits*, vol.45, pp.2623-2633, Dec., 2010.