

# A CMOS ASIC Design for SiPM Arrays

Samrat Dey<sup>1</sup>, *Student Member, IEEE*, Lushon Banks<sup>1</sup>, *Student Member IEEE*, Shaw-Pin Chen<sup>1</sup>, *Student Member IEEE*, Wenbin Xu<sup>1</sup>, *Student Member IEEE*, Thomas K. Lewellen<sup>2</sup>, *Fellow IEEE*, Robert S. Miyaoka<sup>2</sup>, *Senior Member IEEE*, and Jacques C. Rudell<sup>1</sup>, *Senior Member, IEEE*

**Abstract**—Our lab has previously reported on novel board-level readout electronics for an 8x8 silicon photomultiplier (SiPM) array featuring row/column summation technique to reduce the hardware requirements for signal processing. We are taking the next step by implementing a monolithic CMOS chip which is based on the row-column architecture. In addition, this paper explores the option of using diagonal summation as well as calibration to compensate for temperature and process variations. Further description of a timing pickoff signal which aligns all of the positioning (spatial channels) pulses in the array is described. The ASIC design is targeted to be scalable with the detector size and flexible to accommodate detectors from different vendors. This paper focuses on circuit implementation issues associated with the design of the ASIC to interface our Phase II MiCES FPGA board with a SiPM array. Moreover, a discussion is provided for strategies to eventually integrate all the analog and mixed-signal electronics with the SiPM, on either a single-silicon substrate or multi-chip module (MCM).

## I. INTRODUCTION

RECENT developments in the area of Positron Emission Tomography (PET) detectors using Silicon Photomultipliers (SiPMs) have demonstrated the feasibility of miniaturizing PET scanners. A smaller detector size implies the density of the detector array will increase significantly, leading to higher resolution PET images. However, while an increase in detector density leads to improved scanner performance, a significantly higher number of channels are required to interface the SiPM array to backend digital signal processing necessary for eventual image reconstruction. At the University of Washington, the Radiology Department working in conjunction with the Department of Electrical Engineering has been exploring novel analog and mixed-signal electronic systems to simplify and reduce the required channels between the individual elements in the SiPM array and the backend digital electronics. Specifically, we are exploring a row-column-diagonal decoding architecture that is analogous to decoding methods used in digital memory arrays. For an  $N$  by  $N$  array, the number of required channels would be  $N^2$  if each channel were read individually. However, our technique

would reduce the number of channels by a factor of  $N$ . If only row-column decoding were used, the number of channels becomes  $2N$ , while the addition of a diagonal decoding channel results in  $4N-1$  channels. The use of row-column or row-column-diagonal summing depends on the type of detector module being decoded and what is needed for extracting the required information for event positioning. While the row-column-diagonal decoder facilitates information about the position of a detected event, an additional, single high-speed channel will be used to extract a timing pickoff signal for all the elements in the SiPM array. This approach to decoding detectors in a SiPM array significantly reduces the number of required ADCs necessary to interface the digital signal processing electronics. Moreover, the bandwidth for the ADCs in the position (spatial) channels is significantly relaxed by a single high-speed ADC used for the timing pickoff. By reducing the number of ADCs as well as the bandwidth requirement for the positioning ADCs, a net reduction in ADC power consumption can be realized.

The aforementioned architecture for SiPM array detection and readout is currently being explored at the University of Washington. A discrete board-level implementation of the row-column readout method has been realized in the lab with an emphasis towards integrating the decoder electronics into a single silicon device [1,4]. Eventually, our goal is to integrate all the analog detector electronics with the SiPM device into a single CMOS chip, or Multi-Chip Module (MCM).

This paper will first discuss some of the basics surrounding SiPM detectors followed by a description of the readout architecture. A discussion is then given on the challenges and strategies for realizing all the decoder analog and mixed-signal electronics in a silicon process. Lastly, some circuit simulation results are given for a transistor level model realized in Cadence for a 90nm TSMC, 9-layer CMOS process.

## II. DETECTORS AND CRYSTALS UNDER CONSIDERATION

The decoder electronics described in this paper was intended to interface with a variety of SiPM arrays with the initial device being a MAPD-3N array manufactured by Zecotek Photonics Inc, Singapore. The layout of the array is shown in Fig. 1(a) and 1(b). The SiPM pads are assembled into an 8x8 array of individual photodetection elements with a bias voltage approaching 90V. The individual elements in the array are spaced with a pitch of 3.6mm, while the entire detector array is  $3.3 \times 3.3 \text{ cm}^2$ , this includes the ceramic package. Fig. 1(a) shows the connector on the back side of the detector array. The cathode of each SiPM element has an

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<sup>1</sup>S. Dey, L. Banks, W. Xu, S.P. Chen, and J.C. Rudell are with the Electrical Engineering Department, University of Washington, Seattle, WA 98195-2500, USA (telephone: (206)685-1600, email: jcrudell@u.washington.edu).

<sup>2</sup>T.K. Lewellen, and R.S. Miyaoka are with the Radiology Department, University of Washington, Seattle, WA 98105, USA (telephone:(206)543-2084 email: tkldog@u.washington.edu)

individual output which can feed into a current amplifier. While all the cathodes of the 64 elements have their own output, the anodes are wired together. We propose to use the common anode channel for event timing. However, as explained later, when integrating the readout electronics in single chip form, it may be advantageous to simply use the cathode output for row, column, diagonal decoding in addition to generating a signal for the common pickoff.

However, for the current generation of ASIC targeted as an interface to our phase II board [4], the timing signal will be taken from the common anode. Fig. 1(c) shows the 8x8 lutetium-based scintillator crystal array (LFS-3, Zecotek) that we use for testing the SiPM array and supporting electronics. Each element of the crystal is optically isolated using diffuse reflecting material and measures 3.5mm by 3.5mm by 20mm.

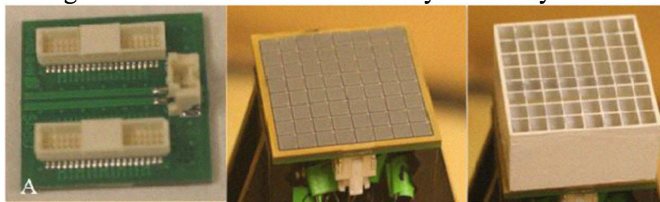


Figure.1(a) Connectors of the 8x8 SiPM array (b) SiPM elements (c) 8x8 LFS crystal array

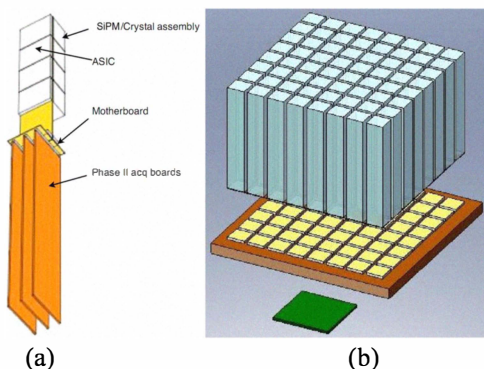


Figure.2 (a) Architecture of the proposed detector module (b) Detector assembly

### III. ARCHITECTURE FOR PHASE II INTERFACE ELECTRONICS

Although we eventually intend to integrate all the analog electronics on a single-silicon substrate along with the SiPM device, the initial architecture for the readout electronics was realized in discrete form and reported in [1-4]. The original proposed system is shown in figure 2 with the intention of reducing the number of channels from individual detectors in the array. The phase II interface boards described in [4] acquire both the cathode and the anode signals from the SiPM array.

Two amplifiers are used at the cathode of the SiPM device. In the discrete version of the board, each amplifier is realized with an operational transconductance amplifier (OTA) which drives an emitter-degenerated transconductance amplifier. The current output supplied by the transconductance amplifier is connected to a common line shared by other SiPM amplifier outputs assembled in a row or column format. The shared current output associated with an individual row or column

reduces the number of channels required for the entire SiPM array from  $N^2$  to  $2N$ . The reduction in the number of channels has the advantage of reducing the number of ADCs required. As part of the Phase II board, algorithms in the FPGA were designed to perform the pulse processing and to use low bandwidth pulses ( $< 60$  MHz) for reduced cost and power requirements of the ADCs. In addition to sensing a SiPM event from the cathode, the anodes of all the SiPM devices in the array were shorted to a common node. This was used as a common pickoff point. In short, an event detected by any element of the SiPM array is sensed by an amplifier at the shared anode. This allows better timing information with respect to any individual SiPM event in the array, since it reflects the total current drawn by the array when multiple elements are fired. As all SiPM elements share the common anode and the intent is to optimize timing, this particular timing channel needs significantly higher bandwidth for the amplifier electronics as compared to the amplifiers and ADCs associated with the individual row and column readout (spatial positioning) electronics. For example, the bandwidth of an individual row amplifier is on the order of a few MHz, while the electronics for the common pickoff requires at least 200MHz of bandwidth.

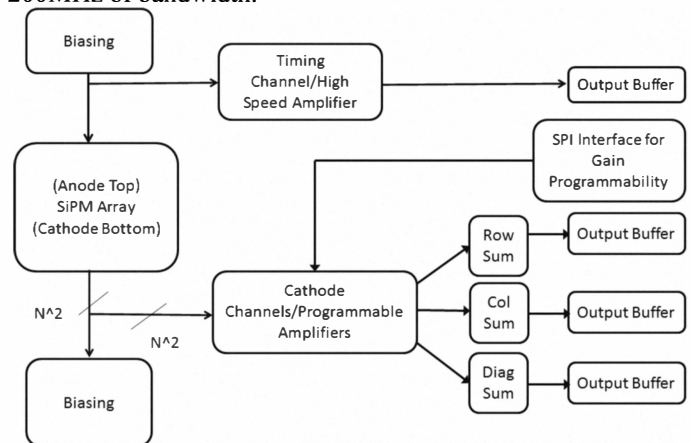


Figure 3. ASIC System-Level Block Diagram

The row, column and common pick off lines are fed to output buffers and then ADCs. For the phase II MiCEs board, an FPGA is then used for pulse reconstruction, timing alignment and array addressing information. The details of the FPGA are described in [5 – 8].

### IV. READOUT CIRCUITS AND STRATEGIES FOR INTEGRATION

A prototype board of the row-column decoder technique has been developed and measurements were taken to evaluate the effectiveness of the architecture [1]. Two versions of the board were developed and the second generation board showed significant improvement in both timing and energy resolution. At present, an IC design research group at the University of Washington is working with the Radiology department to realize an ASIC which replaces the discrete version of our prototype readout board. This section explores some of the

design issues and challenges associated with realizing this front-end ASIC interface.

At present we are designing both the individual amplifiers for the row-column decoder as well as a high-bandwidth (BW) amplifier for the current pickoff node. The ASIC will be between the SiPM array and the ADC board which also contains the FPGA; see Fig 4.

### INTEGRATED PHASE II MiCES INTERFACE

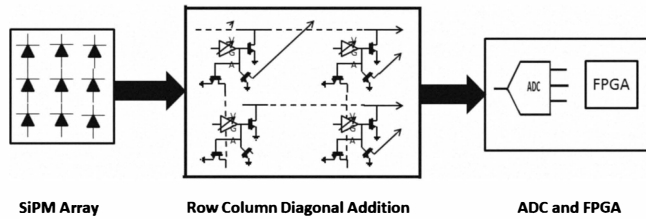


Figure 4. Intermediate goal, integration of electronics which act as the interface between the SiPM array and the FPGA board.

Our program seeks to eventually integrate the readout electronics either in the same package as the SiPM devices or on the same silicon substrate. This could potentially allow sophisticated calibration methods to address mismatch and non-idealities in the readout electronics. Moreover, by integrating all the electronics in the same package or silicon die, the SiPM could potentially produce a digital code which represents both location and intensity of a detected photon event; this is illustrated in Fig. 5.

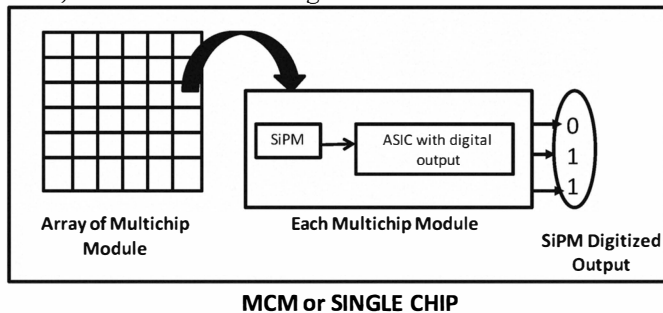


Figure 5. Long term goal to integrate electronics with SiPM.

Our goal is to realize an ASIC that is generic enough to work with multiple SiPM vendors and with a variety of readout interfaces. Although the Phase II MiCES interface electronics previously published only produces row and column data to fit the manufacturer used, other devices available could potentially accommodate diagonal readout from the SiPM array. Therefore, we are exploring circuit systems that are generic enough to produce a row, column and diagonal output. This is illustrated in Fig. 6.

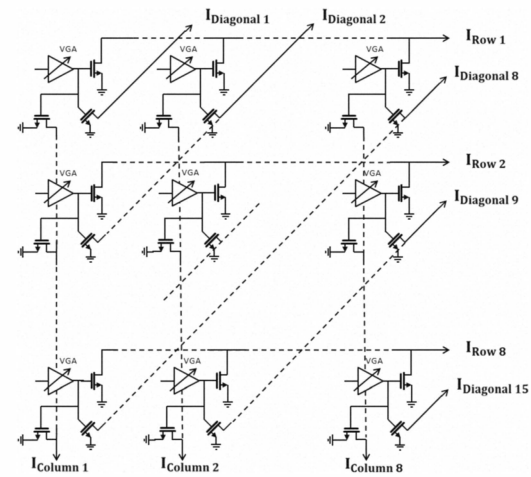


Figure 6. Row-Column-Diagonal Summation Topology

At present we are exploring readout electronics implemented in submicron CMOS technologies. This has the advantage of enhancing integration by eventually allowing the analog front-end amplifiers to exist on the same silicon as the ADCs, and the digital electronics, thus implying a reduction in area and cost. Moreover, by integrating the analog electronics on a silicon chip, significantly higher bandwidth and lower power solutions may be realized, as compared to the discrete counterpart. This is mainly due to a substantial reduction in parasitic capacitance when moving from a board to a monolithic silicon system level implementation of the hardware.

The circuit designs that we are exploring at present seek to address a number of challenges associated with PET scanner readout electronics. Such challenges include:

- Minimization of dark noise produced by thermal effects in the SiPM device, leading to an errant detection of photon events.
- Improved calibration algorithms to compensate for mismatch and variations due to Process, Voltage and Temperature (PVT), between elements within the SiPM array.
- Maximizing dynamic range.
- Minimizing distortion.

#### A. Single-Amplifier Interface

The electronics for the phase II MiCES FPGA interface electronics exploits use of both the SiPM cathode and anode. As mentioned earlier, the cathode of each SiPM device generates a common row and column current pulse, this is detailed in [1]. The anode is used for the common current pickoff producing timing information in the discrete solution. However, as an integrated solution, we are exploring using just the cathode of the SiPM device to generate all the necessary addressing and timing information. The proposed frontend architecture would look similar to Fig.7. Here one current amplifier is used to produce a row, column, diagonal and common pickoff output signal. This has the advantage of increased bandwidth at the SiPM – Current Amp interface as the signal produced by the SiPM is a current. In addition, current mode circuits are generally significantly faster than the

voltage mode counterpart. This is primarily due to the fact that current mode amplifiers typically drive low-impedance nodes. The input impedance looking into the amplifier can be made extremely low simply by utilizing shunt feedback or having a diode connected device to realize the input stage. The use of a single amplifier interface from the SiPM would reduce the likelihood of cross talk between the SiPM devices in the array. In addition, because a single amplifier is used for row, column, diagonal and pickoff signaling, the capacitance seen by the cathode is minimized, further increasing the bandwidth at the node between the SiPM and the amplifier.

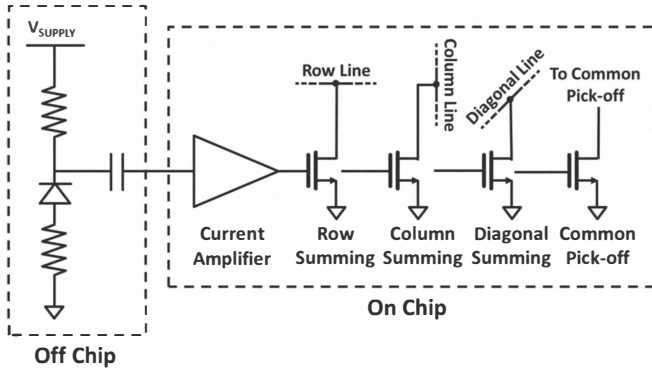


Figure 7. Proposed Front-End Amplifier Architecture

#### B. Dark Current Noise with shared row-column output

One challenge associated with the row-column summation approach is the potential accumulation of noise down a single line. This situation is illustrated in Fig 8, where the “dark” thermal noise of the individual SiPM devices is shown to accumulate with other detectors, due to the shared common current output on the row, column or diagonal output lines. When the noise is added at the output, there is an increased chance of false triggering as compared to a single-channel readout of individual SiPMs, as the accumulated noise from the row or column output, is likely to be comparable to a desired signal; fig. 8.

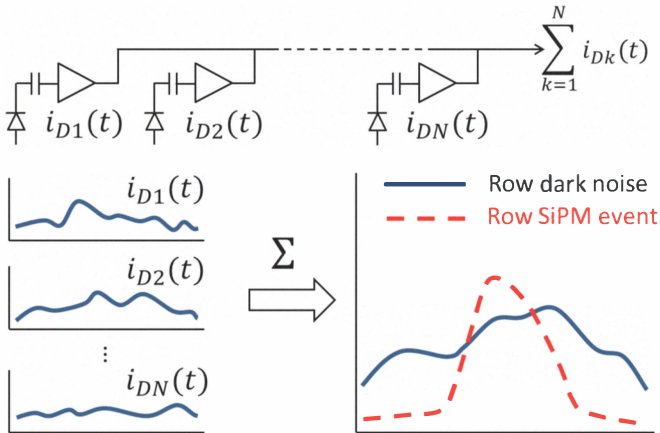


Figure 8. Noise accumulation along a single row

One advantage of integration in silicon is the possibility of enabling threshold-level detection. In short, the amplifier output stage could be disabled/disconnected from the summation lines running through the array. Then with a

variable threshold detection circuit, tunable to compensate for PVT variations, the amplifier would only make a contribution to a summation line if the signal were large enough to signify a detected gamma event. This approach will minimize the accumulation of noise in the addressing lines; see fig. 9.

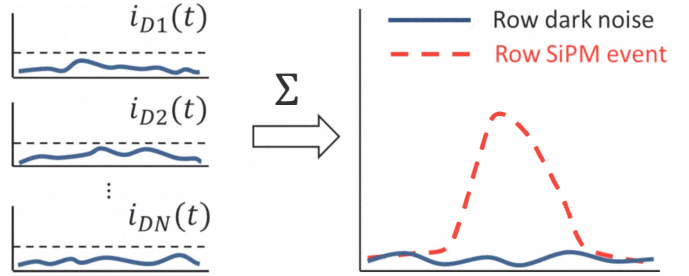


Figure 9. Illustration of noise reduction in row-column summation line with threshold detection.

Enabling threshold detection for a continuous-time amplifier would have challenges associated with delay matching between the amplifier output signal and the result of the threshold detection circuitry. Current comparators could be utilized for the detection circuitry. However, this circuit needs to be substantially faster than the main current amplifier which drives the output summation line. We see a longer term solution to address the delay matching of the threshold detection path by using switched-capacitor sampled-data techniques. This is a strong candidate for an approach that would integrate the front-end electronics in the same package, or on the same die with the SiPM device. A clocked sampled-data signal would permit accurate timing alignment between the threshold detection circuitry and that of the main row-column-diagonal amplifier. In addition, once the signal is sampled, further calibration algorithms may be used to tune PVT variations between the various SiPM elements. Lastly, by realizing the amplifier as a sampled-data circuit, the signal could then be easily digitized using conventional pipeline converters.

#### V. MOS CURRENT AMPLIFIER CIRCUIT

A transistor schematic of the SiPM output current amplifier design was realized using models from a 90nm TSMC PDK. As mentioned earlier, a single-input amplifier interfaces just the cathode of the SiPM device. A closed-loop shunt-shunt feedback amplifier is used. The feedback network produces a current which matches the current produced by the SiPM device. The amplifier itself produces a voltage output, but the current form of this signal, in the amplifier output stage is mirrored to produce current outputs for the row, column, diagonal and high-speed pickoff lines.

The circuit concept for this single-current input, multiple current output, is shown in fig. 10. The shunt feedback at the input of the amplifier has the desired effect of reducing the amplifier input impedance by the Loop Gain,  $\Gamma$ . However, the output of this amplifier produces a voltage. Again, emphasizing that the current in the feedback resistor,  $R_f$ , matches the current produced by the SiPM device. Therefore, to produce current gain in the opamp output stage, an auxiliary resistor,  $R_L$ , is used. Thus, the current pulse supplied by the

SiPM device is shunted to the amplifier summing node. The output of the opamp produces a voltage which is simply,  $V_o = i_{pulse} \cdot R_f$ . However, by adding the auxiliary resistor,  $R_L$ , additional current will be required by the opamp output stage. The current required by the output stage can then be described by,

$$i_o = i_{pulse} + \frac{i_{pulse} \cdot R_f}{R_L}$$

For large ratios of  $R_f$  to  $R_L$  the current gain can be approximated by,

$$i_o / i_{pulse} \cong R_f / R_L$$

Thus, by adjusting the resistor ratio, the current gain can be modulated and potentially calibrated. In addition,  $R_f$  and  $R_L$  were selected to keep a reasonable high loop bandwidth, thus ensuring the sufficient bandwidth of the current output signal.

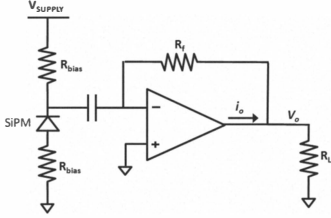


Figure 10. Concept of Current Amplifier Topology.

The amplifier uses a simple two stage configuration and is shown in fig. 11. A simple common source, differential to single-ended output realizes the first stage, while a simple common source configuration was designed for the output stage. The gate of the NMOS current source has been replicated to produce the four desired output signals required by each SiPM element in our array. Other opamp topologies are being explored, including those found in [9]. This approach has the advantage that the NMOS device in the driver stage is inside the feedback loop. Thus, the current produced at the drain of  $M_9$  is very linear. Moreover, the current supplied by the row, column, diagonal and common pickoff transistors are slaved to the device in the feedback loop, thus their current output will likewise be very linear. We are currently exploring more sophisticated opamp topologies which improve the output impedance, and bandwidth of the OTA.

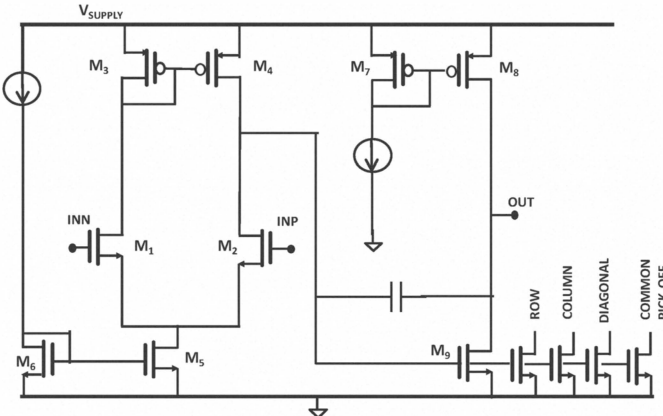


Figure 11. Two-Stage Amplifier with four current outputs.

## VI. AMPLIFIER SIMULATION

The circuits shown in fig. 10 and 11, were simulated using Cadence Spectre tools. Data was acquired from a SiPM device in the lab, and applied as an input signal to a transistor level model of the aforementioned design. This particular SiPM device is optimistically fast to exercise the speed of the current amplifier. The opamp consumes 1.2mA of current, running from a 2.5 V supply. With the pulse applied, the output signal was applied to the closed-loop amplifier, with both the input and output waveforms shown in fig. 12(a) and fig. 12(b). The resistor ratio  $R_f/R_L$  was designed for a ratio of approximately ten, thus implying a corresponding amount of current gain.

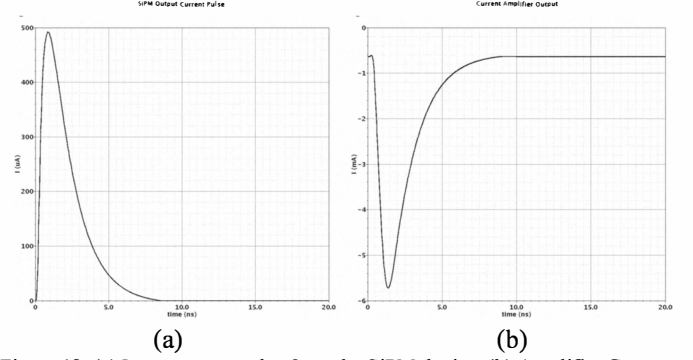


Figure 12. (a) Input current pulse from the SiPM device. (b) Amplifier Current Output.

## VII. CONCLUSIONS

Strategies for implementing SiPM frontend analog electronics have been presented in this paper. Current amplifiers were found to be the best approach with a single input to interface the SiPM cathode. This minimizes the detector loading while increasing the amplifier bandwidth for a minimal power consumption solution. Additional design work will take place over the coming months to realize the full system to eventually fabricate and interface with the Phase II MiCES FPGA board. An additional discussion was provided for some of the strategies towards integrating the electronics either on the same silicon substrate or potentially in the same package as the SiPM device.

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