

Overview for the Special Section on the 2007 Radio Frequency Integrated Circuits Symposium

THE May issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) is traditionally devoted to highlighting some of the advances in wireless integrated circuit design that are presented at the previous year's RFIC Symposium. In 2007, sun, sand and surf went along with circuits, systems and Smith charts in Honolulu, Hawaii, the site of last June's RFIC/IMS Conference. The RFIC Symposium continues to grow, with increasing attendance, higher quality papers and presentations, and a broader scope of wireless topics, making it the premier conference for publishing advances in the area of wireless IC design. Focus areas at this year's conference ranged from ultra-low-power radio ICs to a broad representation of standards based single-chip radios for PAN, WLAN, and WAN standards. In addition, millimeter-wave circuits and systems, some of which demonstrated operation above 100 GHz in conventional silicon technologies, were prevalent. This issue of the JOURNAL presents thirteen papers that reflect the general challenges that RF IC designers are confronting; mainly, practical integration of CMOS power amplifiers, implementation of integrated circuits from 60 GHz to above 100 GHz, and various circuit techniques to enable broadband/multi-band transceivers. In addition, two publications found in this issue present either extremely low-voltage or ultra-low-power circuits.

One of the last frontiers in achieving a true, single-chip CMOS transceivers is the integration of power amplifiers with reasonable efficiency and output power, for use in medium- to long-range radio applications. Two papers are presented which help advance the state-of-the-art in CMOS power amplifier design. The first paper in this issue, by Haldi *et al.*, titled "A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS," uses an innovative, integrated power combiner to realize a CMOS class AB linear PA which achieves 24.3 dBm maximum output power at a peak drain efficiency of 27% with a 1 dB compression point of 20.5 dBm. This is followed by a paper that compares the use of series-combining to parallel-combining transformers to realize an on-chip power combiner. The paper, "Power-Combining Transformer Techniques for Fully Integrated CMOS Power Amplifiers" by K. H. An *et al.*, describes two PAs which were fabricated to demonstrate the parallel-combining transformer approach. This paper reports output power for the two PAs of 31.2 dB and 32 dBm, with PAEs of 41% and 30%, respectively. These power amps operate off of a 3.3 V supply and are integrated in a 0.18 μm CMOS process.

The technology scaling of silicon devices continues to increase the achievable carrier frequency of which a transceiver can operate using a single-silicon die. The next pair of papers illustrate operation at 60 GHz and higher frequency bands using conventional silicon technologies. The first paper is "A 16–18.8-GHz Sub-Integer-N Frequency Synthesizer for 60-GHz Transceivers." The author, B. A. Floyd, demonstrates a frequency synthesizer that is capable of generating 55.8 to 65.8 GHz and a divided version of 16.0 to 18.8 GHz in 0.13 μm SiGe BiCMOS technology using 144 mW from a 1.2 and 2.7 V supply. The synthesizer features a phase-rotating multi-modulus divider capable of sub-integer division. This paper is followed by a complete transceiver which reports an operating frequency of 165 GHz, written by E. Laskin *et al.*, entitled "165-GHz Transceiver in SiGe Technology." For the first time, the feasibility of SiGe BiCMOS circuits in the 100–180-GHz range is demonstrated. Highlights of this device are broadband vertically stacked transformers for single-ended-to-differential conversion, a static frequency divider, an 80 GHz quadrature Colpitts oscillator, Gilbert cell mixers, and a five-stage amplifier. The device has a down-conversion gain of -3 dB while the PAs have a saturated output power of 0 dBm at 165 GHz, and consume 0.9 W. This chip occupies an area of $840 \mu\text{m} \times 1395 \mu\text{m}$.

Most of the remaining papers found in this issue advance the state-of-the-art integrated circuit design for wireless applications by demonstrating multi-band operation. This group of papers begins with "A Low-Power Single-Weight-Combiner 802.11abg SoC in 0.13 μm CMOS for Embedded Applications Utilizing An Area and Power Efficient Cartesian Phase Shifter and Mixer Circuit," by A. Afsahi *et al.* The device described in this paper uses a novel signal-path Cartesian phase generation and combination technique to achieve the best reported sensitivity and lowest power consumption in its class. The radio and AFE occupy 100 mm^2 and consumes 85 mW off a 1.2 V supply. This is followed by another paper which presents a clever scheme to recycle a single-mixer stage to perform multiple frequency translations. The paper titled, "Recursive Receiver Down-Converters With Multiband Feedback and Gain-Reuse" by J. Han and R. Gharpurey, describes two mixer designs using a recursive technique which is fabricated in a 0.13- μm CMOS process achieving peak gains of 50 and 56 dB with noise figures of 12.7 and 9.4 dB and an OIP3 of 8 and 11 dBV while consuming 2.9 and 2.1 mA off of a 1.2 V supply. The seventh paper, entitled "A Broadband Low-Cost Direct-Conversion Receiver Front-End in 90 nm CMOS" by J.-H. C. Zhan *et al.*, describes a broadband receiver which eliminates the need for on-chip spiral inductors, thus reducing the overall die area and lowering cost. This device occupies

0.2 mm² of active area and operates in the 2–5.8 GHz band while dissipating 85 mW with 44 dB of total gain. The double sideband noise figure is –21 dBm and a measured inband IIP₃ of –15 dB is reported.

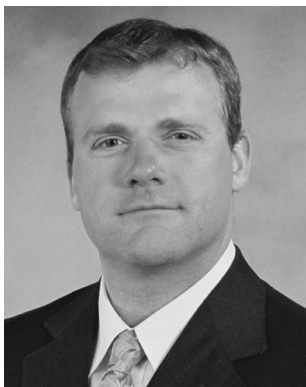
Although the next papers do not necessarily focus on multi-band operation, they do address significant challenges which face all RF IC designers in the coming years. The eighth paper in this issue confronts the design challenges associated with the required low-supply voltages of future silicon CMOS technologies. Specifically, “A 2.4-GHz ISM-Band Sliding-IF Receiver with a 0.5 V Supply” by N. Stanic *et al.* describes a 90 nm CMOS receiver with an LNA, image-reject LC filter, sliding IF two-stage mixer and baseband section all of which operate off of a 0.5 V supply. The device has a gain of 30 dB, noise figure of 18 dB while occupying an area of 3.4 mm² and consumes 8.5 mW. A number of papers at this year’s conference focused on ultra-low-power SOCs for sensor node and RFID applications. Written by P. B. Khannur *et al.*, “A Universal UHF RFID Reader IC in 0.18- μ m CMOS Technology” operates in the 860 to 960 MHz RFID band and is an example of low-power RFID technology. This device consumes 540 mW from a 1.8 V supply and integrates 10-bit DACs, pulse-shaping filters, an IQ modulator and a power amplifier in the transmit chain, while the receiver contains a LNA, downconverters, channel-select filter, and 10-bit ADCs.

The last set of papers for this issue focus on building blocks which address multi-band or wideband operation and a concluding article on an integrated self-testing LNA. The first paper in this section and the tenth paper in this issue addresses the need for extremely broad tuning range VCOs which are required in multi-band frontends. This paper, “Design of Wide Tuning-Range CMOS VCOs Using Switched Coupled-Inductors” by M. Demirkan *et al.*, describes a technique to augment existing capacitive tuning methods by performing a coarse tuning of spiral inductors. An analysis of different methods for switching in and out turns of an integrated spiral inductor is described. The inductor with selectable turns was then used in an experimental VCO which was realized with a 90 nm digital CMOS

process. This oscillator achieves a 62% tuning range with a 11.75 GHz center frequency, and –106 dBc/Hz phase noise at 1 MHz offset while dissipating 7.7 mW from a 1.2 V supply. The next paper demonstrates the broadband capability of an inductorless LNA which uses a circuit scheme that simultaneously cancels both noise and distortion in the signal path. “A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation” by W.-H. Chen *et al.* implements a noise and distortion cancelling LNA in a 0.13 μ m CMOS technology. It achieves +16 dBm IIP₃ with a gain of 14.5 dB and noise figure of 2.6 dB from 800 MHz to 2.1 GHz while consuming 11.6 mA from a 1.5 V supply. The next paper, “A CMOS VCO and LNA Using Tuned-Input Tuned-Output Circuits” by S. Shekhar *et al.*, describes a novel circuit topology which enables both a VCO and an LNA to achieve extremely low power with excellent performance through the use of a clever current reuse scheme. The measured VCO phase noise is –130.5 dBc/Hz at 1 MHz offset while operating at 2.5 GHz. The amplifier has more than 20 dB of gain and consumes 2.7 mW. Finally, the last paper of this issue, “Design of a 0.9 V 2.45 GHz Self-Testable and Reliability-Enhanced CMOS LNA” by M. Cimino *et al.*, presents a novel scheme for an integrated self-testing on-chip LNA. Parametric faults are injected and detected to demonstrate the efficiency of the BIST circuitry used.

In closing, I would like to invite everyone to Atlanta, Georgia, for the 2008 RFIC Symposium, to be held from June 15th to 17th. This year’s conference will again present the latest advances in the wireless chipset industry. For detailed information on the conference, I encourage you to visit the following website, <http://www.rfic2008.org>. All of us on the RFIC program committee look forward to seeing you in Atlanta. Finally, I hope you enjoy this issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

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