Alignment and Performance Considerations for Capacitive, Inductive, and Optical Proximity Communication

Arka Majumdar, John E. Cunningham, and Ashok V. Krishnamoorthy

***Abstract*—We present a comparative analysis of different physical approaches to chip-to-chip proximity communication, PxC, based on capacitive, inductive and optical signalling. Each method is modeled theoretically and the tolerances for packaging are identified. Analytical formulas for performance in terms of the pad size and pad spacing are derived and compared to reported experimental data. The tolerance of each communication method to misalignment is reported. The design space in terms of channel density and chip separation for capacitive and inductive proximity communication is explored for a specified bit-error-rate (BER) or signal-to-noise ratio (SNR) and transmitter power or voltage. The relative merits of each technology are discussed. A general conclusion is that capacitive proximity communication is advantageous for dense communication with small pads at low voltages and when low raw bit-error rates are required; however a hard requirement for vertical separation between chips is identified, independent of the area of the pads, and fixed by the supply voltage and the technology parameters. On the other hand, inductive communication provides a larger working range of chip separations, and is advantageous when larger pad sizes are used; however the minimum voltage is similarly constrained in order to maintain low bit-error rates. Optical proximity communication potentially provides the largest chip separations, but has low tolerance to in-plane misalignment.**

***Index Terms*—Capacitance modeling, cross-talk, Gaussian beam theory, misalignment, mutual inductance, packaging, proximity communication, wireless interconnects.**

I. Introduction

DIGITAL processing of information requires nonlinear devices for logic operations and storage; and also interconnects to relay the information from one place to the other. The energy requirement for relaying this information typically increases sharply as the signal exits the processor and memory chips and is forced to traverse a second level package and printed circuit board. Highly sought are low power communication interfaces that can relay information from one chip to another while maintaining the density performance metrics associated with on-chip wiring. One such interface is proximity communication [3]. The idea of proximity communication was first investigated by Salzman and Knight in the context of multichip modules [1], [2]. Proximity communication can be broadly defined as wireless communication between chips, and has been investigated by means of capacitive coupling [3], [4] inductive coupling [5]–[7], and optical coupling [10] between chips. It has already been established that proximity communication provides considerable advantages over wired communication [3], [9], [12]. With capacitive coupling, changing a voltage at a transmitter plate induces a voltage change in the receiver plate that can be amplified to digital logic levels. In inductive coupling, a transmitter changes the current in a metal inductor and a receiver samples the voltage induced by the current and then recovers the data. With optical proximity communication, light of one or more wavelengths in a waveguide on the transmitter chip is coupled to a waveguide on the receiver chip without conversion to the electrical domain. At the physical level, all the three forms of inter-chip communication are based on coupling of electromagnetic waves across two chips with capacitive proximity being the electrical component, inductive proximity being the magnetic component and optical proximity combining both the electrical and magnetic components. Fig. 1 shows schematic diagrams of all three proximity communication methods.

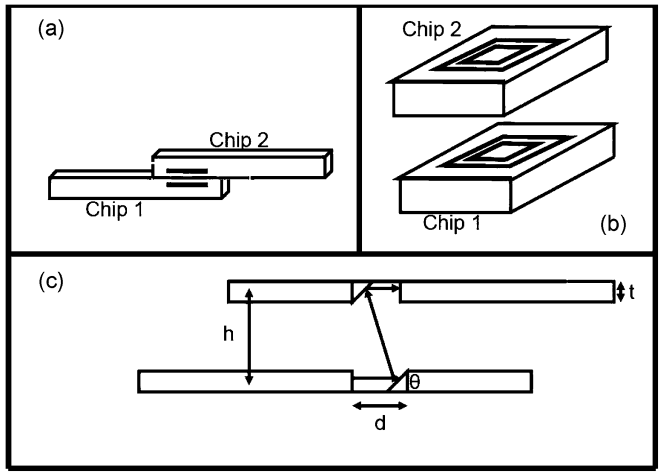

Fig. 1. Schematic of proximity communication methods. (a) Capacitive proximity. (b) Inductive proximity. (c) Optical proximity.

The idea of proximity communication while simple in concept, presents a number of packaging related challenges when attempting to reduce it to a practical implementation. Among these are the critical parameters of alignment tolerance and

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cross-talk, which will be the focus of this paper. These two parameters have competing requirements because any attempt to improve one while maintaining high-density communication with low error rates causes a penalty in the other and hence both cannot independently be optimized. However each of the three PxC methods behave differently in terms of their crosstalk and alignment sensitivity, and the question of which of the PxC methods offers the simplest packaging solutions and the best path to a robust, manufacturable communications interface is an open one. To help answer this, we develop analytical models of these two critical parameters for each of the PxC methods and compare their performance. We note that a considerable amount of circuit techniques have been developed in recent years to optimize the performance of capacitive and inductive proximity [13], [14]. For simplicity, in our approach we assumed that in each case, no special circuit techniques are used to enhance the alignment tolerance. For completeness, the analytical results are compared for agreement with experimental data reported elsewhere.

In this paper Sections II, III, and IV present analytical models for capacitive, inductive, and optical proximity, respectively. Section V describes how cross-talk noise affects signal-to-noise ratio (SNR) and Section VI gives an approximate power calculation method to normalize the performance of capacitive and inductive proximity. Section VII reports results and compares different proximity schemes. Section VIII concludes the paper.

II. Capacitance Modeling

Considerable effort has been devoted to modeling a parallel-plate capacitance in 1-D taking into consideration fringing effects [15], [17]. There are several approximate formulas for the capacitance per unit length of an infinitely long micro-strip line over a ground plane, but the capacitance between two finite parallel plates has not been exactly modeled. Here, the expression in [15] is improved to model the capacitance between finite plates. The capacitance between two finite metal plates (separated by a distance d) of dimension $w \times l$ and thickness t is given by

$$C = \epsilon_0 \epsilon_r \left[\frac{(w - t/2)(l - t/2)}{d} + \pi(l + w) f(d/2, t) \right] \quad (1)$$

where $f(d,t)$ is given by

$$f(d,t) = \left[log_e \left(1 + \frac{2d}{t} + \sqrt{\frac{2d}{t}\left(\frac{2d}{t} + 2\right)} \right) \right]^{-1} \quad (2)$$

where ϵ_o is the permittivity of free space and ϵ_r is given by $\epsilon_r = d(\sum_i (d_i/\epsilon_i))^{-1}$, where d_i and ϵ_i are the thickness and dielectric constant for i^{th} dielectric (in a VLSI chip, there can be multiple dielectric layers present between the two metal plates). Fig. 2 shows analytically calculated and experimentally measured capacitances [16]. Details of the capacitance models are provided in Appendix I.

It should be noted that, the fabricated capacitance is not from a continuous pad, but rather from an array of pads. The fringing term used in (1) is calculated assuming no neighboring pads. If there are neighboring pads, then the fringing fields from one plate will be shared between the lateral neighboring pads and the plate over it. To model that, the fringing capacitance is multiplied by a factor of x_1/x_1+d, where x_1 is the distance between two lateral neighboring pads.

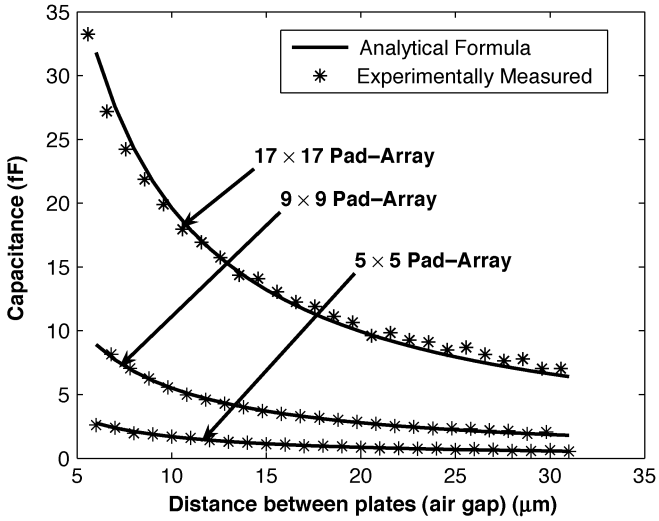

Fig. 2. Capacitance value calculated analytically and measured experimentally. In the experiment, there were array of pads of dimension $8\ \mu\mathrm{m} \times 8\ \mu\mathrm{m}$ with a pitch (center to center distance between pads) of $9\ \mu\mathrm{m}$. Each metallic pad is made of Aluminium (thickness of $1\ \mu\mathrm{m}$) and has a passivation layer of $1\,\mu\mathrm{m}\ SiN$ (dielectric constant 7.9) and $1\ \mu\mathrm{m}\ SiO_2$ (dielectric constant 4.1).

A. Circuit Model for Capacitive Proximity

In a practical circuit, there are several pads for communication. The parallel plate capacitance alone does not provide a realistic picture. Modeling of both cross-talk capacitance as well as the capacitance for misaligned parallel plates is necessary. To do this an understanding of the physical origin of these capacitances is useful.

The capacitance between two pads (a transmitter and its corresponding receiver) is the desired capacitance (C_s). There is a stray or parasitic capacitance (C_p) (capacitance between each pad and the ground plane) and a capacitance that causes cross-talk (C_{xt}), arising from the neighboring pads. The geometrical parameters along with the origin of different capacitances are shown in Fig. 3.

The desired signal capacitance C_s (when the plates are not misaligned) was modeled above. C_p depends on the technology parameters and the pad area. C_p for a square pad with side x can be modeled as $C_0 x + C_1 x^2$, where C_0 accounts for the fringing capacitance due to side walls and C_1 accounts for the parallel plate part of C_p. Fitting this model to experimentally-obtained stray capacitances, one finds that for 0.18 μ technology, $C_0 = 0.1\ \mathrm{fF}/\mu\mathrm{m}$; $C_1 = 0.03\ \mathrm{fF}/\mu\mathrm{m}^2$. The cross-talk capacitance originates from two different mechanisms, as shown in Fig. 3. One is the capacitance between one transmitter and another receiver, and the other is the capacitance between two adjacent receivers. Each must be modeled separately. The detailed derivation of the cross-talk capacitance as well as the misaligned capacitance is provided in the Appendix. Fig. 4 shows the analytically calculated and measured values of the capacitance when the plates are misaligned.

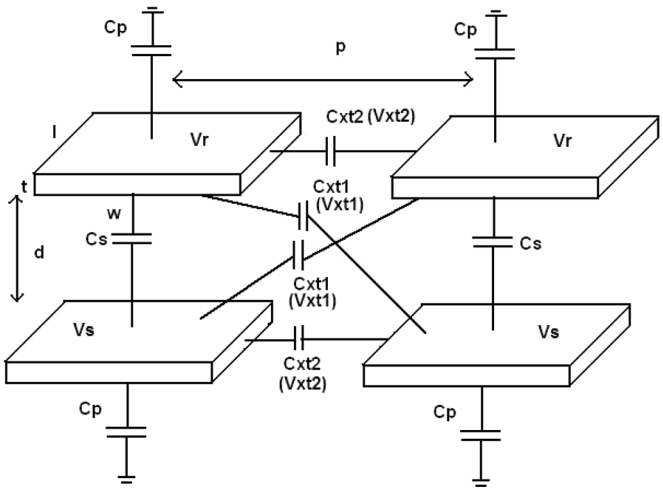

Fig. 3. Geometrical dimensions and the capacitances between neighboring plates in capacitive proximity communication (signal, parasitic, and cross-talk capacitances).

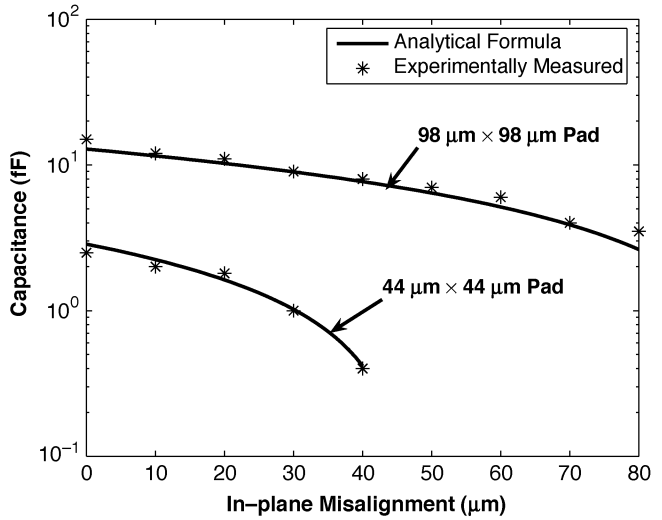

Fig. 4. Analytically calculated and measured capacitance when the plates are misaligned.

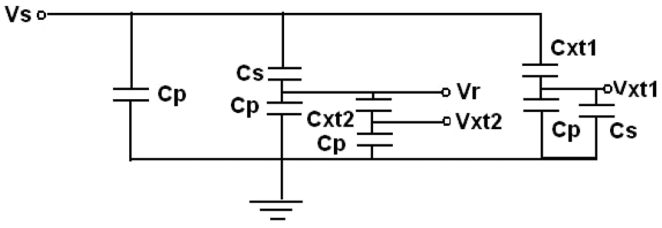

Fig. 5. Equivalent circuit for capacitive proximity communication.

Fig. 5 shows the circuit model for capacitive PxC. If the receiver has an input gate capacitance of C_{in} (typical value of C_{in} is 10–15 fF), then

$$V_r = V_s \frac{C_s}{C_s + C_p + C_{in} + C_{xt2}} \tag{3}$$

$$V_{xt} = V_{xt1} + V_{xt2} \tag{4}$$

$$V_{xt1} = V_s \frac{C_{xt1}}{C_s + C_p + C_{in} + C_{xt1}} \tag{5}$$

$$V_{xt2} = V_r \frac{C_{xt2}}{C_p + C_{in} + C_{xt2}} \tag{6}$$

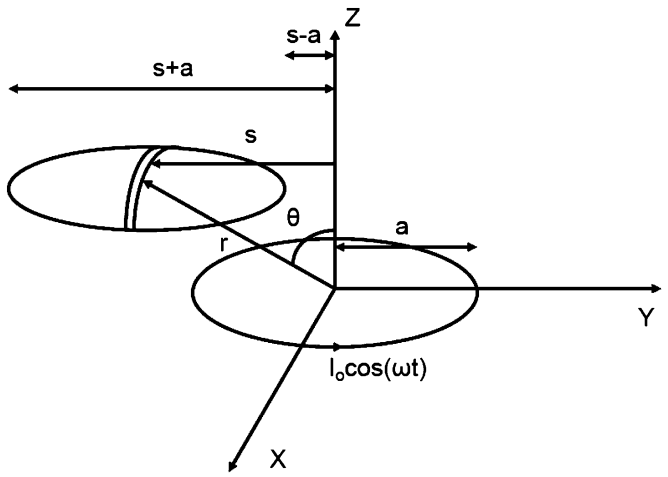

Fig. 6. Figure showing the parameters for modeling coupled flux in inductive coupling.

where V_s, V_r, and V_{xt} are the signal, received and cross-talk voltage amplitudes, respectively. V_{xt} has two components: V_{xt1} is due to capacitance C_{xt1} and V_{xt2} is due to capacitance C_{xt2} (Fig. 5). In a circuit implementation, V_{xt2} is often very small (as $C_{xt2} \ll C_{xt1} \ll C_p$) and can be neglected. It should be noted that the model described here appears frequency independent, which is not strictly correct. In practice, there are finite parasitic resistances (resistance of the leaky capacitances, driver resistance and/or receiver resistance) that make the circuit a low pass filter and thus limit the bit-rate. For the purposes of this study it is assumed that the circuit is operating in the pass-band.

III. Inductive Coupling

The inductors in modern VLSI technology are planar and typically rectangular in shape. But to obtain an analytical expression, inductors are assumed to have a spiral shape [8].

A. Modeling Inductors

For a coil of radius a carrying current I, the magnetic field components at a point (distance from center is r and making an angle θ with z-direction) is given by [18]

$$B_r = \frac{\mu_0 I a^2 \cos\theta}{2(a^2+r^2)^{1.5}} \left[1 + \frac{15a^2r^2\sin^2\theta}{4(a^2+r^2)^2}\right] \tag{7}$$

and

$$B_\theta = -\frac{\mu_0 I a^2 \sin\theta}{4(a^2+r^2)^{2.5}} \left[2a^2 - r^2 + \frac{15a^2r^2\sin^2\theta(4a^2-3r^2)}{8(a^2+r^2)^2}\right] \tag{8}$$

where μ_0 is the magnetic permeability of free space. The flux coupled to a receiving coil due to a current in a transmitting coil (Fig. 6) must be calculated. Due to the circular nature of the current-carrying wire, an arc can be found in the receiving loop (as shown in Fig. 6) where the magnetic field is constant and thus the flux linked to the loop can be readily found by integrating over the area of the loop. The total flux (Φ) is given by

$$\Phi = \int_{x=s-a}^{x=s+a} dx |B_r \cos\theta - B_\theta \sin\theta| 2x \cos^{-1}\left(\frac{x^2+s^2-a^2}{2xs}\right). \tag{9}$$

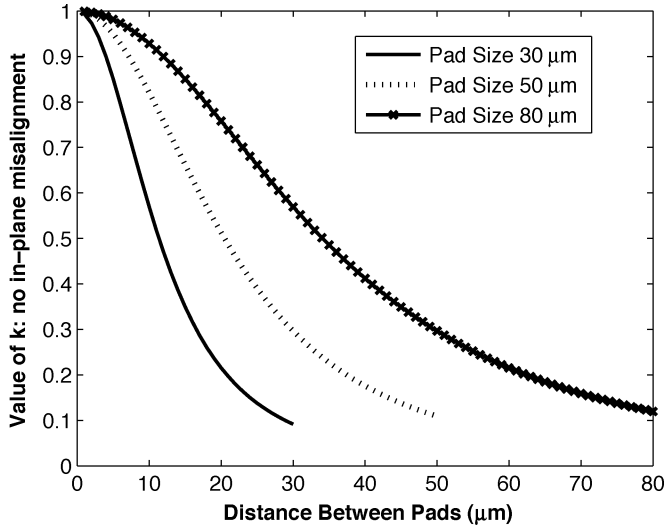

Fig. 7. Figure showing the value of k as a function of pad-separation for various pad sizes.

A calculation of Φ shows us that it is linearly proportional to the current I in one inductor. Hence, the e.m.f. ε generated in the other inductor can be written as

$$\varepsilon = \frac{d\Phi}{dt} = \frac{d(\beta I)}{dt} = \beta \frac{dI}{dt}. \tag{10}$$

The mutual inductance M between two inductors L_1 and L_2 is defined as

$$\varepsilon = M \frac{dI}{dt} \tag{11}$$

M is also given by $k\sqrt{L_1 L_2}$, where $k(0 < k < 1)$ depends on the relative position, size and shape of two coils. k thus provides the tolerance towards misalignment. It is assumed that $\Phi = \Phi_{\max}$ and $k = 1$ when the two coils are placed close to each other. For any other position $k = \Phi/\Phi_{\max}$. Fig. 7 shows values of k for different vertical separations between pads. As explained above, the inductors are rectangularly shaped in practice. When using the approximation for circular inductors, for a corresponding square inductor with outer side d_{out} and inner side d_{int}, the circular inductor is assumed to have a radius of $0.25(d_{\text{int}} + d_{\text{out}})$. The values of inductors and other parasitics (capacitors and resistances) are related to the layout parameters. Wire thickness and gap between wires are kept at 1 μm [7] and it is assumed that number of turns in the inductor are 3. While it is true that one can increase the inductance by increasing number of turns, for smaller pad sizes, the number of turns is limited by metal thickness. The performance of inductive PxC can be enhanced by using multilayer metals and thereby increasing number of turns (even for smaller pads). An approximate expression for k, based on the assumptions that the field is constant in the loop area and the horizontal separation is small compared to the radius of the coil, is provided in [7]. Here a full integration is performed to obtain a more accurate value of k; this approach is also valid for the case when the horizontal separation is comparable to the radius of the coil. The values of k calculated here match those provided in [7] when the horizontal separation is small and area of the loop is small. Unfortunately, a generalized closed form expression could not be found.

B. Cross-Talk

The model described above can be used to find the cross-talk because the cross-talk is also modeled as a mutual inductance between two inductors. For inductive PxC the cross-talk from nearest neighbors can be exactly zero at certain positions. These positions occur where the field lines going up and going down integrated over the loop-area are equal. However, the tolerance of these points is small and minor mis-alignment in pad placement can result in significant cross-talk.

C. Circuit Model

The circuit given in [7] is used to model inductive coupling. A similar circuit is used for finding cross-talk voltage. Note that for inductive PxC, a current is induced in the receiving chip by a current in the transmitter. The circuit proposed in [7] converts the voltage to a current. Here the resistance used to do voltage to current conversion is assumed to be 50 Ω. The output transmitter capacitance is assumed to be 500 fF.

IV. Optical Proximity

The idea of optical proximity communication (OPxC) has recently been proposed [10]. To find the alignment sensitivity for OPxC, gaussian beam theory is applied [19]. As the chip gap in Fig. 1(c) increases the chip to chip coupling decreases for a number of reasons. One deleterious effect develops when the reflecting mirrors are built in (100) Si platform using a (111) facet plane created by anisotropic etching. In this case, as the chip gap increases the optical beam eventually walks off the receiving mirror. This can be corrected with a lateral shift of the chips for each change in the coupling gap or by using 45° micromirrors as opposed to (111) facet planes. This clipping of the optical signal (due to the beam walking off the mirror) is not modeled here. Hence the effect of the reflections is simply the propagation across a distance of $l = 2d + (h - t/sin2\theta)$ [see Fig. 1(c)] through a dielectric medium. If the beam radius is w_0 and the curvature is $R = \infty$ at the transmitter waveguide, then the beam radius at the receiver waveguide is

$$w_R = \sqrt{\left(\frac{\lambda^2 l^2 + \pi^2 w_0^4}{\pi^2 w_0^2}\right)} \tag{12}$$

and the curvature is

$$R_R = l + \frac{\pi w_0^2}{\lambda^2 l}. \tag{13}$$

Using these, the beam profile close to the other waveguide can be found. If the coordinate of the point (from where light exits) on the transmitter waveguide is (0,0,0), then the coordinate of the point (where light impinges) on the receiver waveguide will be (X_0, Y_0, l). X_0 and Y_0 are the lateral misalignments and are zero if the light falls at center of the receiver waveguide. Denoting the electric field at the transmitter as E_T and at the receiver as E_R, the coupling efficiency η is given by

$$\eta = \frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} E_T^* E_R dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} |E_T|^2 dxdy}. \tag{14}$$

The final expression of η is

$$\eta = \frac{w_0}{w_R}\frac{A_T}{A_R} exp[-i\Psi] exp\left[\frac{B_x^2 + B_y^2 - 4A_R C_x - 4A_R C_y}{4A_R}\right] \tag{15}$$

where

$$\Psi = \frac{2\pi}{\lambda}(l+\phi)$$
$$A_T = \frac{1}{w_0^2}$$
$$A_R = \frac{1}{w_0^2} + \frac{1}{w_R^2} + \frac{i\pi}{\lambda R_R}$$
$$B_x = \frac{-2(X_0 \cos\alpha + Y_0 \sin\alpha)}{w_0^2}$$
$$B_y = \frac{2(X_0 \sin\alpha - Y_0 \cos\alpha)}{w_0^2}$$
$$C_x = \left(\frac{X_0}{w_0}\right)^2$$
$$C_y = \left(\frac{Y_0}{w_0}\right)^2$$
$$\phi = \tan^{-1}\left(\frac{\lambda l}{\pi w_0^2}\right)$$

where α is the angle of rotation between the co-ordinates used for the transmitter and receiver. While the tolerance due to the gap variation between pads is calculated, X_0 becomes $|h - h_0|/\tan 2\theta$, where h_0 is the distance for which the light beam remains at the center of the mirror). Here it is assumed that the beam has a radius of 3 μm and a wavelength (λ) of 1550 nm.

V. Cross-Talk Noise and BER

Let us assume that $x(t)$ is the desired signal, $c(t)$ is the cross-talk nosie and $n(t)$ is white Gaussian noise. To avoid any complication related to the circuit configuration, a typical value of rms noise (of power σ_n^2) is used in the calculation, which includes thermal noise, power supply noise and all other constant circuit noise. In practice, the value of this constant noise is on the order of 1 mV. It is assumed that the detection point is kept at $0.5x(t)$ to obtain optimal performance (assuming equi-probable binary signals).

The circuits commonly used for PxC are synchronous and hence the cross-talk signal will affect only the signal, and not the noise. Hence, BER is defined as

$$\text{BER} = \frac{1}{4} erfc\left(\frac{0.5x - c - M}{\sqrt{2}\sigma_n}\right) + \frac{1}{4} erfc\left(\frac{0.5x + c - M}{\sqrt{2}\sigma_n}\right) \tag{16}$$

where M is due to transistor mismatch, c is the cross-talk noise and $erfc$ is the error function associated with Gaussian random variables. M depends on the transistor dimension and decreases with increasing transistor size.

We emphasize that both $x(t)$ and $c(t)$ are dependent on V_s but the constant circuit noise is not. Hence, the dependence of the performance on the supply voltage differs for capacitive and inductive proximity because the cross-talk is different for the two methods.

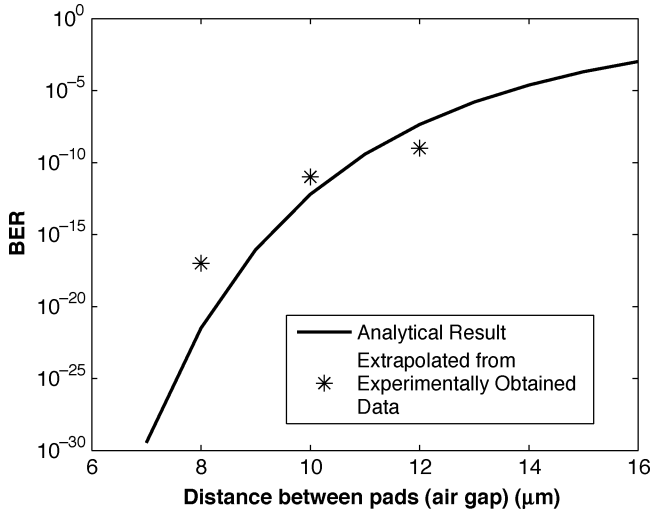

Fig. 8. Figure showing the experimental result (extrapolated from [20] for zero timing margin) and the analytical prediction. Because the experiment used differential signaling with two pairs of pads, the crosstalk is made zero in the analytical model. Pad dimensions: $106\ \mu \times 106\ \mu$. Center-to-center separation between two adjacent pads: 126 μm. Parasitic cap is 500 fF and supply is 1.1 V. Transistor mismatch voltage is 5 mV. Constant rms noise is 1 mV.

VI. Transmitter Energy Calculation

The energy required to communicate data via PxC is a key performance criteria and may be used to compare the different methods. Here, only the switching energy required to communicate between two chips is calculated. The switching energy needed to transmit data via capacitive coupling is given by the sum of the energy spent at transmitter-plate $(0.5(C_p||C_s)V_s^2))$, the energy spent to charge the parasitic capacitance $(0.5C_pV_s^2)$, and the energy wasted due to the cross-talk capacitance $(0.5(C_p||C_{xt})V_s^2))$. For inductive coupling, the transmitter inductance is driven and the field generated by the transmitter drives the receiver. Hence the switching energy needed is given by $0.5L_tI_t^2 + 0.5k\sqrt{L_tL_r}I_t^2$, where L_t is inductance of the transmitters, L_r is inductance of the receiver, and I_t is the current in the transmitter circuit. The factor of 0.5 appears because half of the bits are 0 and hence nothing is transmitted. It is assumed as a first-hand approximation that inductive and capacitive proximity methods differ only in the energy required to transmit the signal and that all other power (receiver power, power due to clocking and the power due to relaying the signal to the proximity pads) are the same.

VII. Results

A. Comparison With Experimental Result

To validate the theory, the analytical result is compared with experimental data published elsewhere. Fig. 8 shows the experimental result from [20] (extrapolated for zero timing margin) along with the predictions from the analytical formula for capacitive coupling. In this experiment, the test-chip was fabricated via a 90-nm commercial CMOS process; a six-axis manipulator was used to correct the relative board positions until the capacitive PxC transmitter and receiver were laterally aligned. Then the pads were vertically separated to obtain the tolerance to the

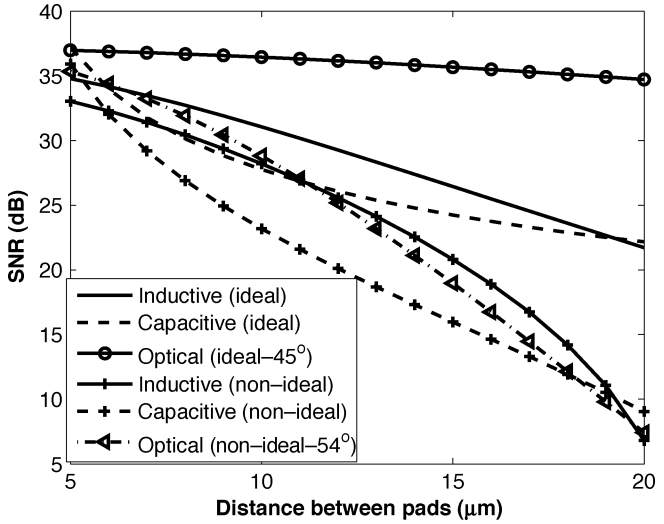

Fig. 9. SNR for the three proximity methods versus variation in the gap (chip separation) between pads. The pad dimension is $30\ \mu\mathrm{m} \times 30\ \mu\mathrm{m}$. Supply voltage is 0.7 V. For optical proximity, the beam radius is $3\ \mu\mathrm{m}$.

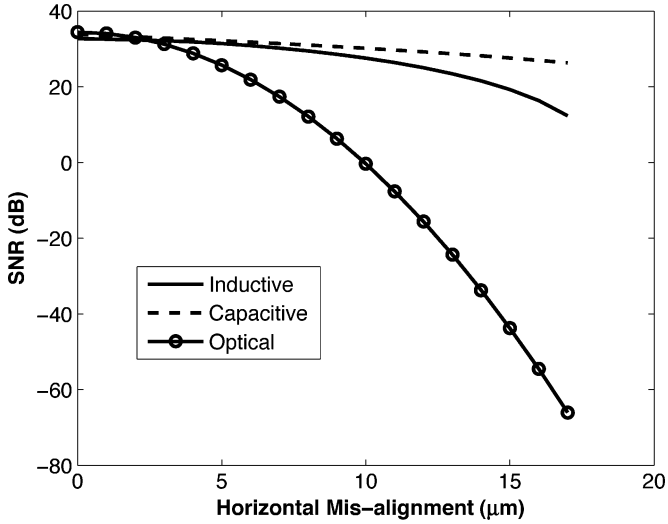

Fig. 10. SNR for the three proximity methods versus in-plane (lateral) misalignment between pads. Here it is assumed that only one direction (either x or y) is misaligned. The pad dimension is $30\ \mu\mathrm{m} \times 30\ \mu\mathrm{m}$. The gap between pads including all dielectrics, is $8\ \mu\mathrm{m}$. The supply voltage is 0.7 V. For optical proximity, the beam radius is $3\ \mu\mathrm{m}$. In general, lateral misalignment can also cause crosstalk to increase. To isolate the effect of misalignment and to make the comparisons simpler, this effect is ignored, and the crosstalk is kept constant at the value for zero lateral misalignment.

pad-to-pad distance. The chip incorporated a cross-talk cancellation technique (differential signalling). Hence in the analytical calculation cross-talk was not included. As shown the experimental result matches quite well with the predicted analytical result. In all the calculations for capacitive PxC, it is assumed that there is a passivation layer of $1\ \mu\mathrm{m}\ SiN$ and $1\ \mu\mathrm{m}$ of SiO_2 over each pad.

B. Misalignment Tolerance

These three different methods are compared in terms of their tolerance to lateral misalignment (i.e., in x and y directions) and to chip separation. Cross-talk noise is included for capacitive and inductive PxC. In practice, optical cross-talk noise is very small and here it is ignored. For inductive communication it is assumed that there are four neighbors that contribute to the cross-talk (the contribution of distant pads is negligible). The model takes into account capacitive crosstalk from an infinite number of pads (though the effect of distant pads is small). We make the further assumptions that all pads are square; that transmitter-pads are separated by half of the length; and that receiver pads have the same area as transmitter pads. The input signal amplitude is kept constant for both capacitive and inductive proximity. For optical communication, the required transmitter power depends on the receiver sensitivity and efficiency. For simplicity, it is assumed that when the pads are properly aligned in optical proximity, the received signal power is the same as for capacitive PxC.

Figs. 9 and 10 show SNR versus chip separation and lateral misalignment for the three PxC methods with a pad size fixed at $30\ \mu\mathrm{m} \times 30\ \mu\mathrm{m}$. In Fig. 9, the ideal case for capacitive and inductive communication represents zero transistor mismatch. For the nonideal case a 10 mV transistor mismatch is assumed—which makes the SNR fall monotonically as the chip separation (distance between the transmitter and receiver pads) is increased. In the case of optical proximity communication, as the gap increases the optical beam walks off the mirror for a 54.7° facet. This is not the case for a 45° reflecting facet. Silicon micro-machining typically produces an angle of 54.7° as opposed to the more ideal case of a 45° reflector. In the latter, the exact position of the pit relative to the ball and alignment pit creates coupling conditions that are independent of z or chip gap whereas for the 54.7° reflector the beam walks off the pit for different chip gaps. A more detailed analysis and experimental evaluation of the coupling loss versus gap is provided in [10]. Based on that analysis, two cases are considered here: the ideal 45° case with no walk-off and the 54.7° case where beam walk-off prevents the optical signal from being captured by the optical receivers and hence degrades the received optical signal. While calculating the effects of misalignment along a particular dimension it is assumed that the other dimensions are properly aligned.

From Fig. 9, one can see that when the chip separation increases, inductive PxC SNR falls off quickly compared to capacitive PxC for small pad sizes. This is also true for large lateral misalignment, as shown in Fig. 10. In Fig. 11, the SNR for capacitive and inductive PxC is drawn for a constant separation of 10 μm, showing a stronger dependence of SNR versus pad size for inductive versus capacitive PxC. It turns out that the tolerance to misalignment and chip separation is inversely dependent on the cubed power of pad-size for inductive PxC, but reduces only linearly with pad-size for capacitive PxC. One conclusion is that there is a minimum voltage limit for inductive PxC to maintain a constant BER as pad sizes are reduced. Later in this section, Table I provides general analytical approximations that can be use to quantify these dependencies for arbitrary pad sizes and chip separation. The modeling shows that optical proximity is intolerant to in-plane misalignment. However, optical proximity communication can be designed to be tolerant to chip separation by designing the system so that $h = h_0$. But if $h \neq h_0$ and $\theta = 54°$, then at large chip separations, optical

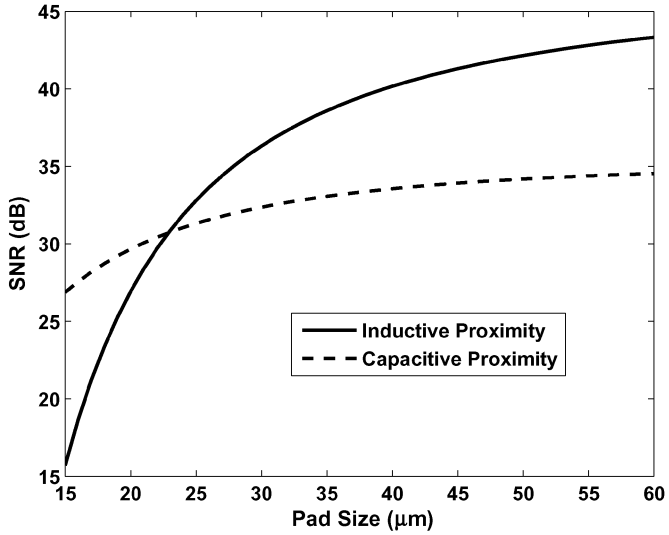

Fig. 11. SNR for Inductive and Capacitive PxC with changing Pad Area. The chip separation is kept constant at 10 μm and supply voltage at 0.7 V.

TABLE I
TABLE SHOWING THE EMPIRICAL FORMULAS FOR SIGNAL AMPLITUDE REDUCTION WITH MISALIGNMENT FOR PADS OF SAME AREA

Parameter	Inductive	Capacitive	Optical
d	$A_i \frac{a^3}{(a^2+d^2)^{1.5}}$	$\frac{\epsilon_{eff} A_c}{(\epsilon_{eff} A_c + C_p d^{1.04})}$	$e^{-(\frac{d}{w_0 tan 2\theta})^2}$
s	$A_i' \frac{(a^2+d_0^2)^{1.5}}{(a^2+d_0^2+s^2)^{1.5}}$	$\frac{\epsilon_{eff} l}{C_p d_0}(w - D_c s)$	$e^{-(\frac{s}{w_0})^2}$

SNR falls off quickly. Note that when $\theta = 45°$, optical PxC can be very tolerant towards chip separation assuming corrections are made to avoid clipping of the received beam. At small pad sizes and small chip gaps, both capacitive and inductive PxC are tolerant towards misalignment.

C. Parameter Space for Constant BER

While designing a communication system, a primary performance criterion is the BER. Here inductive and capacitive proximity methods are compared in terms of achievable BER for various pad sizes. For a constant BER of 10^{-12}, Fig. 12 provides a plot of maximum chip separation versus pad area, assuming a constant voltage swing, for inductive and capacitive PxC. In Fig. 12 it is assumed that the pads are properly aligned in-plane. Curves for two supply voltages are shown, viz. 0.7 V (corresponding to a 45 nm technology node) and 1.2 V (for a 90 nm technology node). One distinct difference between capacitive and inductive PxC is that the performance of inductive PxC can be enhanced by increasing metal layer and thus effectively increasing the number of turns.

Fig. 13 shows the switching energy for capacitive and inductive PxC, at the maximum chip separation, for a fixed area and a BER of 10^{-12}. As expected, the switching energy of capacitive PxC grows rapidly with the pad dimension since the pad capacitance increases quadratically. Although increasing the pad area increases both the capacitance (C_s) and the corresponding inductances (L_t, L_r), the parasitic capacitance C_p increases proportionally, whereas the parasitic capacitance of L_t and L_r do not increase proportionally because the metal area coverage for the inductors is relatively small. Hence, increasing the pad size

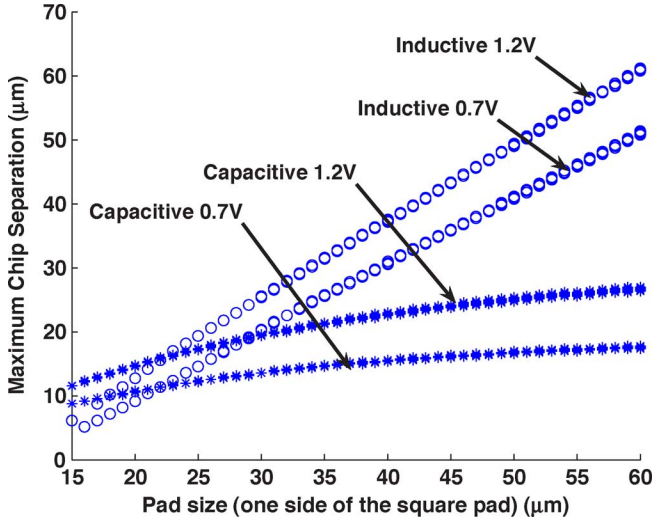

Fig. 12. Maximum chip separation for a BER of 10^{-12} versus pad area for capacitive and inductive PxC assuming the applied voltage swing is fixed. Plots are shown for each communication method for two supply voltages: 0.7 V and 1.2 V. Crosstalk-related penalties are included for both cases.

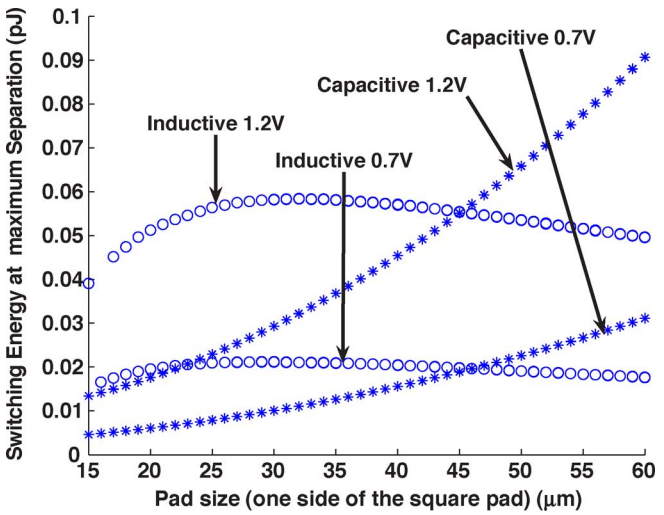

Fig. 13. Switching energy for a BER of 10^{-12} versus at the maximum chip separation (obtained from Fig. 12) versus pad size for capacitive and inductive PxC.

beyond a point becomes an inefficient means of improving the received voltage in capacitive PxC, whereas it continues to be effective for inductive PxC. The switching energy for inductive PxC exhibits less dependence on pad size, and beyond a point, increasing the pad area for inductive PxC reduces the switching energy for a constant voltage. Fig. 14 shows the effect of removing crosstalk on the maximum chip separation for both PxC methods. For capacitive PxC, it is evident that there is a fixed benefit for crosstalk cancellation independent of pad size. This is because the cross-talk voltage is determined by the ratio of the crosstalk capacitance and the parasitic (stray) capacitance, which remains relatively constant. In fact, detailed analysis shows that in capacitive PxC, the effect of cross-talk scales inversely to the square root of the pad area and hence at very large pad sizes, the cross-talk effect is negligible. The benefit of crosstalk cancellation becomes evident for inductive PxC

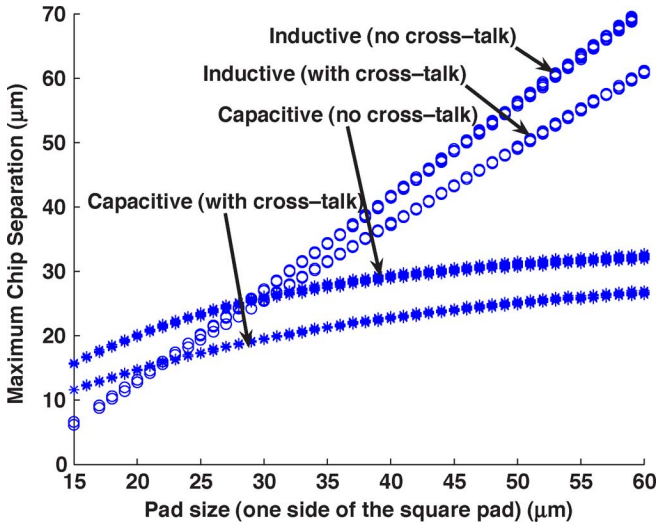

Fig. 14. Maximum chip separation for a BER of 10^{-12} versus pad area for capacitive and inductive PxC assuming the applied voltage swing is fixed for a supply voltage of 1.2 V. Plots are shown with crosstalk-related penalties (same as Fig. 12) and without (assuming crosstalk is perfectly cancelled).

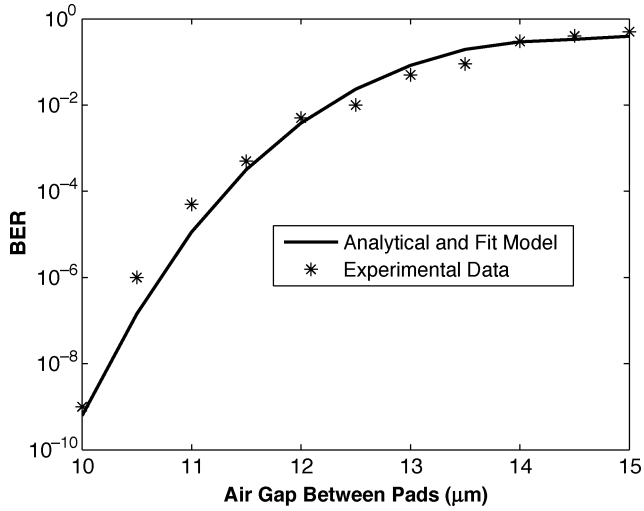

Fig. 15. Figure showing the experimental result [13] and the analytical predictions. Pad Area: $30\,\mu \times 30\,\mu$. Center-to-center distance between two adjacent pads $36\,\mu$m. Parasitic Cap of 45 fF and Supply of 1.8 V. A constant circuit noise of 1 mV, transistor mismatch of 14 mV, and constant angle of 4° is assumed. $a_1 = 1.15$ and $e_1 = 0.8$ is used to fit the data.

for larger pad sizes when the crosstalk-causing mutual inductance becomes significant. From Figs. 12–14, one can conclude that capacitive PxC will perform reliably with low switching energies and hence low per-bit communication energies with the voltage swings available with fine-line CMOS if the chip package can ensure that the effective chip separations (including dielectrics) are kept under a fixed maximum distance—whether or not crosstalk cancellation techniques are used. This limiting distance is dependent on the specific technology parameters, and was found to be in the range of 25–30 μm for the assumed 1.2 V technology parameters (and as low as 15–20 μm for the 0.7 V technology). One of the reasons for the chip separation limit for capacitive PxC is the parasitic capacitance C_p, which scales with area. To overcome this limit, one would need to either increase the voltage supply or to improve the value of the signal capacitance C_s without increasing C_p. One way of accomplishing this could be to use materials with higher dielectric constant (high-K materials) between the capacitor plates [11], [13]. Assuming the packaging challenges [21], [23] can be conquered, capacitive PxC appears to have strong potential for a low power interconnect solution for a multichip module with partially overlapping face-to-face chips. On the other hand, inductive communication can be energy efficient for larger chip separations, but to achieve this it requires a larger pad area or a higher voltage if a low BER is desired. The benefits of inductive PxC relative to capacitive PxC become evident for larger pad sizes since this can provide effective communication over larger distances, and hence could be used for vertically-stacked multichip packages as well as multichip modules. Also the performance of inductive PxC can be enhanced by using multilayers and the performance obtained from a multilayer metallic structure is comparable to capacitive PxC at low pad size (Fig. 12). We also note that inductive PxC can be operated at high bit-rates to achieve a high communication bandwidth-density (similar to capacitive PxC with small pads) since the cutoff bandwidth for inductive PxC is large.

D. Situation With Significant Lateral Misalignment and Chip-Separation

So far it was assumed that only one form of misalignment (chip gap or either x or y misalignment) was present. But in practice, all misalignments simultaneously occur presenting a significant packaging challenge. When the pads are laterally misaligned, both C_s and C_{xt} are affected. C_s for misaligned capacitance has already been modeled. When misaligned, C_{xt} has a parallel-plate component C_{pp} and a fringing component C_{fr}. The way C_{xt} changes depends on a number of factors including the direction and the amount of misalignment, additional circuit-technique to reduce cross-talk, etc. These are difficult to model analytically. Hence, fitting parameters are used to model this situation and the model used is $C_{xt} = a_1(C_{pp} + C'_{fr}(m/l)^{e_1})$, where, C'_{fr} is the fringing capacitance when the plate is totally misaligned, m is the amount of in-plane misalignment, l is length of the pad and $a_1(0 < a_1 < 2)$ and $e_1(0 < e_1 < 1)$ are the fitting parameters. This model is used to explain experimentally observed data [13]. The test chip was fabricated in commercial 0.18 μm CMOS process. Also an electronic alignment correction scheme [22] is applied in the chip to compensate for lateral misalignment.

A steep rise in BER was observed with distance in [13], even though a cross-talk cancellation technique (butterfly differential signalling) was applied. Here, we assume that there was a constant angle along which the plates were separated and hence when vertical separation increased, the plates became laterally misaligned. There is no conclusive proof for the value of the angles, but with reasonable estimates for experimental errors and fitting parameters, our model accurately matches the experimental results (Fig. 15).

E. Empirical Formula and Physical Reasoning

In this section, empirical formulas of received signal amplitude reduction with a chip separation or gap d (out-of-plane misalignment) and an in-plane misalignment (center to center

distance of two pads s) are provided for three methods, assuming same voltage swing is applied to the pads. For optical d is defined as $h - h_0$. Table I shows the formulas for the three proximity communication methods. The constants in the empirical formula depend on dielectric constant, permeability, permittivity and pad area. A_i and A_i' are constants that depend on area of the chip and layout parameters; a is the radius of loop or half of the side for a square inductor; ϵ_{eff} is the effective dielectric constant of the gap between pads; A_c is the area of the pad; C_p is the stray capacitance; d_0 is the vertical distance between two pads after in-plane misalignment is taken into account; w and l are width and length of the pad; D_c is a fitting parameter which takes into account the fringing field dependence (found to be 0.835); θ is the angle of the mirror and w_0 is the light-beam radius at transmitter waveguide.

These empirical formulas are based on approximations of the detailed modeling reported in this paper. The strength of the received signal in inductive coupling depends on the strength of the magnetic field. When the chips are aligned in-plane (i.e., s is small), then the contribution of B_θ is negligible. Hence for out-of-plane alignment, only B_r needs to be used. If the loops are not very large, then it can be assumed that the magnetic field is almost constant over the loop area. Hence the dependence of signal strength with d is given by (7). Similarly when s is small, the dependence is similar. But when s becomes larger, then both B_r and B_θ should be used and simple approximations do not hold.

For capacitive coupling, the dominant component of the proximity capacitance is due to parallel plate capacitance. Hence the dependence on chip separation physically should be of the order of d^{-1}. In practice, the coupling depends on the cross-talk as well as fringing capacitance and the exponent is determined by a best-fit. For lateral misalignment, when considering just the parallel plate part of capacitance the dependence is proportional to s. However, the fringing fields are not much affected by misalignment hence the proportionality factor is reduced and again determined by a best-fit.

For the optical proximity communication model considered here, the broadening of the beam-profile does not significantly affect the coupling. In fact, at a distance of several wavelengths the beam is not broadened significantly (i.e., $w_R \approx w_0$). Hence for both types of misalignment, the empirical formula depends on the horizontal misalignment and the exponential dependence follows from (15) (provided there is no clipping of the signal). If h becomes large, then the derived formula fails to correctly predict the received signal.

VIII. Discussion

In this paper, three promising physical proximity chip-to-chip communication (PxC) methods (viz., capacitive, inductive and optical) are analytically modeled. In each case, a circuit-independent physical view of the communication method is created and examined for its tolerance to packaging and signaling non-idealities. Particular emphasis is placed on capacitive PxC, where the variation of capacitance with physical parameters is explored and new formulas, based on physical reasoning, are developed. Assumptions of transistor mismatch, noise, and crosstalk consistent with the intended use of the communication methods are inserted into the model, and compared to experimental data where available. The analytical solutions show good agreement with experimental data. BER models are validated when cross-talk cancellation techniques were employed. Conditions for effective crosstalk cancellation for capacitive PxC are discussed and supported by experimental data. Simplified "rule-of-thumb" formulas are proposed for all three PxC methods to model signal degradation versus in-plane and out-of-plane misalignment. The design space in terms of the minimum pad size and the maximum chip separation for capacitive and inductive proximity communication is explored for a given bit-error rate while keeping the transmitted voltage constant. Similarly, the per-bit switching energy at the maximum chip separation as a function of pad size is explored for various transmitted voltages. The relative merits and optimum operating conditions of each technology are discussed.

A general conclusion is that capacitive proximity communication is advantageous for chip-to-chip communication with small pads at low voltages and low switching energy, when low bit-error rates are required. These conditions are typically valid with fine line-width CMOS technologies and represent an important application target for dense chip-to-chip digital communication links. However, chips must be placed face-to-face and a hard requirement for vertical separation between chips is imposed—even if the crosstalk is removed by the use of appropriate circuit techniques. The requirement to maintain a signal-to-noise requirement for a given BER drives this limit. It turns out that this limiting value is not dependent on pad size but dependent only on the specific technology parameters. The reason is that the parasitic (stray) capacitance also scales with area and hence increasing pad size cannot alone suffice. To overcome this limit, one would need to either increase the voltage supply or improve the value of the capacitance without increasing the stray capacitance. Nevertheless, this result is encouraging since the dual benefits of very low energy and high density chip-to-chip signaling can be simultaneously obtained.

In contrast, inductive proximity communication exhibits a strong dependence on pad size and technology parameters. The benefits of inductive communication are that it can provide a larger working range of chip separations (by increasing pad size), potentially higher speed, and flexible chip configurations (face-to-face or stacked chips face up), and is found to be advantageous from a transmitter power perspective when larger pad sizes are used. However the benefits of relaxed chip separations constrain the minimum voltage requirement in order to maintain low bit-error rates. The advantages of inductive communication can be extended to smaller pad sizes and lower voltages if the requirements on the raw bit-error-rates of the link are relaxed. Optical proximity communication has the most stringent requirements on lateral (in-plane) alignment, but can potentially provide the largest working range of chip separations if appropriate measures are taken to provide beam shaping and beam-steering. Other benefits of the optical channels are its ability to extend the reach of the interconnect significantly beyond the chip-to-chip scale, and to support wavelength division multiplexing as a means of providing bandwidth aggregation or routing functionality. The power requirements of the optical proximity methods

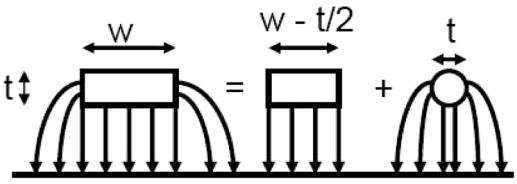

Fig. 16. Model for the field of a parallel plate capacitor using a decomposition into a rectangular plate and a cylindrical wire.

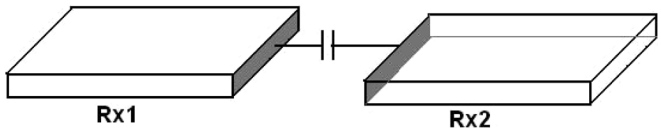

Fig. 17. The shaded faces form the parallel plate capacitance. In this case, the capacitance is formed by the facing sides of the plates, so the thickness of this parallel plate capacitance is more than its width.

are currently higher than other forms of proximity communication, but these are currently being aggressively reduced by several groups and will be considered in future work.

APPENDIX A
DERIVATION OF CAPACITANCE

A. Modeling of Capacitance

It is a well-known fact that capacitance per unit length between a conducting cylindrical wire (of radius a) and a ground plane (situated at a distance d from the center of the wire) is $2\pi\epsilon/log_e((d+\sqrt{d^2-a^2})/a)$, where $\epsilon = \epsilon_0\epsilon_r$ and the space is filled with a dielectric of dielectric constant ϵ_r. Fringing field lines of a rectangular micro-strip line over a ground plane can be modeled as field lines due to a cylinder as shown in Fig. 16. If the infinite ground plane is replaced by a finite plate, then the fringing field can be modeled as field-lines due to a ground plane placed in between two plates. The capacitance due to fringing will then be half of the capacitance for fringing between one plate and the ground plate placed in middle. By this argument, the formula in [15] is modified to get the capacitance (C) between two finite parallel plates [with dimension $w \times l$ and plate thickness t and plate separation d (face-to-face distance)]

$$C = \frac{\epsilon}{d}(w-t/2)(l-t/2) + \pi\epsilon(l+w)f(d/2,t) \tag{17}$$

where $f(d,t)$ is given by

$$f(d,t) = \left[log_e\left(1+\frac{2d}{t}+\sqrt{\frac{2d}{t}\left(\frac{2d}{t}+2\right)}\right)\right]^{-1} \tag{18}$$

This formula does not account for the effect of the four corners of the plates. The capacitance (C_{fc}) due to the four corners can be modeled by a sphere of radius $t/2$ and the contribution of that (though very small and not incorporated in further analysis) is

$$C_{fc} = \pi\epsilon\sqrt{d'^2-4a^2}\sum_n\left(\coth\left[(n+0.5)\cosh^{-1}\left(\frac{d'}{2a}\right)\right]-1\right) \tag{19}$$

where $d' = d + t/2$ and $a = t/2$. This analysis is valid when $w > t/2$. Sakurai [17] also gave a formula for a finite conducting plate over an infinite ground-plane (based on the method of subarea). That formula is modified for two finite plates and the total capacitance (C_{sk}) is then

$$C_{sk} = \epsilon\left[1.15\frac{wl}{d}+1.4(w+l)\left(\frac{2t}{d}\right)^{0.222}+1.03d\left(\frac{2t}{d}\right)^{0.728}\right]. \tag{20}$$

The first term in (20) denotes the parallel plate part of the total capacitance; the second term denotes the fringing due to sides of the plates; and the third term takes into account of four corners. Because (20) matches more closely with the experimental results, the factor of 1.15 is incorporated in the first term in (17).

B. Modeling Cross-Talk Capacitance

As Fig. 3 shows there are two sources of cross-talk. The first one (C_{xt1}) is due to the fringing fields emanating from one side (here length) of the transmitter and not captured by the receiver plate above it. This implies the fringing capacitance will be the difference of fringing (due to the length of the transmitter as here it is assumed the pads are placed in a $1-D$ array) between two situations: when the receiver is infinite and when it is of same size of the transmitter. Mathematically this is given by

$$C_{xt1} = \pi\epsilon l\left(f(d,t) - 0.5f(d/2,t)\right). \tag{21}$$

If the pads are placed in a $2-D$ array fashion, then

$$C_{xt1} = \pi\epsilon(l+w)\left(f(d,t) - 0.5f(d/2,t)\right) \tag{22}$$

The second one (C_{xt2}) is a parallel plate capacitor formed between two adjacent receivers. It is to be noted that the finite thickness t of the plate mainly contributes to C_{xt2}. In all the analytical results reported in this paper, this thickness is kept at 1 μm. The two faces that produce the capacitance C_{xt2} (shaded faces in Fig. 17) are of area $t \times l$, thickness w and face-to-face gap $p-w$ where p is center to center distance between two adjacent pads. We note that C_{xt2} is due to two parallel plates which are facing each other laterally and the plate thickness w is larger than the width t of the face and hence a different formula (after modifying for finite plates) [15] is used

$$C_{xt2} = \epsilon\left[\frac{tl}{(p-w)} + Af\left((p-w)/2,w\right) + 1.47l\right] \tag{23}$$

where

$$A = 0.5\pi(t+l)\left(1-0.0543w/(p-w)\right). \tag{24}$$

The field lines from a receiver plate will be shared between the plate (corresponding transmitter) below it and the adjacent receiver plate in-plane. Hence in practice C'_{xt2} should be modeled as

$$C'_{xt2} = C_{xt2}\left(\frac{d}{p-w+d}\right). \tag{25}$$

This formula is heuristically calculated arguing for a physically meaningful result at the limiting cases.

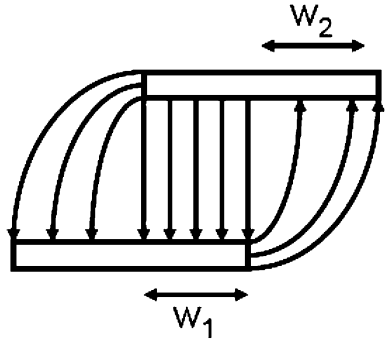

Fig. 18. Field lines when the plates of the capacitor are misaligned.

C. Modeling Misalignment

The capacitance (C_{ma}) between two misaligned parallel plates is difficult to model exactly by analytical methods and needs numerical simulation. Here an approximate analysis is done to estimate the capacitance. The field lines when two plates are misaligned is shown in Fig. 18. Let us assume that the plates are misaligned only in one dimension, say width. Then it can be written $w = w_1 + w_2$, where w_1 is the width of the receiver plate which is overlapping with the transmitter plate. The total capacitance is given by

$$C_{ma} = q\epsilon \left[\frac{w_1 l}{d} + \pi w_1 f(d/2, t) + \pi l f\left(\sqrt{0.25\,(d^2 + w_2^2)}, t \right) \right]. \tag{26}$$

It should be noted that, when $w_2 = 0$, this equation reduces to (1).

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