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Fast and Energy-Efficient Non-Volatile III-V-on-Silicon Photonic Phase Shifter Based on Memristors

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Silicon photonics has evolved from lab research to commercial products in the past decade as it plays an increasingly crucial role in data communication for next-generation data centers and high-performance computing. Recently, programmable silicon photonics has also found new applications in quantum and classical information processing. A key component of programmable silicon photonic integrated circuits (PICs) is the phase shifter, traditionally realized via thermo-optic or free-carrier effects that are weak, volatile, and power hungry. A non-volatile phase shifter can circumvent these limitations by requiring zero power to maintain the switched phases. Previously non-volatile phase modulation is achieved via phase-change or ferroelectric materials, but the switching energy remains high (pico to nano joules) and the speed is slow (micro to milliseconds). Here, a non-volatile III-V-on-silicon photonic phase shifter based on a HfO_2 memristor with sub-pJ switching energy (≈400 fJ), representing over an order of magnitude improvement in energy efficiency compared to the state of the art, is reported. The non-volatile phase shifter can be switched reversibly using a single 100 ns pulse and exhibits excellent endurance over 800 cycles. This technology can enable future energy-efficient programmable PICs for data centers, optical neural networks, and quantum information processing.

1. Introduction

The silicon photonic phase shifter is a fundamental building block of programmable photonic integrated circuits (PICs).[1–3] For certain applications such as electro-optic modulators, the phase shifters need to operate fast and are generally achieved by free-carrier dispersion[4] or electro-optic effect,[5,6] which are ultra-fast but the extent of index change is small. On the other hand, applications such as light routing between functional devices and post-fabrication trimming, do not require high speed but need large changes in index. These functionalities are traditionally achieved using thermo-optic effects[7] and micro-electro-mechanical systems (MEMS).[8] A major limitation of all these methods is their volatile nature – a constant power (≈mW) or bias (>20 V) must be applied to maintain the switched states. For programmable photonics, it is highly desirable to have non-volatile phase shifters that require zero[9,10] or minimal power[11] to maintain the switched states, and the information is retained when the bias is removed. For example, non-volatile phase shifters based on phase change materials[9,12] are very compact and allow true “set-and-forget” operation, but they require relatively high switching energy (≈nJ) and suffer from slow switching speed (≈hundreds of ns to μs). The high temperature (≈900 K) required to switch the phase change materials can also have reliability concerns. Non-volatile ferroelectric phase shifters based on Barium Titanate[11] can achieve multilevel operation and low loss, but the electro-optic effect is weak, and the switching speed is even slower, requiring 10^4 pulses with a total duration of hundreds of microseconds for initializing the states. Although MEMS are shown to exhibit a non-volatile effect and have a compact footprint (L_π≈17 μm), they require large driving voltage (>20 V) and the switching time can take up to a few seconds imposed by the slow I-V sweep[13] to achieve adhesion latching. Lastly, plasmonic memristor switches have been demonstrated to exhibit the latching effect,[14,15] but the high insertion loss (≈10 dB) from the metal absorption makes it prohibitive for cascaded phase shifters. Previously III-V-on-silicon photonic phase shifters have been demonstrated for applications in high-speed modulators,[16,17] but they are based on volatile effect (i.e., free carrier dispersion) so are not ideal for programmable PICs that only require infrequent update of phase states. Table S1 (Supporting Information) presents a comparison of non-volatile programming technologies in PICs. Here, we demonstrate a non-volatile phase shifter

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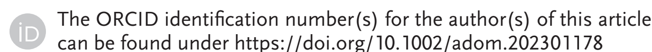
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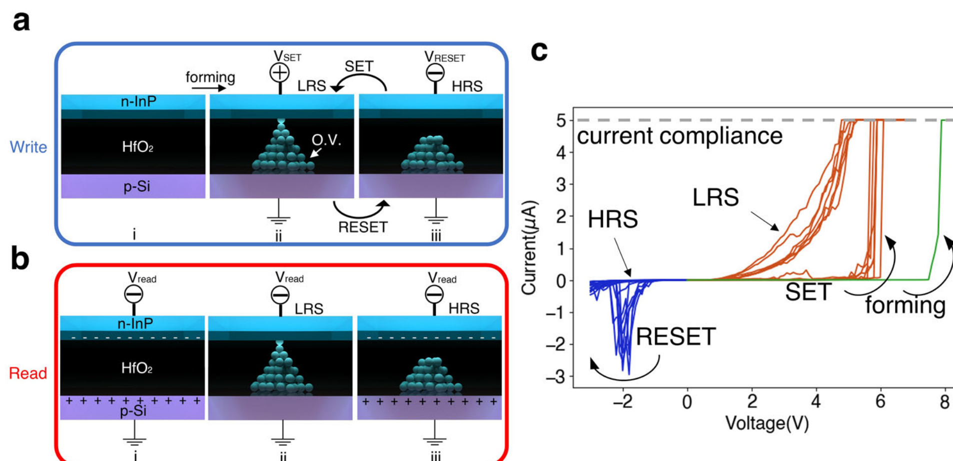

Figure 1. Written and read states in a III-V-HfO_2-Si memristor. a) Schematics illustrating how the states in InP-HfO_2-Si memristor are written. HRS (LRS), high resistance state (low resistance state). O.V. (oxygen vacancies). b) Schematics showing reading the InP-HfO_2-Si memristor at states shown in (a). A constant negative read bias is applied to the n-InP in (i, ii, and iii). c) Current-voltage relationship of the forming (green), SET (orange), and RESET (blue) operations. The voltage is the write bias. The grey dash line indicates the 5 μA current compliance to prevent device damage. Seven I-V SET and RESET cycles are plotted on top of each other to show good cyclability.

on the III-V-on-silicon heterogeneous platform enabled by the memristor effect.[18–21] The non-volatility arises from resistively switching the InP-HfO_2-Si memristor between high-resistance-state (HRS) and low-resistance-state (LRS) using a single 100 ns long voltage pulse. The phase shifter exhibits a switching energy as low as ≈400 fJ, representing over an order of magnitude reduction compared to the state-of-the-art,[9,11] and an excellent endurance of over 800 cycles. Moreover, the III-V-on-silicon heterogeneous platform is fully compatible with foundry processes,[22] potentially enabling seamless integration with laser sources and the energy-efficient large-scale programmable PICs.

2. Working Principle of the III-V-HfO_2-Si Memristor

The memristor is based on the heterogeneous integration between III-V n-type InP and p-type silicon sandwiching a high dielectric constant HfO_2,[20,23] see **Figure 1**a(i). In Figure 1a(i), the memristor is in its as-fabricated state, and applying a negative bias V_{read} on the n-InP while keeping the p-Si grounded (i.e., forward bias) will cause carrier accumulation at the oxide-semiconductor interface (Figure 1b(i)), which essentially operates as a MOS (metal-oxide-semiconductor) capacitor. On the other hand, if a large enough positive bias is applied, oxygen vacancies (O.V.) diffuse inside the oxide layer and, at a certain threshold, a conduction filament (CF) consisting of oxygen vacancies is formed[24] (see Figure 1a(ii)). Such process is termed "electroforming" and can be visualized in Figure 1c green line where the current suddenly increases at ≈7.5 V and hits the current compliance enforced by the source meter. The voltage in Figure 1c is the bias applied to the n-InP. After forming, the memristor is switched into the LRS, and the MOS capacitor effect is suppressed due to the charge leakage. This is reflected in the Figure 1b(ii) where the forward bias no longer causes carrier accumulation. To return the memristor to HRS, a bias with opposite polarity (i.e., negative) is applied to the n-InP that causes Joule heating and the retraction of oxygen vacancies, eventually giving rise to the rupture of the CFs. The operation is called RESET and is revealed by blue lines in Figure 1c, where the current rapidly increases to ≈2.5 μA at ≈ −2 V before collapsing to near zero. Since Joule heating depends on the power, if the CFs rupture was only caused by the Joule heating, then we would have seen the CFs rupture during the voltage ramp down after the CFs form as a higher power is measured (Figure 1c orange lines). The absence of filament breaking at positive bias shows that the RESET operation is a compound phenomenon of both field effect and Joule heating that enables the switching at a lower voltage than the SET.[25] Reversing the polarity causes the retraction of oxygen vacancies which facilitates the rupture of the filaments. Indeed, electrochemical migration of oxygen vacancies has been regarded as the driving mechanism behind bipolar switching where the SET and RESET polarities are opposite.[26] The rupture of the CFs brings the memristor back to the HRS and the MOS capacitor effect is restored (Figure 1a(iii) and b(iii)). The memristor can then be switched to the LRS again by applying a positive bias to the n-InP but at a lower voltage (5–6 V), as shown by the orange lines in Figure 1c. This is because the CFs do not rupture completely during RESET (Figure 1a(iii)) and fewer oxygen vacancies need to be displaced by the field to re-connect the CFs. Figure 1c shows that SET and RESET operations are repeated for seven consecutive cycles between HRS and LRS.

3. A Memristor-Based III-V-on-Silicon Heterogeneous Photonic Platform

The ability to switch a MOS capacitor on and off using a memristor provides a way to realize non-volatile phase tuning in a microring resonator by controlling the carriers in the accumulation layer formed at the waveguide (**Figure 2**a). Thus, the optical modulation happens via the free-carrier dispersion effect, while the non-volatility comes from the memristor controlling the MOS capacitor, which in turn controls the ability to form an accumulation layer of free carriers. The 250 nm tall, 1.2 μm wide silicon waveguide is formed by partially etching to a 100 nm slab on one side and fully etched to the buried oxide (BOX) on the other side. A

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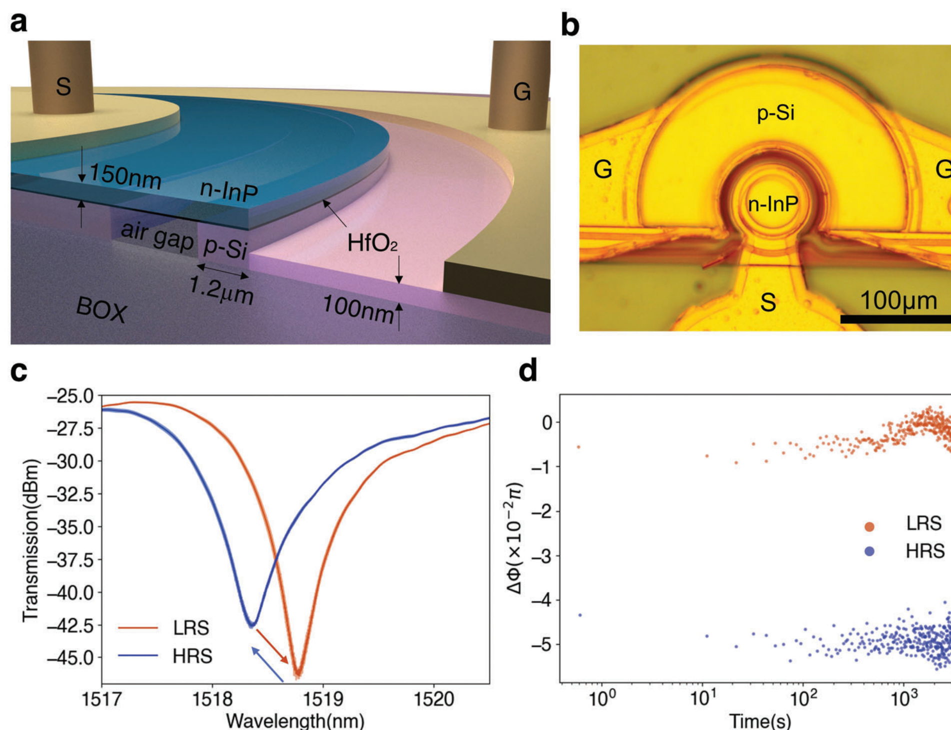

Figure 2. Non-volatile phase tuning of microring resonator using memristors. a) Schematic of the memristive microring MOS capacitor modulator. BOX stands for buried oxide. S (G), signal (ground) electrode. b) Optical micrograph of the microring. c) Reversible switching of microring resonance using memristors. The switching conditions are 7 V, 200 ns pulse width, 8 ns trailing edge for SET and −3 V, 200 ns pulse width, 8 ns trailing edge for RESET. Three consecutive cycles are plotted where the shaded area indicates the standard deviation between the cycles and the solid line indicates the average. d) Time stability test over 1 h of the SET and RESET phase states. The optical spectrum is measured every 10 s to calculate the resonance wavelength. ΔΦ denotes the optical phase shift. A constant −3 V bias at 100 nA current compliance is applied to read the optical states in the above measurements.

150 nm n-InP epitaxial layer is transferred to the silicon layer via a standard wafer bonding technique[27] with 9.6 nm thick HfO_2 as the interface oxide[23] (see Experimental Section for fabrication details). The HfO_2 acts simultaneously as a gate oxide that forms an MOS capacitor with the Si and InP and a memristor switching layer. The air gap is left in the Si layer to confine the MOS capacitor to the fundamental TE mode area in the Si waveguide and hence reduce the total capacitance for a fast electro-optic response.[28] Figure 2b shows the fabricated microring resonator integrated with the memristor. The SEM and TEM images of the heterostructures were reported in our previous work based on the same batch of devices reported here.[23] In the as-fabricated state, the memristor is in the HRS and the negative read bias causes carrier accumulation at the oxide-semiconductor interfaces (Figure 1b(i)). The effective index of the optical mode in the Si waveguide underneath therefore changes by the free carrier dispersion effect which in turn leads to an optical phase shift. Setting the memristor to the LRS leads to the formation of CFs (Figure 1a(ii)) and hence the read voltage can no longer cause carrier accumulation due to the charge leakage (Figure 1b(ii)), and the free carrier induced phase shift is turned off.

Figure 2c shows the reversible switching of a 10 μm radius microring resonator between LRS and HRS states for three consecutive cycles using the device structure shown in Figure 2a,b. Pulses are used instead to switch the memristors, allowing faster operation[29] compared to the I-V sweep. The shaded regions of the spectra indicate the standard deviation between the three switching cycles, clearly revealing excellent cycle-to-cycle reproducibility. A constant read bias of −3 V and current compliance of 100 nA are applied when taking all the optical measurements in this work unless otherwise stated. The resonances at zero read bias for both the SET and RESET states are shown in Figure S1 (Supporting Information). In the LRS, the MOS capacitor is off and −3 V read bias only induces a minimal blueshift (see Figure S1, Supporting Information). As the memristor is reset into the HRS, the MOS capacitor is turned on and a blueshift of 0.44 nm is observed under the constant −3 V read bias, corresponding to a phase shift of 0.09π for a phase shifter length of 47 μm. The L_π is hence estimated to be ≈0.5 mm – half the length of a ferroelectric-based non-volatile phase shifter.[11] The insertion loss introduced by the carrier dispersion is only 0.28 dB or 0.006 dB μm^{-1}, which is comparable to chalcogenide PCMs.[9] We further show in Figure 2d that the phase tuning is indeed non-volatile by monitoring the resonance wavelengths over 1 h at a −3 V read bias. The two-phase levels remain stable over time, with only minimal drift due to the temperature fluctuations, which indicates that the charge leakage is negligible. Section S4 (Supporting Information) shows that the resonances measured after 24 h overlap perfectly with the original spectrum for both the SET and RESET states. However, charge leakage will be an issue for analog operation where charge will leak at the intermediate states and eventually return to the original state. In this case,

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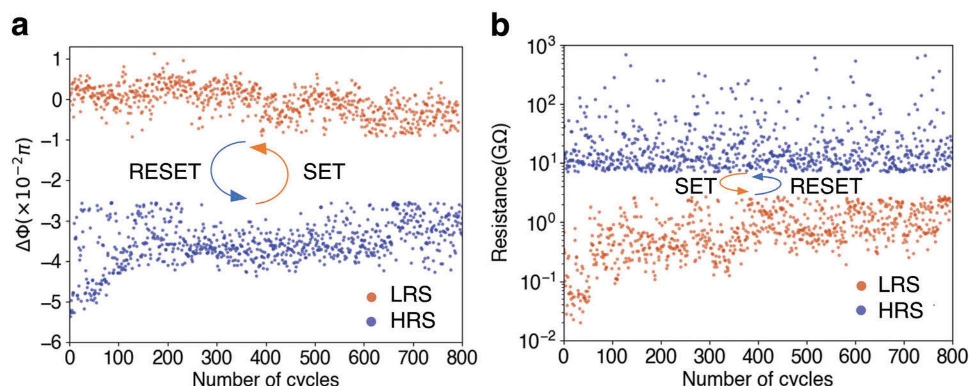

Figure 3. Endurance of the memristor-based non-volatile phase shifter. a) Cyclability of the phase shifter for 800 consecutive cycles or 1,600 switching events. The switching conditions are 15 V, 100 ns pulse width, 8 ns trailing edge for SET and −3 V, 100 ns pulse width, 8 ns trailing edge for RESET. $\Delta\Phi$ denotes the optical phase shift. b) Simultaneous resistance readout of the memristor switching measured at −0.7 V read bias over the 800 cycles. The pulse conditions are the same as in (a).

the phase shifter must operate in a carrier injection mode where the phase shift is controlled by the current injection, but at a cost of increased free carrier absorption and power consumption.

Device endurance is a key metric in assessing the durability of any non-volatile phase shifter. Here, we performed over 800 cycles or 1,600 transitions on the phase shifter without significant degradation in the performance, see **Figure 3**a. The experimental setup and procedure are detailed in Experimental Section. The failure mechanism of the phase shifter is discussed in Section S5 (Supporting Information). A phase shift of $\approx 0.03\pi$ can still be measured after 800 cycles. Meanwhile, in the electrical domain, the current is also monitored in each cycle to estimate the resistance. An HRS/LRS ratio of 10× is measured across the 800 cycles where both LHS and RHS exhibit a high resistance of >1 GΩ, indicating minimal leakage current (<1 nA) under the read bias. The good match between the endurance in optical and electrical domains verifies that the non-volatile phase tuning indeed originates from the memristor switching. Since both states exhibit high resistance (i.e., low switching current ≈μA) and the switching time is short (≈100 ns), we extract a low switching energy of 1.3 pJ for SET and 0.4 pJ for RESET (see Section S2, Supporting Information, for the estimation of switching energy) by averaging across multiple devices, representing over an order of magnitude reduction in switching energy compared to the state of the art.[9,11] Such low switching energy is an intrinsic advantage of memristor – since the CFs responsible for the switching are only nanometer scale,[30] minimal current (≈μA) and time (100 ns) is required to form and break the filaments. In comparison, PCMs typically require nano-joules to switch due to the micro-scale size.[9,10] The lower RESET energy compared to SET is because the RESET is caused by a compound effect of Joule heating and polarity, as discussed earlier. Flipping the polarity causes the retraction of oxygen vacancies, so the RESET pulse requires lower voltage and hence smaller amount of current to rupture the filaments. Fundamentally speaking, the memristor switching does suffer from one to two-order magnitude variation in resistance,[29] which was also observed in Figure 3b, due to the stochasticity in the formation of conduction filaments, particularly when there is no current limiting transistor. However, the optical phase shift does not vary as much as the resistance does because we applied a 100 nA current compliance when the optical state was read, which limited how much the phase shift could vary. Since we are showing a photonic phase shifter, the variation in resistance will be irrelevant in actual applications.

Finally, we show that the SET and RESET have sub-microsecond optical response time, see **Figure 4**. The experimental setup for the real-time measurement can be found in Experimental Section. Note that a constant read bias of −2 V is applied to the Signal during the switching to make sure there is a measurable contrast from the non-volatile switching. Notably, a single 100 ns pulse is enough to trigger both the SET and RESET, compared to hundreds of microseconds required for PCMs[9,10] and milliseconds for ferroelectric materials.[11] We define the time when the optical transmission starts to change significantly upon the electrical pulse as the onset of the optical response and the time when the optical response goes to T_0 as the end of the optical response (see Figure 4). For SET, the pulse starts at −30 ns, and the optical response restores to T_0 at ≈400 ns, so the total response time is ≈430 ns. For RESET, the onset of the optical response is −18 ns, and the optical response restores to T_0 at ≈118 ns, so the total response time for RESET is ≈136 ns. The different response times and dynamics come from the distinct physical effects responsible for SET and RESET in a memristor. When setting the memristor, carrier depletion happens first due to the reverse bias (see Figure 1b(ii)) and then carrier injection quickly follows once the CFs form. However, since the MOS capacitor is already in the carrier-depleted state at zero bias, further carrier depletion hardly gives any optical change. In fact, the slower "spike" optical response and long relaxation time observed in Figure 4a are caused by the carrier injection along with the slow thermo-optic effect after the formation of CFs, which is a typical signature of a PIN diode[31] at high current injection. The non-volatile switching is visualized by a permanent change in optical transmission after the transient effect dies out, indicated by the black dash line. On the other hand, when resetting the memristor the optical response changes almost simultaneously with the voltage pulse without any delay or relaxation due to the rapid carrier accumulation (Figure 4b). The fast response is a signature of the carrier accumulation effect where GHz speed has been measured in the MOS capacitor modulator.[16] The change of

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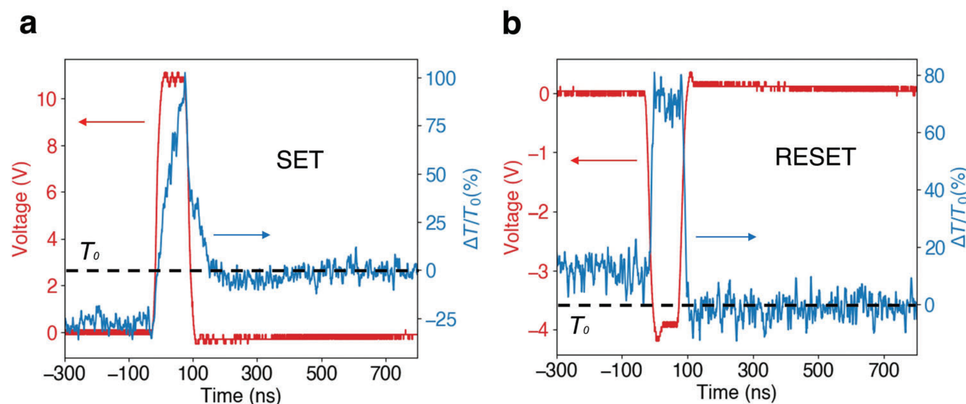

Figure 4. Real-time optical switching response of the phase shifter. a) Dynamics of the SET operation together with the voltage pulse that triggers the switching. *T* is the transmission at the microring through port. The black dash line indicates the optical state after the transient effect dies out. The pulse conditions are 11 V, 100 ns pulse width, 8 ns trailing edge. b) Dynamics of the RESET operation and the voltage pulse that triggers the switching. The pulse conditions are -4.5 V, 100 ns pulse width, 8 ns trailing edge. A constant −2 V read bias is applied in both SET and RESET which is not shown in the figure.

dynamics from a typical carrier injection to a carrier accumulation response clearly shows that the non-volatile optical switching is caused by the memristor. It is worth noting that the filament formation in fact occurs at the onset of the voltage pulse (Figure 4a), implying that sub-nanosecond switching is possible which has been reported in electronic memristors.[32]

4. Conclusion

To summarize, we have demonstrated a non-volatile III-V-on-Si phase shifter with ultra-low switching energy (≈400 fJ) and fast response time (≈100 ns). The non-volatile phase shifter also has an excellent endurance of over 800 cycles or 1,600 transitions. The superior performance is made possible by the well-studied electronic memristive effects[18] that have long been explored for non-volatile storage[33] and in-memory computing.[34] Our results show that memristor can be an energy-efficient, fast, and reliable technology to realize non-volatile phase tuning in PICs. Although the current device only operates in a binary fashion, it is already sufficient to realize applications such as on-chip optical routing[35] and LiDAR[36] which only require π phase shifters to switch all light from one port to the other. Binary switching also simplifies the control of the CMOS circuit as no additional digital-to-analog converters (DACs) are required. We believe the device performance can be further improved by adding a transistor to implement fast current compliance during pulsing, also known as the 1T1M (1-Transistor-1-Memristor) configurations.[37] The transistor can prevent current overshoot during the high-voltage SET pulse, which is essential to reduce the possibility of device failure (see Section S4, Supporting Information). Additionally, by controlling the bias applied to the gate of the transistor, different current limits can be implemented which makes analog operation possible.[38] One can also achieve linear analog operation by adding a TaO_x electro-thermal modulation layer in contact with the HfO_2 which can decrease the rate of change of electric field in the CF gap region.[39] The relatively low Q factor of the ring is limited by the high silicon doping (1×10^{16} cm^{-3}) across the entire ring that ensures that most electric field is dropped across the oxide to cause filamentation. The Q factor can be improved in the future by lowering the doping concentration or increasing the bonding oxide thickness, but at the cost of increased switching voltage. Instead of doping the entire ring, we can also dope a section to reduce the loss, but the phase-tuning efficiency will be reduced.

5. Experimental Section

Device Fabrication: The fabrication[28,40] started with a 100 mm diameter SOI substrate with 250 nm thick, lightly p-doped (1×10^{16} cm^{-3}) top Si layer, and 1 µm thick buried oxide layer (BOX). First, a photolithography step defined the heavily doped p++ regions in Si to form an ohmic contact with the metal. The 1×10^{20} cm^{-3} Boron doping level was targeted after the ion implantation process and doping activation annealing at 1050 °C. Then the process of pattern and dry etching was followed through the top Si layer to form the ring-shaped air trench for electrical and optical isolation along with vertical outgassing channels[27] that ensured proper bonding. To produce the interface HfO_2 for bonding, a plasma activation step in dielectric deposition was introduced.[41] Upon depositing ≈4.8 nm HfO_2 on III-V and Si samples in ALD, III-V/HfO_2, and Si/HfO_2 samples were manually bonded together to form the heterogeneous MOS capacitor structure, followed by a 300 °C annealing step. SiO_2 (250 nm) was then deposited to form a hard mask. Microring patterns of 20 µm diameters were then defined by DUV photolithography and transferred down to the SiO_2 hard mask layer, through III-V layers, and finally into the Si layer by a self-aligned sequential dry etch process. This step with a previously patterned air trench in Si also resulted in a 1.2 µm wide Si waveguide underneath the InP (Figure 1a). Another run of photolithography and III-V dry etch were used to remove all III-V material outside the microrings. Metallization to form the terminals on n-InP and p++-Si was followed by a metal lift-off process and a rapid thermal anneal at 360 °C for 30 s. Finally, the wafer was encapsulated by 300 nm thick SiO_2, followed by etching contact via all three terminals and forming thick metal probes to conclude the fabrication.

Experimental Setup and Measurements: The wafer was placed on a thermally stabilized stage (at 20 °C) and optically probed with a vertical fiber setup via grating couplers defined on the wafer. The devices were electrically addressed via GSG RF probes (CascadeMicrotech ACP-40). The optical spectrum was taken by sweeping the input tunable laser (Santec TSL-510) and collecting the output using a photodetector (Newport 884-FC)

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and power meter (Newport 2936-R). The SET and RESET pulses, both with 100 ns pulse width and 8 ns trailing edge, were applied using the HVPGU (high voltage semiconductor pulse generation unit) in the B1500A semiconductor analyzer at the maximum 1 MΩ load impedance. After applying the pulses, the current was read with the SMU (source measurement unit) of B1500A at a bias of −0.7 V to estimate the resistance while the optical spectrum was taken using the TSL and power meter. An automated script was used to find the resonance wavelength that corresponded to transmission minima from the spectrum data. The setup schematics are shown in Section S6 (Supporting Information).

To perform the real-time optical response measurement, the phase shifter was biased at −2 V using the SMU so that carrier accumulation was induced inside the device (see Section S6, Supporting Information). The SET and RESET pulses were applied via the HVSPGU. The output from the grating couplers was amplified by an EDFA and filtered by a wavelength filter. The optical signal from the wavelength filter was detected by a 70 GHz high-speed photodiode (MACOM P-70A) and measured by an oscilloscope.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

B.T. and D.L. conceived the projects. Z.F. led the electrical and optical measurements and wrote the script for the endurance test. B.T. prepared the setup for the experiment and helped with the measurements. A.D. helped with the tool automation and performed wafer-scale device screening. D.L. and X.H. designed and fabricated the memristor-based phase shifters. G.Z. took optical microscope images for the devices. B.T., G.Z., and A.M. supervised the overall progress of the projects. Z.F. wrote the manuscript with input from A.M. and all the authors.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

memristor, non-volatile memory, programmable photonics, silicon photonics

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