Project:
- Automatic Mixed-Signal Circuit Layout Optimization and Regeneration

Goal and main problem (so far):
12/6/02 - Be able to run Extraction, Optimization, Regeneration, and Inductor part of one analog layout example (Adam's VCO). Finish a paper for DAC.
(1) Sweeping line for the VCO takes too long. We will manually remove VIA and retry.

Weekly Progress:
- The longest path finding function to perform minimum possible transistor W/L searching is done.
- Code restructuring from full one-dimensional at a time, into creating constraints for both direction before solve each one is done. This is necessary for synthesis tool integration.
- With Sam & Roy. Loading VCO design into our code. The CS data structure is fine. The sweep line constraint generation takes 2 days already to run. So we'll keep that running and see progress. Start on poly resizing.

Next Week Plan:
- Be able to load VCO and extract netlist + variables.
- Transistor Poly (sides) resizing.
- Obtaining sample "ARSYN" input and output files from KiYoung, and formatting them as required.