MITLL 0.18 µm Low Power FDSOI CMOS Process Design Guide

(version 5.11.mp5, January 2002)

REDACTED VERSION FOR MULTIPROJECT 5

50 years

MIT LINCOLN LAB

MITLL 0.18 µm Low Power FDSOI CMOS Design Guide
(version 5.11.mp5, January 2002)

About this Design Guide

About Version 5.11

This document contains version 5.11 of the design guide for MIT Lincoln Laboratory's 0.18 µm low power FDSOI CMOS process. It is intended for use by Multiproject 5 contributors. Version 5.11.mp5 is a redaction of version 5.11 that includes only those layers which will be used in preparation of the MP5 reticle set.

About the Process

Since the mission of Lincoln Laboratory is focused on research and development, a large number of process modules have been developed. In each MITLL process version, selected modules are combined in a way that optimizes the process for a particular set of applications. Some process steps are common to all process versions; others are rarely used. The most typical process versions are described in the process parameters section. These include a three metal digital process, and an RF-optimized process in which the third metal level is optimized for design of passive components and trench contacts may be formed along MOS gates to reduce series resistance.   Additional modules for experimental technologies such as 3D stacking, deeply-scaled devices, low voltage coefficient capacitors and dual-gate devices are available in other application-specific process versions. The goal of this document is to provide infomation specific to the RF-optimized process version.

Note on Conventions

In this era of deep submicron scaling, it is becoming increasingly common to express feature sizes in terms of nanometers rather than microns. Unfortunately, this often causes difficulty to designers who have EDA tool configurations and legacy data that relate user units to microns. To facilitate design in this process, we have chosen to express all design rule values in terms of microns. However, to aid in quick conversion to nanometers, we also have elected to consistently maintain three decimal places. This convention does not apply to the case of measured values and tolerance parameters, in which the number of decimal places must be reflective of precision. Thickness parameters are consistently expressed in nanometers.

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Process Parameters

In this section, process parameters are presented for the RF-optimized FDSOI process.

Process Description:

RF-Optimized Process Version: Fully-depleted silicon-on-insilator (FDSOI) CMOS process with single-level poly, two interconnect metal levels and one metal level with ILD and metal thicknesses optimized for design of RF passives. Trench contacts may be formed along MOS gates to reduce series resistance. Contacts and vias may be stacked.

This process version may utilize either local or global SOI thinning. *For MP5, the first lot will use global thinning of the SOI to about 40 nm. Subsequent lots may be locally-thinned or planar.*

Note: Electrical parameters are given for devices at 300 K.

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Resistance Parameters:

Parameter	Value
Bulk resistivity (of p-type handle wafer)	
Float zone substrate (RF process version)	~2000 Ω-cm
Silicided silicon sheet resistance: Case I -- For planar process:	
Silicided n+ active sheet resistance	~40 Ω/sq
Silicided p+ active sheet resistance	~30 Ω/sq
Silicided n+ polysilicon sheet resistance	~30 Ω/sq
Silicided p+ polysilicon sheet resistance	~25 Ω/sq
Silicided silicon sheet resistance: Case II -- For locally thinned process:	
Silicided n+ active sheet resistance	~15 Ω/sq
Silicided p+ active sheet resistance	~15 Ω/sq
Silicided n+ polysilicon sheet resistance	~15 Ω/sq
Silicided p+ polysilicon sheet resistance	~15 Ω/sq
Metal sheet resistances:	
Metal 1 sheet resistance	~0.08 Ω/sq
Metal 2 sheet resistance	~0.08 Ω/sq
Top-level metal sheet resistance	
RF process version	TBD

Note: for RF process version, top-level metal parameters are determined on a case-by-case basis.

Contact and via resistances:	
poly contact (0.250 µm x 0.250 µm)	~10 Ω
n+ active contact (0.250 µm x 0.250 µm)	~10 Ω
p+ active contact (0.250 µm x 0.250 µm)	~10 Ω
interconnect metal via (0.300 µm x 0.300 µm)	~2-3 Ω
top-level RF metal via (TBD) (RF process version)	TBD
RF trench contact CONRFG resistance	~0.4 Ω–µm/w_{trench}
where w_{trench} is the lateral width of the trench contact (RF process version)	
Lateral resistance of RF trench contact CONRFG without metal 1 (not recommended)	~0.25 Ω/sq

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Capacitance Parameters:

Parameter	Value
Parameter	**Value**
MOS gate oxide capacitance (C_{ox}) in inversion	6.5 fF/µm^2
Capacitance of active island or poly to handle wafer (C_{box})	
RF process version	86 aF/µm^2

ILD Thicknesses and Interconnect Overlap and Fringe Capacitances (for RF process version):

From Layer:	To Metal 1:			To Metal 2:			To Metal 3:		
	thickness	*area cap*	*fringe cap*	*thickness*	*area cap*	*fringe cap*	*thickness*	*area cap*	*fringe cap*
	nm	*aF/µm^2*	*aF/µm*	*nm*	*aF/µm^2*	*aF/µm*	*nm*	*aF/µm^2*	*aF/µm*
Active	800	45.7	38.0	2430	15.1	35.2	TBD	TBD	TBD
Poly (field)	650	56.5	47.3	2280	16.1	39.7	TBD	TBD	TBD
Poly (on active)	600	61.2	47.9	2230	16.5	39.8	TBD	TBD	TBD
Metal 1	-			1000	36.7	54.1	TBD	TBD	TBD
Metal 2	-			-			TBD	TBD	TBD

Notes on ILD Parameters:

In the tables above, the values for area capacitance are determined using a parallel plate model. The values for fringe capacitance are based on a model in which fringe field lines from one layer terminate on an infinite ground plane on another layer. More accurate capacitance models may be available. Contact MITLL for more information.

The ILD is planarized, resulting in a layout-dependent thickness distribution. Chemical-mechanical polishing (CMP) is most effective when active, poly, and metal features are evenly distributed across the wafer.

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Other Film Thickness Parameters:

Parameter	Value
MOS transistor gate oxide thickness (ellipsometric)	4.2 nm
SOI buried oxide (BOX) thickness RF process version	400 nm
SOI silicon thickness (in channel region)	40 nm
Polysilicon thickness	200 nm
Isolation technology	mesa-etched
Overglass Thickness	750 nm

Structure of Metal Layers (Bottom to Top)
(for RF process version):

Contact Plug Metal
     to active island   Ti:TiN:W (30 nm : 75 nm : 700 nm)
     to field poly   Ti:TiN:W (30 nm : 75 nm : 550 nm)
RF Trench Contact (CONRFG) Metal   Ti:TiN:W (30 nm : 75 nm : 500 nm)
Via Plug Metal
     below top level   Ti:TiN:W (30 nm : 75 nm : 900 nm)
     top level   Ti:TiN:W (30 nm : 75 nm : TBD)
Metal Levels
     below top level   Ti:AlSi:Ti:TiN (40 nm : 500 nm : 40 nm : 50 nm)
     top level   Ti:AlSi:Ti:TiN (40 nm : TBD : 40 nm : 50 nm)

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Tolerance Parameters:

Parameter	Value
Active Island Width	±0.05 μm
Polysilicon Width	±0.02 μm

Dopant Concentration Parameters:

Parameter	Value
p-channel active (CBP) n-type dopant concentration	~ 5 x 10^{17} / cm^3
n-channel active (CBN) p-type dopant concentration	~ 5 x 10^{17} / cm^3

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Subset of MITLL Design Layers for RF Process Version

Layer	GDS No.	CIF Name	Description
ACT	1	ACT	Active Island
ACTF	2	ACTF	Active Island Fill
ACTXPP	3	ACTX	Active Island With Suppressed Sidewall Processing
CBN	4	CBN	n-Channel Body Implant
CBP	5	CBP	p-Channel Body Implant
POLY	9	POLY	Polysilicon
POLYF	10	POLF	Polysilicon Fill
NSD	12	NSD	n+ Implant (Degenerate Doping)
PSD	13	PSD	p+ Implant (Degenerate Doping)
CON	15	CON	Contact Cut (Metal 1 to Active or Poly)
CONRFG	16	CRFG	Low Series Resistance Contact to Gate for RF
M1	17	M1	Metal 1
M1F	18	M1F	Metal 1 Fill
V12	19	V12	Metal 1 / Metal 2 Via
M2	20	M2	Metal 2
M2F	21	M2F	Metal 2 Fill
VTLRF	31	VTRF	Via to top-level metal modified for RF designs
MTLRF	32	MRF	Top-level metal modified for RF designs
MTLRFF	33	MRFF	RF-modified Top-level metal fill
OGC	34	OGC	Overglass Cut
NOSLOT	50	XSLT	Flag to Suppress Generation of Active Slots
NOFILL	51	XFIL	Flag to Suppress Generation of Fill Structures
RED	58	RED	Comment Layer
GREEN	59	GRN	Comment Layer
BLUE	60	BLUE	Comment Layer

Total Layout Design Layers: 25

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Important Notes:

Layout Submission Requirements

A number of requirements must be met if a layout is to be accepted by MITLL for inclusion on a multiproject run. **MITLL will reject non-compliant layouts.** See the "Layout Acceptance Rules" section of this guide for details.

Planar and Locally Thinned Process Versions

The FDSOI devices in this process require a silicon island thickness of about 40 nm. These thin silicon regions may be formed by either global or local thinning, depending on the process version. In local thinning, only the silicon under the gate of a device is thinned to 40 nm, leaving thicker silicon available in the contact regions. For locally-thinned process versions, the NOSLOT layer is used to suppress the automatic generation of features corresponding to locally-thinned silicon. See the "Design Notes and Examples" section of this guide for more details. *Note: For MP5, the first lot will use global thinning of the SOI to about 40 nm. Subsequent lots may be locally-thinned or planar.*

Feature Bias

Minimum width (0.18 μm) poly features are drawn at 0.200 μm. Exposure and etch bias will produce 0.18 ± 0.02 μm poly lines.

To avoid formation of parasitic edge transistors, layout data will be post-processed by MITLL to allow for sidewall implants. This operation will create the required sidewall implant mask layers, and will adjust the size of active islands slightly to ensure that MOS channel widths correspond to the drawn data. Active island features are bloated by 0.075 μm per side during sidewall post-processing. See "Layout Post-processing for Sidewall Implants" in the "Design Notes and Examples" section of this guide for more information.

Fill Patterns

The design layer section above includes eight fill layers: ACTF, POLYF, M1F, M2F, M3F, M4F, M5F, and MTLRFF. These are for inclusion of fill patterns on active, poly and metal layers to achieve the required feature densities. These layers will be logically ORed with ACT, POLY, M1, M2, M3, M4, M5, and MTLRF, respectively, before physical masks for these layers are generated. These layers should only be used for fill features that do not contribute to the circuit topology of the design.

Submitted layouts will be post-processed to create patterns of floating rectangles to fill unoccupied regions on each active, poly, and metal level. The output of this automatic generation routine will be made available to the designer upon request. To suppress this automatic fill

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generation, the NOFILL layer is provided. Note that submitted layouts that use the NOFILL layer must be compliant with layer density specifications. Density violations may affect other designs on a multiproject die, and hence it is the policy of MITLL to reject any layout that contains unapproved density rule volations.

See the "Design Notes and Examples" section of this guide for more details.

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Lithography Steps for RF Process Version with Local Thinning

| Step	Reticle	Related Design Layers	Description	Field
1	Slot Definition	ACT, POLY, NOSLOT	Defines locally thinned regions	Dark
2	Active Area	ACT, ACTF, ACTXPP	Defines silicon islands	Clear
3	n-Channel Sidewall Implant	ACT, POLY, CBN, CAPP	Implant n-channel island sidewalls	Dark
4	p-Channel Sidewall Implant	ACT, POLY, CBP, CAPN	Implant p-channel island sidewalls	Dark
5	n-Channel Body Implant	CBN	n-channel threshold adjust implant	Dark
6	p-Channel Body Implant	CBP	p-channel threshold adjust implant	Dark
			(gate oxide growth)	
7	Polysilicon	ACT, POLY, POLYF	Defines polysilicon gates and interconnect	Clear
8	n+ Implant Mask (NSD)	NSD	Implant n-channel drift regions	Dark
9	p+ Implant Mask (PSD)	PSD	Implant p-channel drift regions	Dark
			(sidewall spacer formation)	
10	n+ Implant Mask (NSD)	NSD	Implant n+ degenerate regions	Dark
11	p+ Implant Mask (PSD)	PSD	Implant p+ degenerate regions	Dark
			(second spacer formation, salicide formation)	
12	Contact Cut	CON	Defines contacts to active and poly	Dark
12.1	RF Gate Contact	CONRFG	Define low series resistance contact to gate	Dark
13	Metal 1	M1, M1F	Defines first-level metal interconnect	Clear
14	Via 12	V12	Defines metal 1 / metal 2 vias	Dark
15	Metal 2	M2, M2F	Defines second-level metal interconnect	Clear
16	VTLRF Via	VTLRF	Defines metal 2 / RF metal 3 vias	Dark
17	RF Metal 3	MTLRF, MTLRFF	Defines third-level RF metal	Clear
18	Overglass Cut	OGC	Defines pad openings in overglass	Dark

Total Photolithography Levels: **19**
Total Reticle Count: **17**

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In order to facilitate a concise presentation of the design rules, the following terms will be used:

MOS channel region -- The intersection of poly (POLY) and active (ACT) inside either CBN or CBP. Exception: Where one side of a poly line receives NSD implant and the other receives PSD implant, that length is excluded from the MOS channel region. This excluded region is seen in body-contacted device layouts.

☐	Active
■	Polysilicon
▨	MOS channel region
▨	NSD
▨	PSD
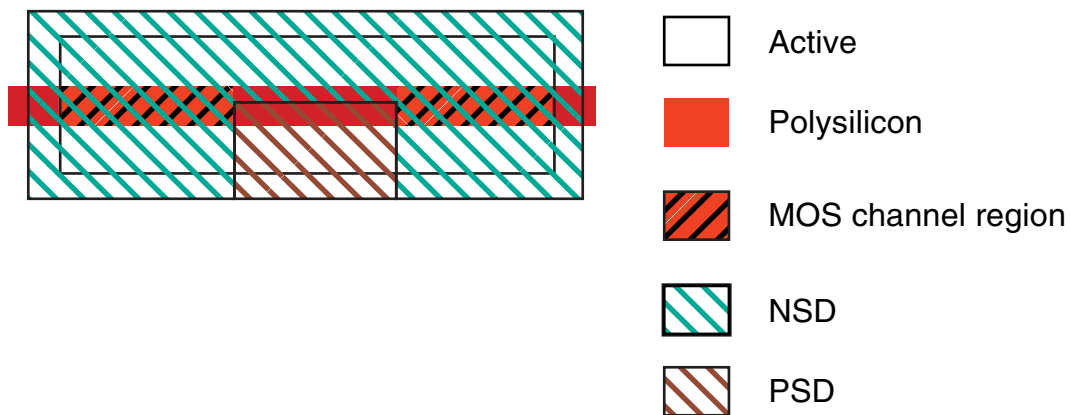
Capacitor region -- The intersection of poly (POLY) and active (ACT) inside CAPLCN, CAPN, or CAPP. It corresponds to the drawn area of a capacitor.

Flag Layer -- A logical layer that is used to control verification or autogeneration processing of a layout, but does not directly correspond to the design data for a particular reticle.

2D Design Layers

Active Area Layer (ACT, ACTF, ACTXPP) -- The ACT layer is generally used to define silicon islands corresponding to MOS active areas, capacitor bottom plates, etc. MITLL will oversize features drawn on ACT by 0.075 µm per side to accommodate the sidewall implant process. This oversized active area will be ORed with ACTF and ACTXPP to produce a single active mask. The ACTF layer is to be used for fill patterns only. For information on the proper use of ACTXPP, contact MITLL.

Rule	Description	Constraint
1.1	Minimum contacted width (derived rule from 15.1 & 15.3)	0.600 µm
1.2	Minimum width (channel region, or used as a conductor)	0.500 µm
1.3	Minimum spacing	0.600 µm
1.4	Minimum extension of active beyond poly	0.500 µm
1.5	Required minimum active density within any 1 mm x 1 mm window	40%
1.6	Required maximum active density within any 1mm x 1mm window	60%

n-Channel Body Implant Layer (CBN) -- NMOS transistor active areas should receive this p-type implant.

Rule	Description	Constraint
4.1	Minimum width	0.500 µm
4.2	Minimum surround on NMOS channel region	0.450 µm
4.3	Minimum spacing CBN to CBN (if not merged)	0.250 µm
4.4	Minimum spacing field CBN to PMOS channel	0.300 µm
4.5	Minimum spacing to PMOS channel on common active	0.400 µm
4.6	CBN-CBP overlap on (ACT AND POLY)	prohibited
4.7	Minimum CBN extension beyond NMOS H-gate arm	0.250 µm

p-Channel Body Implant Layer (CBP) -- PMOS transistor active areas should receive this n-type implant.

Rule	Description	Constraint
5.1	Minimum width	0.500 µm
5.2	Minimum surround on PMOS channel region	0.450 µm
5.3	Minimum spacing CBP to CBP (if not merged)	0.250 µm
5.4	Minimum spacing field CBP to NMOS channel	0.300 µm
5.5	Minimum spacing to NMOS channel on common active	0.400 µm
5.6	CBP-CBN overlap on (ACT AND POLY)	prohibited
5.7	Minimum CBP extension beyond PMOS H-gate arm	0.250 µm

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<u>Polysilicon Gate Layer</u> (POLY, POLYF) -- This layer defines poly lines, MOS gates, capacitor top plates, etc. POLY will be ORed with POLYF to produce a single poly mask. The POLYF layer is to be used for fill patterns only.

Rule	Description	Constraint
9.1	Minimum drawn width (Minimum width lines will be reduced in fabrication to give 0.18 µm features.)	0.200 µm
9.2	Minimum spacing	0.250 µm
9.3	Minimum spacing over common active	0.350 µm
9.4	Minimum field poly spacing to active area	0.350 µm
9.5	Minimum gate extension poly spacing to contact surround active area (for case of "dogbone" transistors)	0.250 µm
9.6	Minimum extension beyond active area	0.400 µm
9.7	Minimum active surround when used as capacitor top plate	0.350 µm
9.8	Minimum CAPP, CAPN, or CAPLCN surround when used as capacitor top plate	0.300 µm
9.9	POLY on ACT outside of NSD or PSD	prohibited
9.10	Required minimum poly density within any 1 mm x 1 mm window	10%
9.11	Required maximum poly density within any 1mm x 1mm window	20%

NOTE: It is strongly recommended that all interconnect poly receive NSD or PSD. Yield may be improved significantly when poly interconnect is implanted.

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***n+ Implant Layer* (NSD) -- This layer defines the NMOS source/drain and PMOS body contact implant. Use this layer for n+ degenerate doping to form ohmic contacts and to dope poly.**

Rule	Description	Constraint
12.1	Minimum width	0.500 µm
12.2	Minimum surround on NMOS channel region except in body contact region	0.400 µm
12.3	Minimum extension beyond active area	0.200 µm
12.4	Minimum spacing NSD to NSD (if not merged)	0.250 µm
12.5	Minimum spacing field NSD to non-NSD active area	0.200 µm
12.6	Minimum spacing field NSD to PMOS channel region	0.400 µm
12.7	Minimum spacing from intersection of non-body contact NSD and active to PMOS channel on common island	0.400 µm
12.8	Minimum NSD overlap on poly gate (This rule applies to body contact structures, where the gate receives NSD on one side and PSD on the other. If the poly width is large enough, a 0.150 µm overlap is strongly recommended.)	0.100 µm
12.9	NSD-PSD overlap on active or poly	prohibited
12.10	Minimum surround on n-type capacitor top plate poly	0.550 µm

***p+ Implant Layer* (PSD) -- This layer defines the PMOS source/drain and NMOS body contact implant. Use this layer for p+ degenerate doping to form ohmic contacts and to dope poly.**

Rule	Description	Constraint
13.1	Minimum width	0.500 µm
13.2	Minimum surround on PMOS channel region except in body contact region	0.400 µm
13.3	Minimum extension beyond active area	0.200 µm
13.4	Minimum spacing PSD to PSD (if not merged)	0.250 µm
13.5	Minimum spacing field PSD to non-PSD active area	0.200 µm
13.6	Minimum spacing field PSD to NMOS channel region	0.400 µm
13.7	Minimum spacing from intersection of non-body contact PSD and active to NMOS channel on common island	0.400 µm
13.8	Minimum PSD overlap on poly gate (This rule applies to body contact structures, where the gate receives NSD on one side and PSD on the other. If the poly width is large enough, a 0.150 µm overlap is strongly recommended)	0.100 µm
13.9	PSD-NSD overlap on active or poly	prohibited
13.10	Minimum surround on p-type capacitor top plate poly	0.550 µm

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***Contact Cut Layer** (CON) -- Use this layer to define contact cuts to the active and poly areas.*

Rule	Description	Constraint
15.1	CON contact size (only size allowed)	0.250 µm square
15.2	Minimum spacing	0.350 µm
15.3	Minimum ACT surround if contacting to ACT	0.175 µm
15.4	Minimum POLY surround if contacting to POLY	0.175 µm
15.5	Minimum spacing to POLY gate	0.350 µm
15.6	Minimum (ACT AND POLY) surround if contacting to POLY over ACT	0.175 µm
15.7	Minimum (NSD OR PSD) surround	0.175 µm

***Low Series Resistance RF Contact Cut to Gate Layer** (CONRFG) -- Use this layer to define low gate series resistance RF T-gates. CONRFG will connect to any intersecting M1 features. Metal 1 must be placed over all CONRFG features. It is permissible for this metal 1 to have its edges coincident with those of the CONRFG features.*

Rule	Description	Constraint
16.1	CONRFG contact trench width (only size allowed)	0.250 µm
16.2	Minimum spacing	0.350 µm
16.3	Minimum spacing CONRFG to CON	0.350 µm
16.4	Maximum width CONRFG NOT POLY)	0.025 µm
16.5	Minimum (NSD OR PSD) surround	0.175 µm
16.6	CONRFG outside metal 1	prohibited

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__Metal 1 Layer (M1, M1F)__ -- This layer defines the first metal level. The M1 layer will be ORed with M1F to produce a single metal 1 mask. The M1F layer is to be used for fill patterns only.

Rule	Description	Constraint
17.1	Minimum width	0.250 μm
17.2	Minimum spacing	0.350 μm
17.3	Minimum surround on contact cut	0.150 μm
17.4	Required minimum metal 1 density within any 1 mm x 1 mm window	30 %
17.5	Required maximum metal 1 density within any 1mm x 1 mm 1mm x 1 mm window	50 %

__Metal 1 / Metal 2 Via Layer__ (V12) -- This layer defines vias between the first and second metal levels.

Rule	Description	Constraint
19.1	Via size (only size allowed)	0.300 μm square
19.2	Minimum spacing	0.400 μm
19.3	Minimum metal 1 surround	0.150 μm
19.4	Stacked via V12 on contact (metal 1 must be present)	Allowed
19.5	Stacked via V12 on CONRFG (metal 1 must be present)	Allowed

__Metal 2 Layer (M2, M2F)__ -- This layer defines the second metal level. The M2 layer will be ORed with M2F to produce a single metal 2 mask. The M2F layer is to be used for fill patterns only.

Rule	Description	Constraint
20.1	Minimum width	0.250 μm
20.2	Minimum spacing	0.350 μm
20.3	Minimum surround on via V12	0.150 μm
20.4	Required minimum metal 2 density within any 1 mm x 1 mm window	30 %
20.5	Required maximum metal 2 density within any 1mm x 1 mm window	50 %

Top-level RF Metal Via Layer *(VTLRF) -- This layer defines vias between the Top-level RF metal level and the highest-level interconnect metal level below. For example, if the process includes three metal levels, and the third metal level corresponds to MTLRF, then VTLRF defines vias between MTLRF and M2. The rules for this layer are determined by the thickness of the ILD through which the via is formed, as specified by the given formulae.*

Rule	Description	Constraint
31.1	Via size (only size allowed)	w x w square
31.2	Minimum spacing	d_{min}
31.3	Minimum underlying metal surround	0.150 µm
31.4	Stacked via VTLRF on prior via (underlying metal must be present	Allowed

Formulae:

$w = (t_{ILD} / 3) - 50$ nm; and
$d_{min} = (t_{ILD} / 3) + 50$ nm;

where t_{ILD} is the thickness of the ILD through which the via cut is formed.
Note that w and d_{min} should be rounded *up* to a multiple of 25 nm.

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Top-level RF Metal Layer *(MTLRF, MTLRFF) -- This layer defines a top-level metal layer optimized for RF design. The MTLRF layer will be ORed with MTLRFF to produce a single RF metal mask. The MTLRFF layer is to be used for fill patterns only. The rules for this layer are determined by the thickness of the metal layer, as specified by the given formulae.*

Rule	Description	Constraint
32.1	Minimum width	w_{min}
32.2	Minimum spacing	d_{min}
32.3	Minimum surround on via VTLRF	0.150 µm
32.4	Required minimum top-level RF metal density within any 1 mm x 1 mm window	30 %
32.5	Required maximum top-level RF metal density within any 1mm x 1 mm window	50 %

Formulae:

$$W_{min} = (t_{metal} / 2) - 50 \text{ nm; and}$$
$$d_{min} = (t_{metal} / 2) + 50 \text{ nm;}$$

where t_{metal} is the thickness of the metal layer.
Note that w_{min} and d_{min} should be rounded *up* to a multiple of 25 nm.

Overglass Pad Cut Layer *(OGC) -- This layer defines pad cuts in the overglass, which allow top-level metal pads to be contacted.*

Rule	Description	Constraint
34.1	Spacing in from top-level metal pad edge	1.000 µm

Additional Flag Design Layers

<u>Slot Suppression Flag</u> (NOSLOT) -- This layer suppresses automatic generation of locally-thinned regions. For the locally thinned process version, all island areas residing under polysilicon are locally thinned if NOSLOT is not present.
(NO RULES PROVIDED)

<u>Automatic Fill Generation Suppression Flag</u> (NOFILL) -- This layer suppresses automatic fill generation. In regions not getting NOFILL, fill structures are automatically generated by MITLL to force compliance with layer density rules. IMPORTANT: When NOFILL is used, it is the responsibility of the designer to ensure compliance with all layer density specifications. Non-compliant layouts will be rejected, unless MITLL has approved a written application for a waiver of density constraints. This application must be submitted at least one month in advance of the design submission deadline to allow for sufficient time for consultation with the designer and with MITLL process engineers. Contact MITLL for more information.
(NO RULES PROVIDED)

Comment and Markup Layers

<u>Red Comment Layer</u> (RED) -- Use for comments
    (NO RULES PROVIDED)

<u>Green Comment Layer</u> (GREEN) -- Use for comments
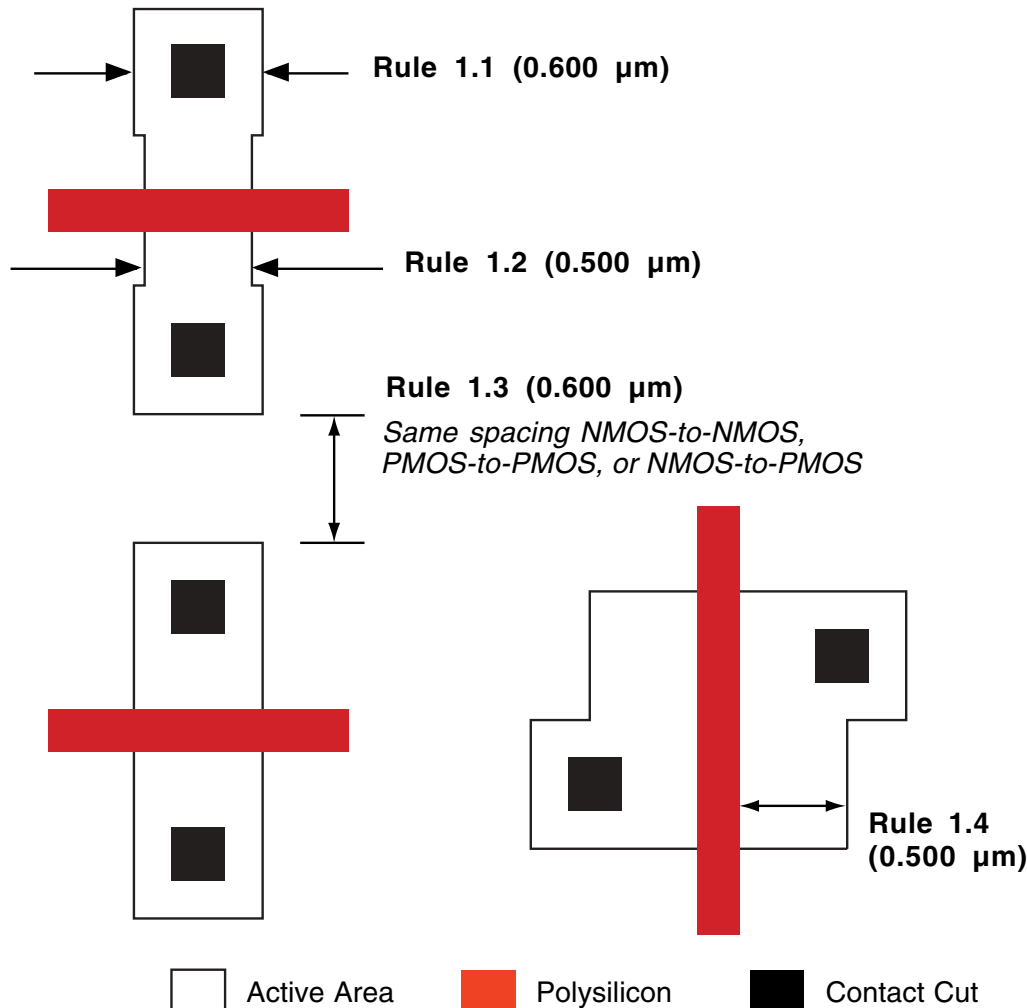   **(NO RULES PROVIDED)**

<u>Blue Comment Layer</u> (BLUE) -- Use for comments
    (NO RULES PROVIDED)

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***Active Area Layer** (ACT, ACTF, ACTXPP) — **The ACT layer is generally used to define silicon islands corresponding to MOS active areas, capacitor bottom plates, etc.* MITLL will oversize features drawn on ACT by 0.075 µm per side to accommodate the sidewall implant process. This oversized active area will be ORed with ACTF and ACTXPP to produce a single active mask. The ACTF layer is to be used for fill patterns only. For information on the proper use of ACTXPP, contact MITLL.*

Rule	Description	Constraint
1.1	Minimum contacted width (derived rule from 15.1 & 15.3)	0.600 µm
1.2	Minimum width (channel region, or used as a conductor)	0.500 µm
1.3	Minimum spacing	0.600 µm
1.4	Minimum extension of active beyond poly	0.500 µm
1.5	Required minimum active density within any 1 mm x 1 mm window	40%
1.6	Required maximum active density within any 1mm x 1mm window	60%

Rule 1.1 (0.600 µm)

Rule 1.2 (0.500 µm)

Rule 1.3 (0.600 µm)

Same spacing NMOS-to-NMOS, PMOS-to-PMOS, or NMOS-to-PMOS

Rule 1.4 (0.500 µm)
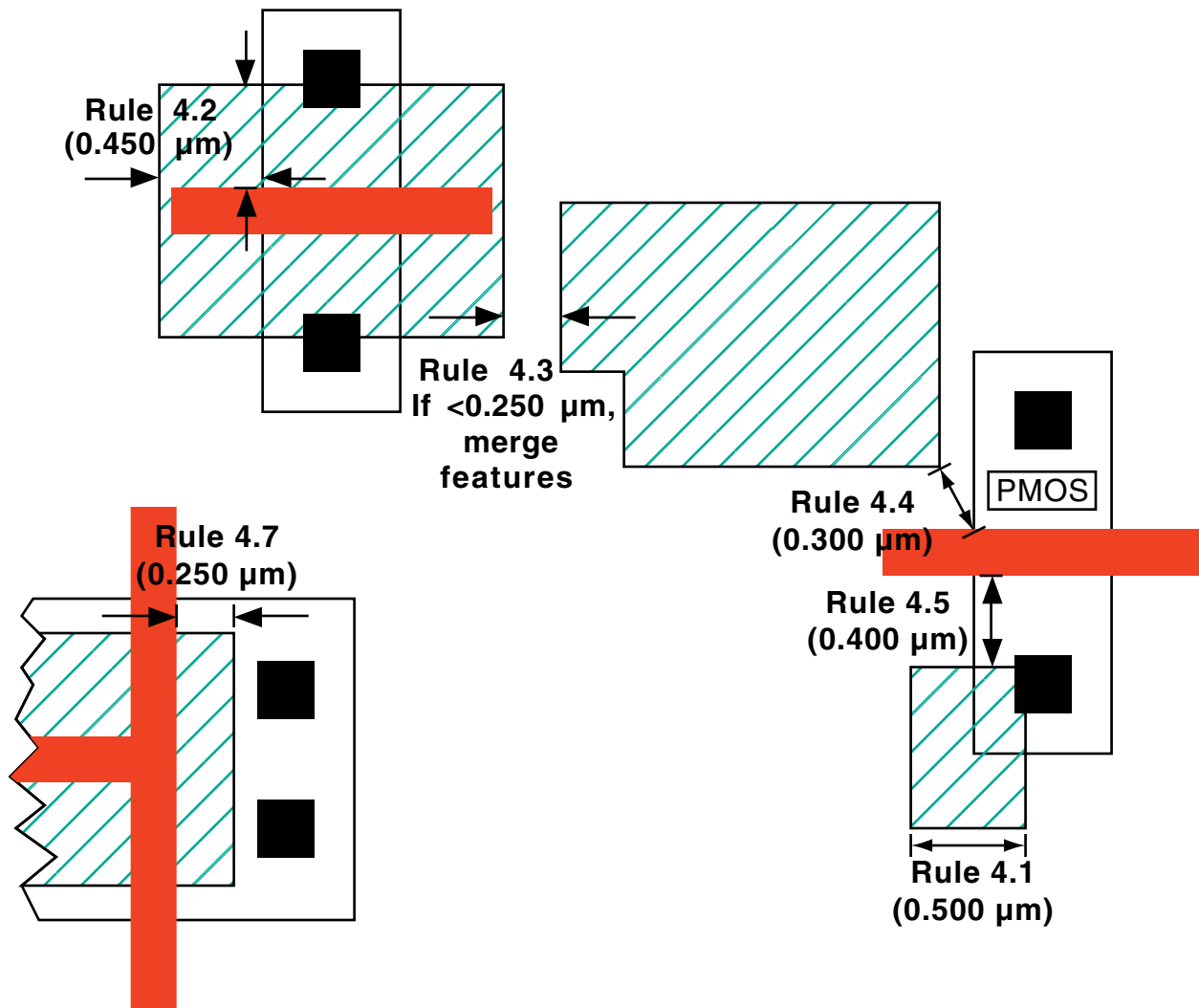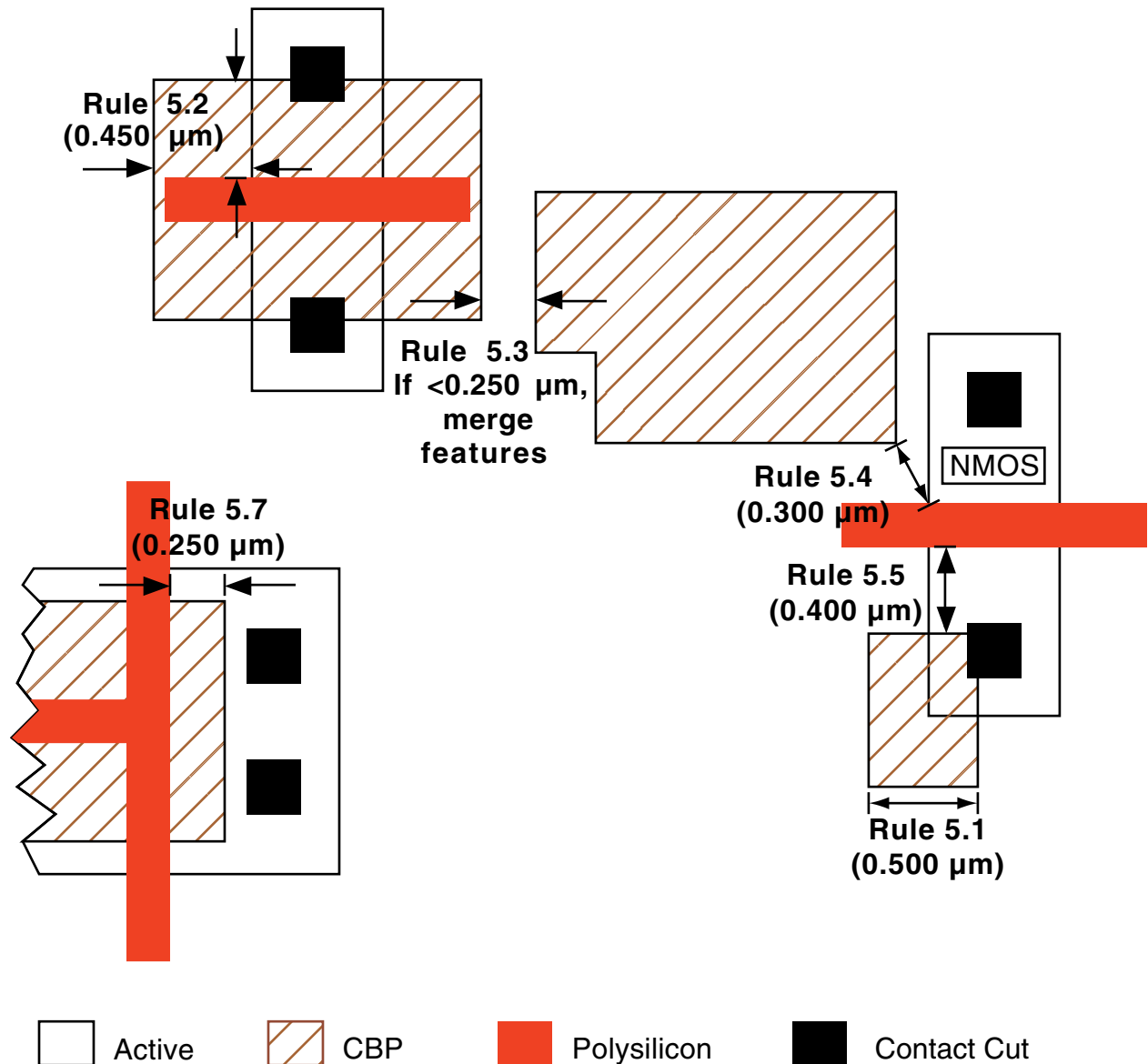
Active Area   Polysilicon   Contact Cut

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules
(version 5.11.mp5, January 2002)

n-Channel Body Implant Layer (CBN) — NMOS transistor active areas should receive this p-type implant.

Rule	Description	Constraint
4.1	Minimum width	0.500 µm
4.2	Minimum surround on NMOS channel region	0.450 µm
4.3	Minimum spacing CBN to CBN (if not merged)	0.250 µm
4.4	Minimum spacing field CBN to PMOS channel	0.300 µm
4.5	Minimum spacing to PMOS channel on common active	0.400 µm
4.6	CBN-CBP overlap on (ACT AND POLY)	prohibited
4.7	Minimum CBN extension beyond NMOS H-gate arm	0.250 µm

Rule 4.2
(0.450 µm)

Rule 4.3
If <0.250 µm,
merge
features

Rule 4.4
(0.300 µm)

Rule 4.5
(0.400 µm)

PMOS

Rule 4.7
(0.250 µm)

Rule 4.1
(0.500 µm)

| | Active | | CBN | | Polysilicon | | Contact Cut |

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

p-Channel Body Implant Layer (CBP) **_ — PMOS transistor active areas_**
should receive this n-type implant.

Rule	Description	Constraint
5.1	Minimum width	0.500 µm
5.2	Minimum surround on PMOS channel region	0.450 µm
5.3	Minimum spacing CBP to CBP (if not merged)	0.250 µm
5.4	Minimum spacing field CBP to NMOS channel	0.300 µm
5.5	Minimum spacing to NMOS channel on common active	0.400 µm
5.6	CBP-CBN overlap on (ACT AND POLY)	prohibited
5.7	Minimum CBP extension beyond PMOS H-gate arm	0.250 µm

Active	CBP	Polysilicon	Contact Cut

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

Polysilicon Gate Layer (POLY, POLYF) — This layer defines poly lines, MOS gates, capacitor top plates, etc. POLY will be ORed with POLYF to produce a single poly mask. The POLYF layer is to be used for fill patterns only.
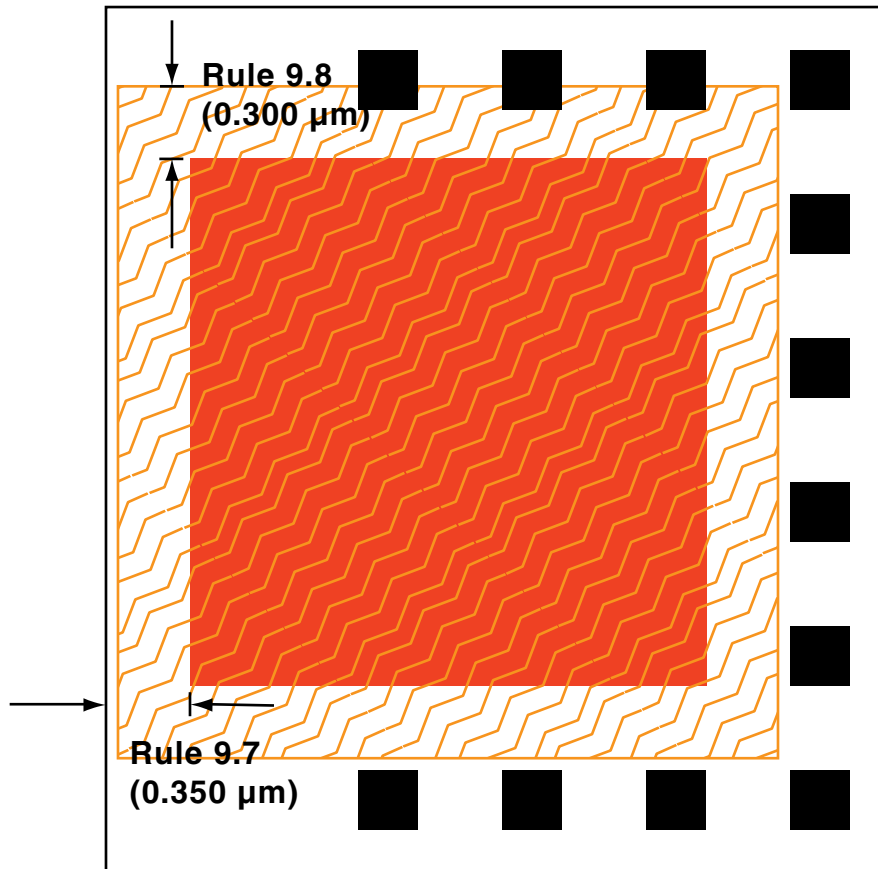
Rule	Description	Constraint
9.1	Minimum drawn width (Minimum width lines will be reduced in fabrication to give 0.18 µm features.)	0.200 µm
9.2	Minimum spacing	0.250 µm
9.3	Minimum spacing over common active	0.350 µm
9.4	Minimum field poly spacing to active area	0.350 µm
9.5	Minimum gate extension poly spacing to contact surround active area (for case of "dogbone" transistors)	0.250 µm
9.6	Minimum extension beyond active area	0.400 µm
9.7	Minimum active surround when used as capacitor top plate	0.350 µm
9.8	Minimum CAPP, CAPN, or CAPLCN surround when used as capacitor top plate	0.300 µm
9.9	POLY on ACT outside of NSD or PSD	prohibited
9.10	Required minimum poly density within any 1 mm x 1 mm window	10%
9.11	Required maximum poly density within any 1mm x 1mm window	20%

NOTE: It is strongly recommended that all interconnect poly receive NSD or PSD. Yield may be improved significantly when poly interconnect is implanted.

Rule 9.2 (0.250 µm)
Rule 9.5 (0.250 µm)
Rule 9.3 (0.350 µm)
Rule 9.4 (0.350 µm)
Rule 9.1 (0.200 µm)
Rule 9.6 (0.400 µm)

Active Area   Polysilicon   Contact Cut

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

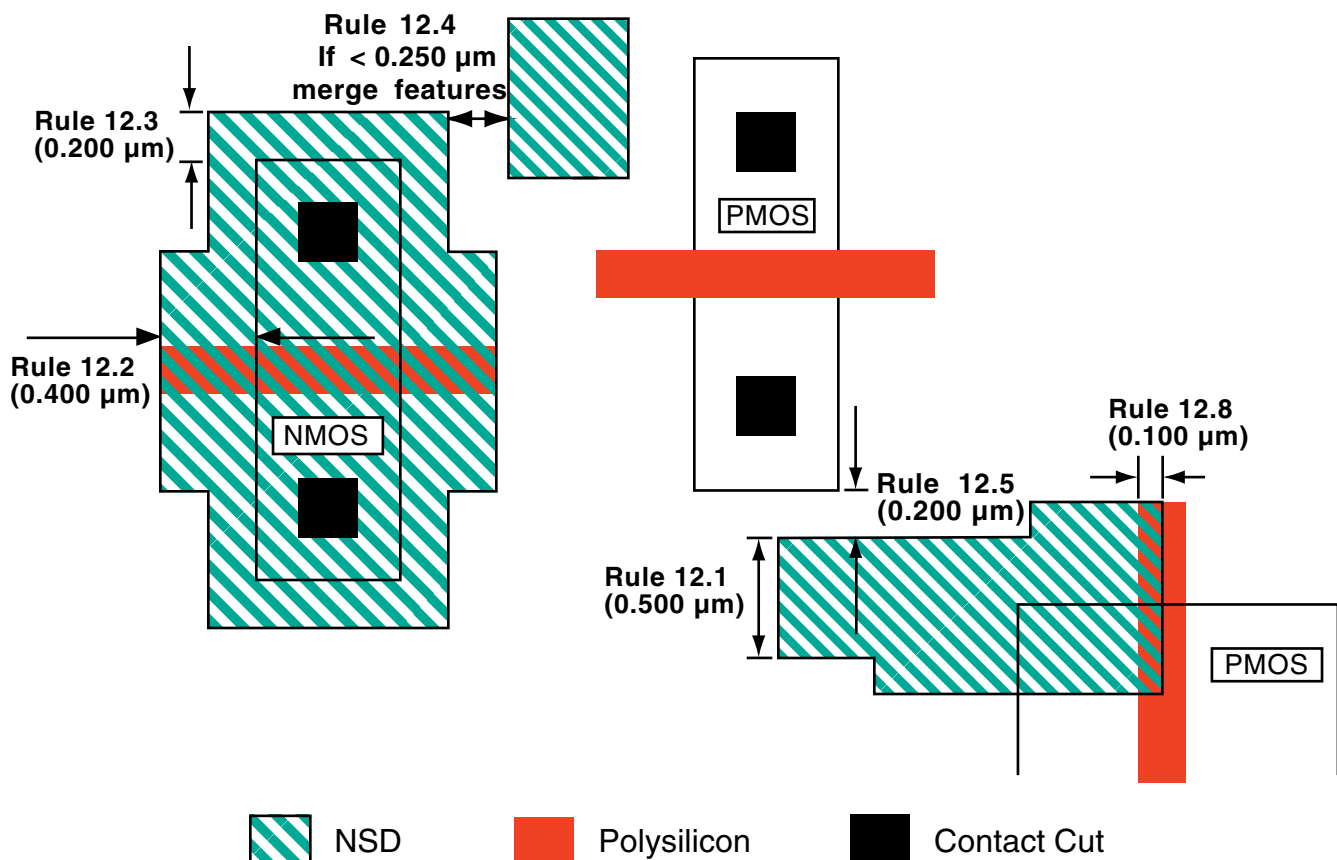| | Active Area | | CAPLCN | | Polysilicon | | Contact Cut |

Note: In the above figure, the region receiving CAPLCN is also illustrative of the case where the CAPN or CAPP implant layers are used.

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules
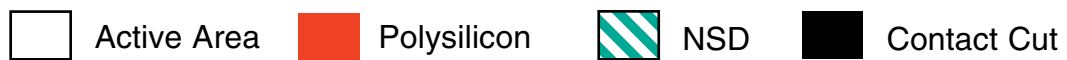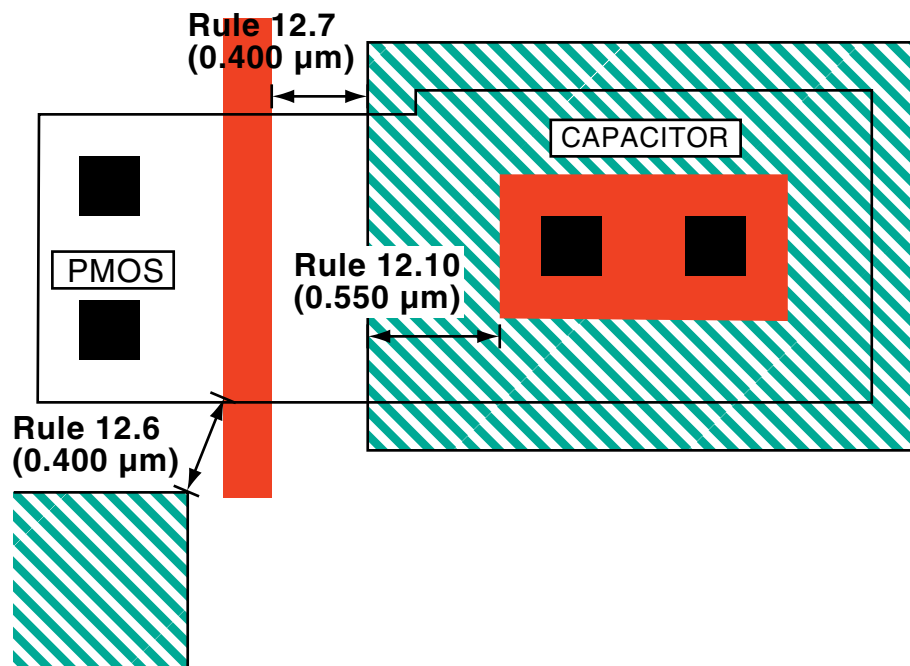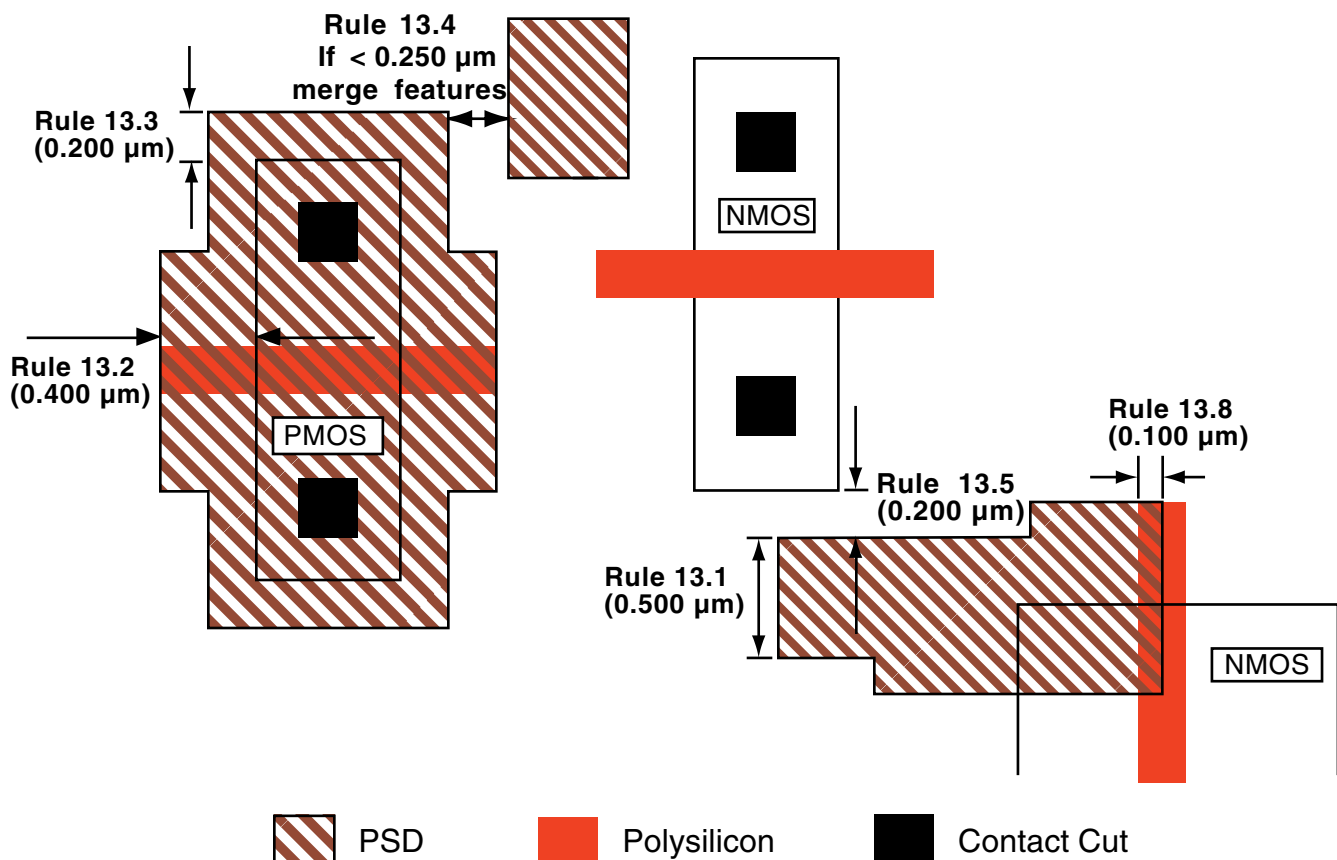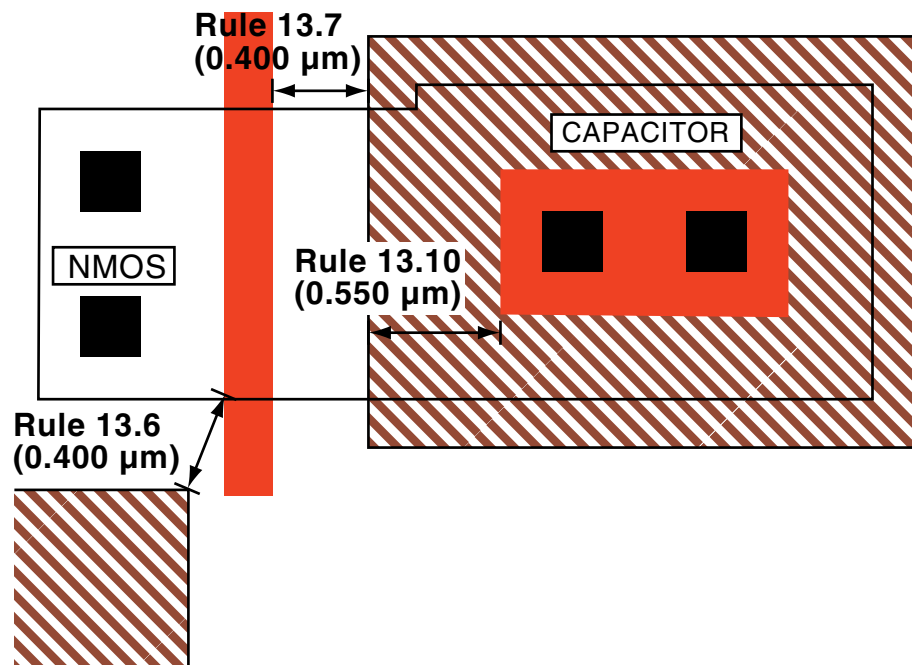
(version 5.11.mp5, January 2002)

n+ Implant Layer (NSD) — This layer defines the NMOS source/drain and PMOS body contact implant. Use this layer for n+ degenerate doping to form ohmic contacts and to dope poly.

Rule	Description	Constraint
12.1	Minimum width	0.500 µm
12.2	Minimum surround on NMOS channel region except in body contact region	0.400 µm
12.3	Minimum extension beyond active area	0.200 µm
12.4	Minimum spacing NSD to NSD (if not merged)	0.250 µm
12.5	Minimum spacing field NSD to non-NSD active area	0.200 µm
12.6	Minimum spacing field NSD to PMOS channel region	0.400 µm
12.7	Minimum spacing from intersection of non-body contact NSD and active to PMOS channel on common island	0.400 µm
12.8	Minimum NSD overlap on poly gate (This rule applies to body contact structures, where the gate receives NSD on one side and PSD on the other. If the poly width is large enough, a 0.150 µm overlap is strongly recommended.)	0.100 µm
12.9	NSD-PSD overlap on active or poly	prohibited
12.10	Minimum surround on n-type capacitor top plate poly	0.550 µm

MITLL 0.18 μm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

**Rule 12.7
(0.400 μm)**

CAPACITOR

PMOS

**Rule 12.10
(0.550 μm)**

**Rule 12.6
(0.400 μm)**

Active Area   Polysilicon   NSD   Contact Cut

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

p+ Implant Layer (PSD) — This layer defines the PMOS source/drain and NMOS body contact implant. Use this layer for p+ degenerate doping to form ohmic contacts and to dope poly.

Rule	Description	Constraint
13.1	Minimum width	0.500 µm
13.2	Minimum surround on PMOS channel region except in body contact region	0.400 µm
13.3	Minimum extension beyond active area	0.200 µm
13.4	Minimum spacing PSD to PSD (if not merged)	0.250 µm
13.5	Minimum spacing field PSD to non-PSD active area	0.200 µm
13.6	Minimum spacing field PSD to NMOS channel region	0.400 µm
13.7	Minimum spacing from intersection of non-body contact PSD and active to NMOS channel on common island	0.400 µm
13.8	Minimum PSD overlap on poly gate (This rule applies to body contact structures, where the gate receives NSD on one side and PSD on the other. If the poly width is large enough, a 0.150 µm overlap is strongly recommended)	0.100 µm
13.9	PSD-NSD overlap on active or poly	prohibited
13.10	Minimum surround on p-type capacitor top plate poly	0.550 µm

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

**Rule 13.7
(0.400 µm)**

CAPACITOR

**Rule 13.10
(0.550 µm)**

NMOS

**Rule 13.6
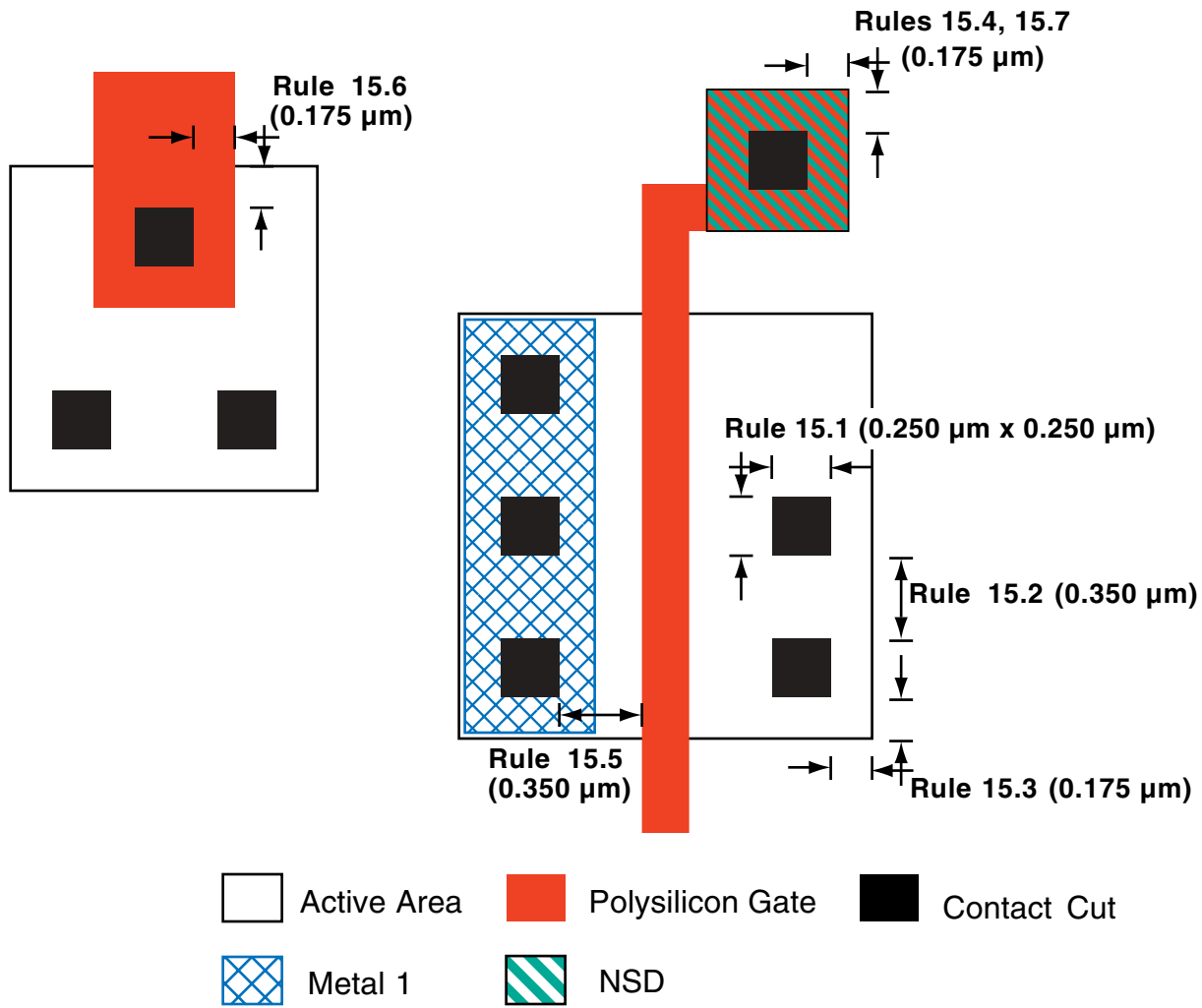(0.400 µm)**

Active Area   Polysilicon   PSD   Contact Cut

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

Contact Cut Layer (CON) — Use this layer to define contact cuts to the active and poly areas.

Rule	Description	Constraint
15.1	CON contact size (only size allowed)	0.250 µm square
15.2	Minimum spacing	0.350 µm
15.3	Minimum ACT surround if contacting to ACT	0.175 µm
15.4	Minimum POLY surround if contacting to POLY	0.175 µm
15.5	Minimum spacing to POLY gate	0.350 µm
15.6	Minimum (ACT AND POLY) surround if contacting to POLY over ACT	0.175 µm
15.7	Minimum (NSD OR PSD) surround	0.175 µm

NOTE: In the above figure, the region receiving NSD is also illustrative of the case where PSD is used.
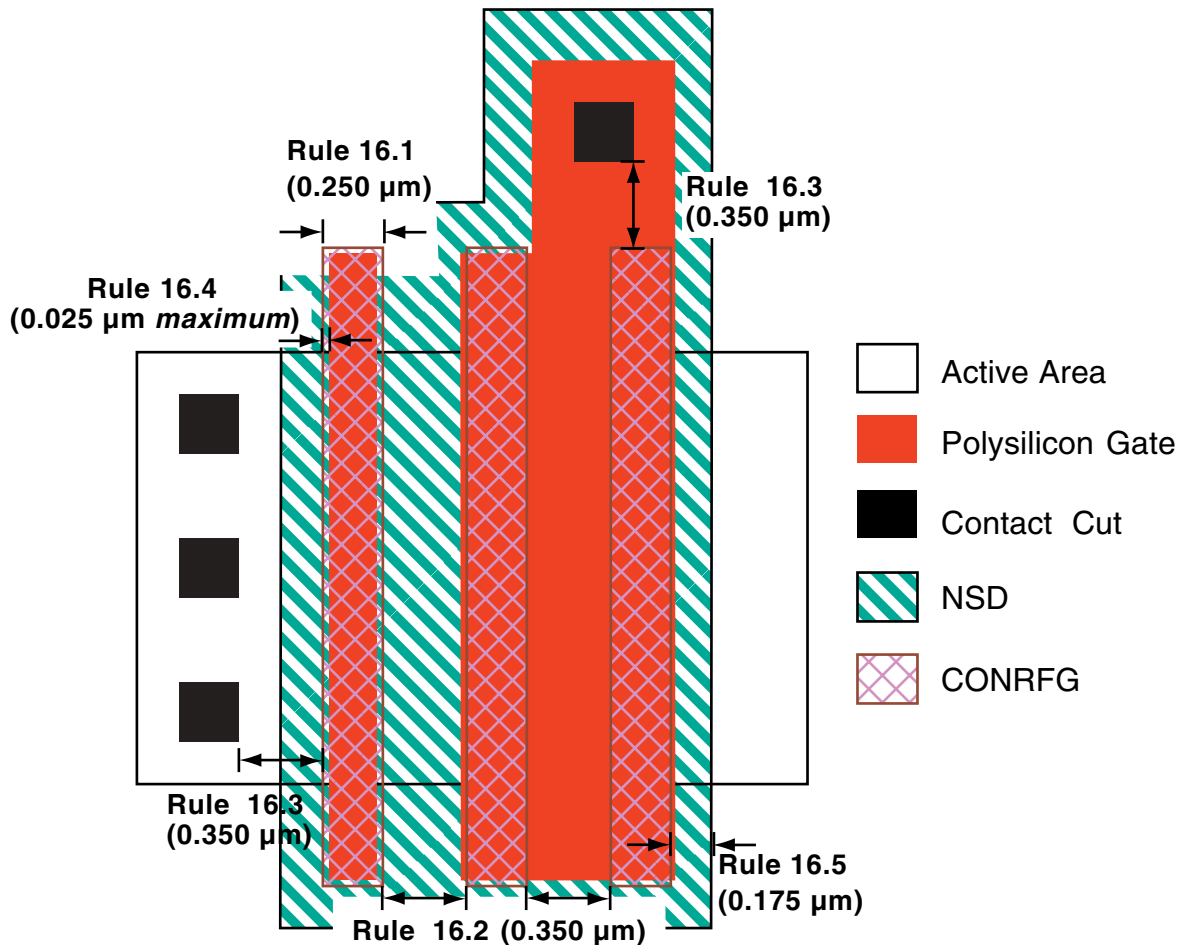
MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

***Low Series Resistance RF Contact Cut to Gate Layer (CONRFG) — Use this
layer to define low gate series resistance RF T-gates. CONRFG will connect to
any intersecting M1 features. Metal 1 must be placed over all CONRFG
features. It is permissible for this metal 1 to have its edges coincident with
those of the CONRFG features.***

OPTIONAL LAYER — NOT OFFERED IN ALL PROCESS VERSIONS

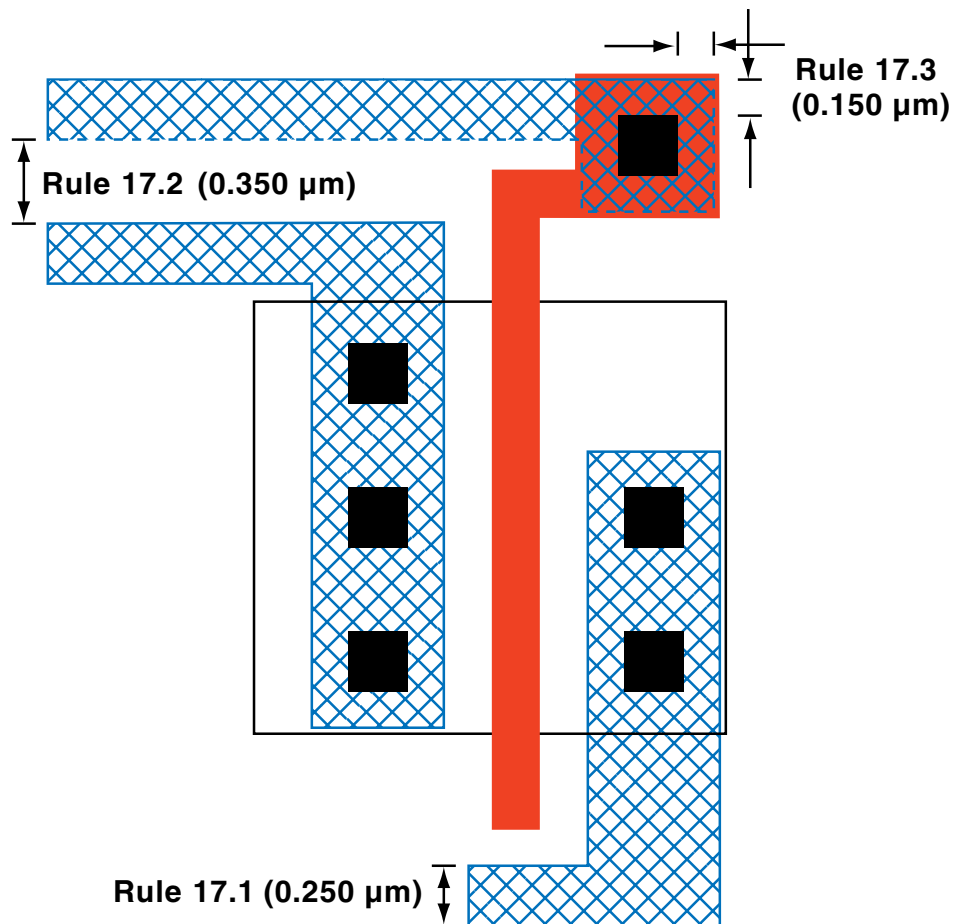| Rule	Description	Constraint
16.1	CONRFG contact trench width (only size allowed)	0.250 µm
16.2	Minimum spacing	0.350 µm
16.3	Minimum spacing CONRFG to CON	0.350 µm
16.4	Maximum width CONRFG NOT POLY)	0.025 µm
16.5	Minimum (NSD OR PSD) surround	0.175 µm
16.6	CONRFG outside metal 1	prohibited

**NOTE: In the above figure, the region receiving NSD is also illustrative of the case
where PSD is used. Metal 1 would be placed in the same location as the drawn
CONRFG features. The required NSD surround on the channel region (rule 12.2) is
not included.**

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

Metal 1 Layer (M1, M1F) — This layer defines the first metal level. The M1 layer will be ORed with M1F to produce a single metal 1 mask. The M1F layer is to be used for fill patterns only.

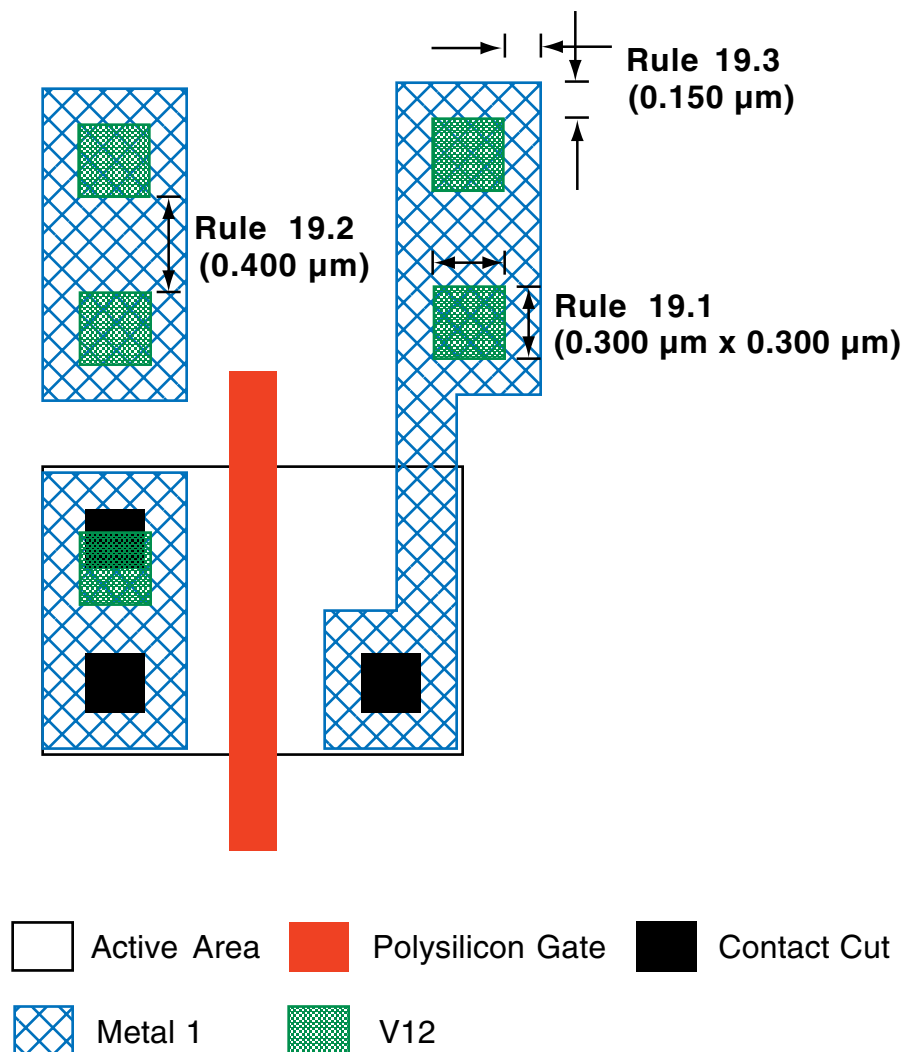| Rule	Description	Constraint
17.1	Minimum width	0.250 µm
17.2	Minimum spacing	0.350 µm
17.3	Minimum surround on contact cut	0.150 µm
17.4	Required minimum metal 1 density within any 1 mm x 1 mm window	30 %
17.5	Required maximum metal 1 density within any 1mm x 1 mm 1mm x 1 mm window	50 %

MITLL 0.18 μm Low Power FDSOI CMOS Design Rules
(version 5.11.mp5, January 2002)

Metal 1 / Metal 2 Via Layer (V12) — This layer defines vias between the first and second metal levels.

Rule	Description	Constraint
19.1	Via size (only size allowed)	0.300 μm square
19.2	Minimum spacing	0.400 μm
19.3	Minimum metal 1 surround	0.150 μm
19.4	Stacked via V12 on contact (metal 1 must be present)	Allowed
19.5	Stacked via V12 on CONRFG (metal 1 must be present)	Allowed

Rule 19.3 (0.150 μm)

Rule 19.2 (0.400 μm)

Rule 19.1 (0.300 μm x 0.300 μm)

☐ Active Area   🟥 Polysilicon Gate   ⬛ Contact Cut
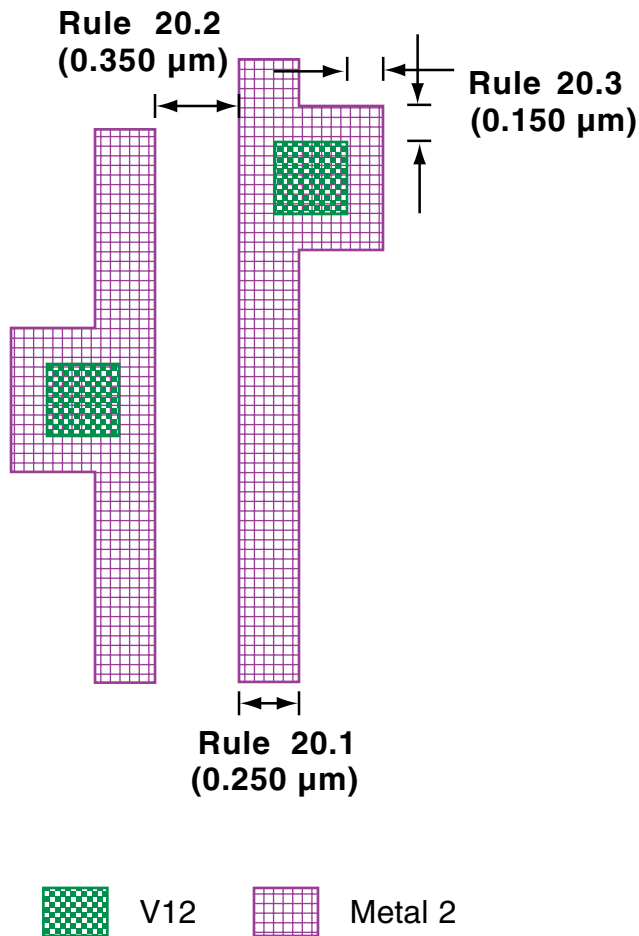
▨ Metal 1   ▨ V12

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

(version 5.11.mp5, January 2002)

Metal 2 Layer (M2, M2F) — This layer defines the second metal level. The M2 layer will be ORed with M2F to produce a single metal 2 mask. The M2F layer is to be used for fill patterns only.

Rule	Description	Constraint
20.1	Minimum width	0.250 µm
20.2	Minimum spacing	0.350 µm
20.3	Minimum surround on via V12	0.150 µm
20.4	Required minimum metal 2 density within any 1 mm x 1 mm window	30 %
20.5	Required maximum metal 2 density within any 1mm x 1 mm window	50 %

Rule 20.2
(0.350 µm)

Rule 20.3
(0.150 µm)

Rule 20.1
(0.250 µm)

V12   Metal 2

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules
(version 5.11.mp5, January 2002)

Top-level RF Metal Via Layer (VTLRF) — This layer defines vias between the Top-level RF metal level and the highest-level interconnect metal level below. For example, if the process includes three metal levels, and the third metal level corresponds to MTLRF, then VTLRF defines vias between MTLRF and M2. *The rules for this layer are determined by the thickness of the ILD through which the via is formed, as specified by the given formulae.*
OPTIONAL LAYER — NOT OFFERED IN ALL PROCESS VERSIONS

Rule	Description	Constraint
31.1	Via size (only size allowed)	w x w square
31.2	Minimum spacing	d_{min}
31.3	Minimum underlying metal surround	0.150 µm
31.4	Stacked via VTLRF on prior via (underlying metal must be present	Allowed

Formulae:

$w = (t_{ILD} / 3) - 50$ nm; and
$d_{min} = (t_{ILD} / 3) + 50$ nm;

where t_{ILD} is the thickness of the ILD through which the via cut is formed. Note that w and d_{min} should be rounded *up* to a multiple of 25 nm.

VTLRF   Underlying Metal

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules
(version 5.11.mp5, January 2002)

***Top-level RF Metal Layer** (MTLRF, MTLRFF) — This layer defines a top-level metal layer optimized for RF design.* *The MTLRF layer will be ORed with MTLRFF to produce a single RF metal mask. The MTLRFF layer is to be used for fill patterns only. The rules for this layer are determined by the thickness of the metal layer, as specified by the given formulae.*
OPTIONAL LAYER — NOT OFFERED IN ALL PROCESS VERSIONS

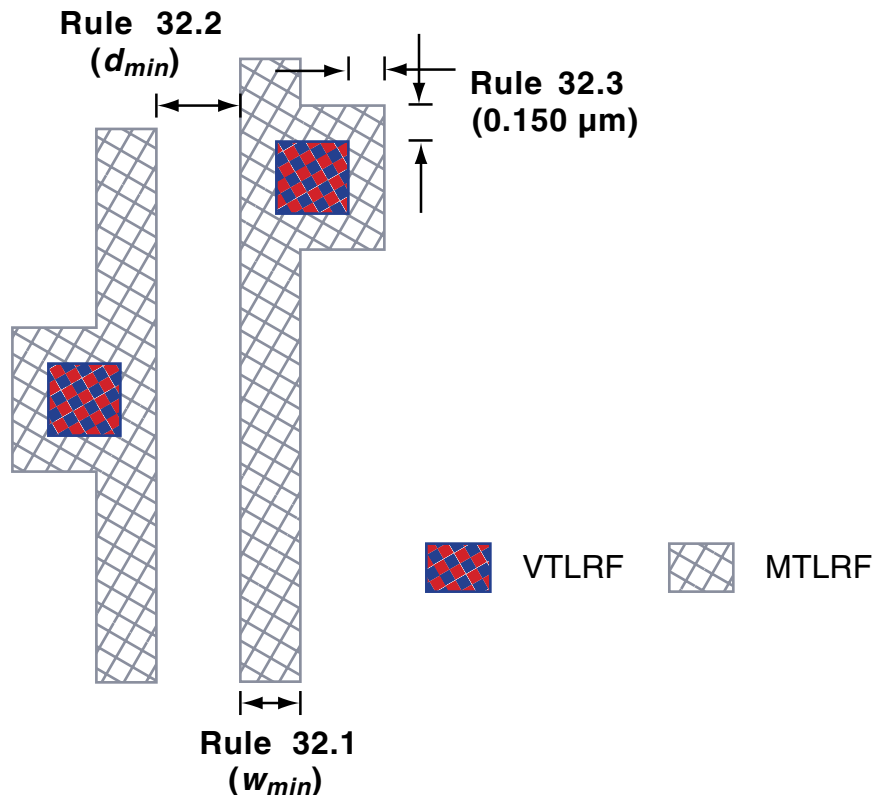| Rule	Description	Constraint
32.1	Minimum width	w_{min}
32.2	Minimum spacing	d_{min}
32.3	Minimum surround on via VTLRF	0.150 µm
32.4	Required minimum top-level RF metal density within any 1 mm x 1 mm window	30 %
32.5	Required maximum top-level RF metal density within any 1mm x 1 mm window	50 %

Formulae:

$$W_{min} = (t_{metal} / 2) - 50 \text{ nm; and}$$
$$d_{min} = (t_{metal} / 2) + 50 \text{ nm;}$$

where t_{metal} is the thickness of the metal layer.
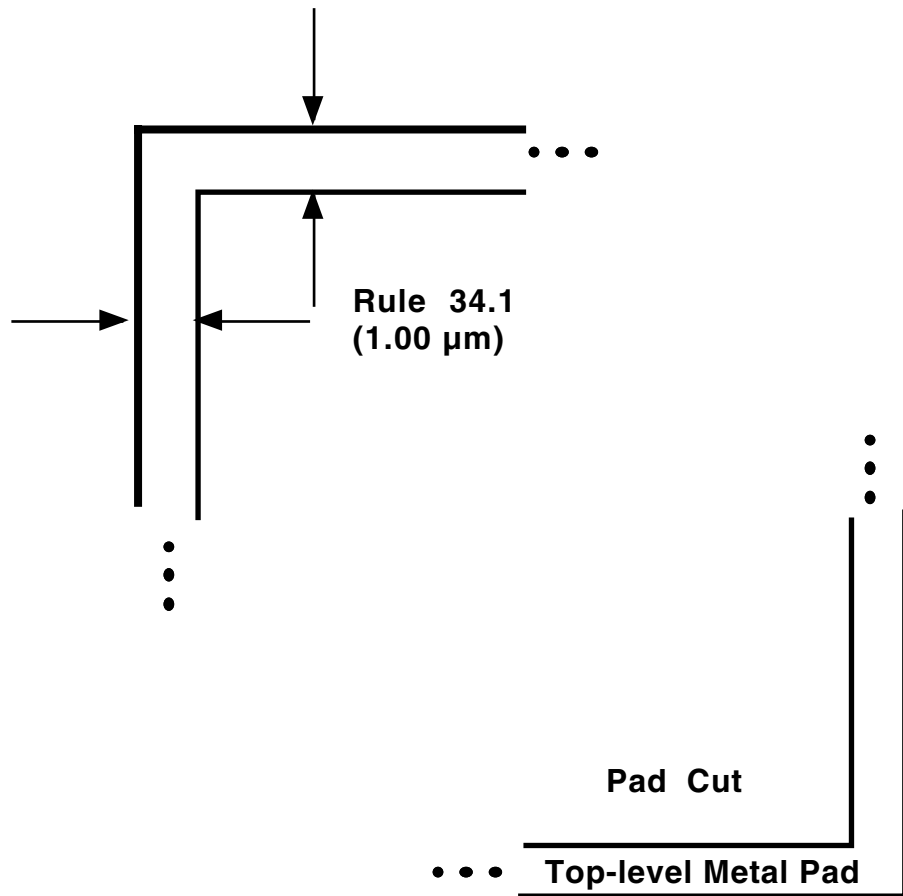Note that w_{min} and d_{min} should be rounded *up* to a multiple of 25 nm.

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MITLL 0.18 µm Low Power FDSOI CMOS Design Rules

Overglass Pad Cut Layer *(OGC) — This layer defines pad cuts in the overglass, which allow top-level metal pads to be contacted.*

Rule	Description	Constraint
34.1	Spacing in from top-level metal pad edge	1.000 µm

**Rule 34.1
(1.00 µm)**

Pad Cut

Top-level Metal Pad

***Slot Suppression Flag* (NOSLOT) — This layer suppresses automatic generation of locally-thinned regions. For the locally thinned process version, all island areas residing under polysilicon are locally thinned if NOSLOT is not present.**
(NO RULES PROVIDED)

***Automatic Fill Generation Suppression Flag* (NOFILL) — This layer suppresses automatic fill generation. In regions not getting NOFILL, fill structures are automatically generated by MITLL to force compliance with layer density rules. IMPORTANT: When NOFILL is used, it is the responsibility of the designer to ensure compliance with all layer density specifications. Non-compliant layouts will be rejected, unless MITLL has approved a written application for a waiver of density constraints. This application must be submitted at least one month in advance of the design submission deadline to allow for sufficient time for consultation with the designer and with MITLL process engineers. Contact MITLL for more information.**
(NO RULES PROVIDED)

MITLL 0.18 µm Low Power FDSOI CMOS Design Rules
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Red Comment Layer _(RED) — Use for comments_
    (NO RULES PROVIDED)

Green Comment Layer _(GREEN) — Use for comments_
    (NO RULES PROVIDED)

Blue Comment Layer _(BLUE) — Use for comments_
    (NO RULES PROVIDED)

2D FDSOI Design Notes and Examples

Introduction

The MIT/LL 0.18 μm Low Power FDSOI CMOS process offers many advantages over bulk CMOS, including full dielectric device isolation, high packing density, reduced parasitic junction capacitances, and improved subthreshold slope. However, certain features of the process can also present challenges to the circuit designer. Mesa isolation, local thinning, silicided active and polysilicon, floating MOS body effects, and chemical-mechanical polishing (CMP) effects all contribute to circuit performance. In this section, the effect of these features on device layout is discussed. Design examples are presented which respond to these challenges.

Throughout this section, a number of values for particular process parameters are mentioned. Some of these are dependent on the particular process version that is implemented. Hence, it is always best to refer to the process parameters table when looking for the exact value for a particular process parameter. The numbers included in this discussion are included so that a correct order of magnitude may be associated with the qualitative discussion. While every attempt will be made to use actual process parameter values in these examples, exact specification of process parameter values in these notes is not guaranteed.

Mesa Isolation

In this process, devices are mesa-isolated. Hence each active region consists of a 40-nm thin silicon island. When any device layout is considered, it becomes important to consider the effect of the island edge on device performance. While this may not be a concern for many digital designs, edge effects can contribute to noise, and may significantly alter subthreshold device characteristics. These effects are discussed in detail in the notes which follow. Layout options for edgeless devices are also presented.

Planar and Locally Thinned Process Versions

The FDSOI devices in this process require a silicon island thickness of about 40 nm. Two approaches to thinning of the silicon to this desired thickness exist. In the planar approach all SOI silicon is thinned to about 45 nm before island definition. As a result, in the final fabricated device, the channel region of transistors is about 40-nm thick, and the contact regions of transistors are even thinner, resulting in less available silicon for silicide formation and hence a higher contact resistance. In the locally thinned process version only the silicon in the channel region of MOS devices is thinned to this thickness, leaving thicker silicon in the contact regions. The NOSLOT layer is used to suppress the automatic generation of features corresponding to locally thinned silicon. A schematic cross section of a device fabricated in the locally thinned process is shown in figure DN-1.

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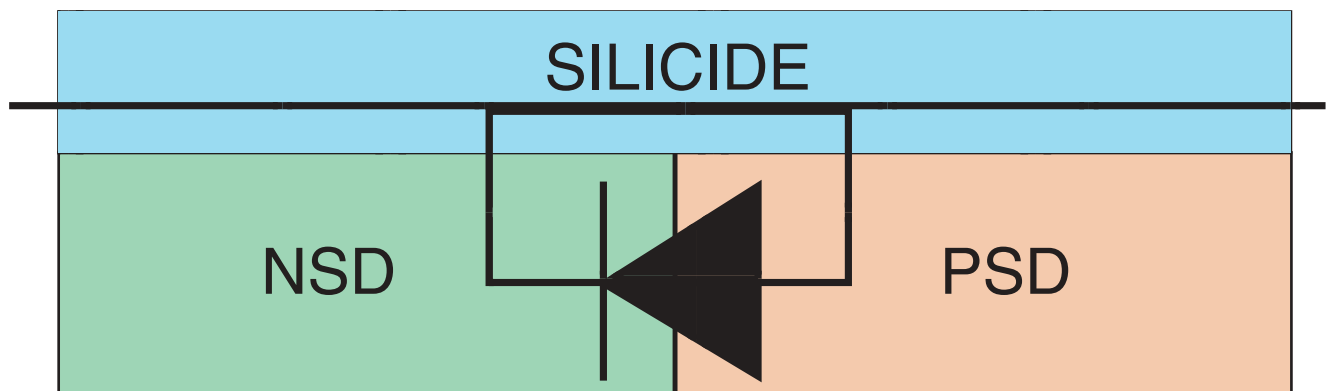# MITLL 0.18 μm Low Power FDSOI CMOS Design Notes and Examples

(version 5.11.mp5, January 2002)
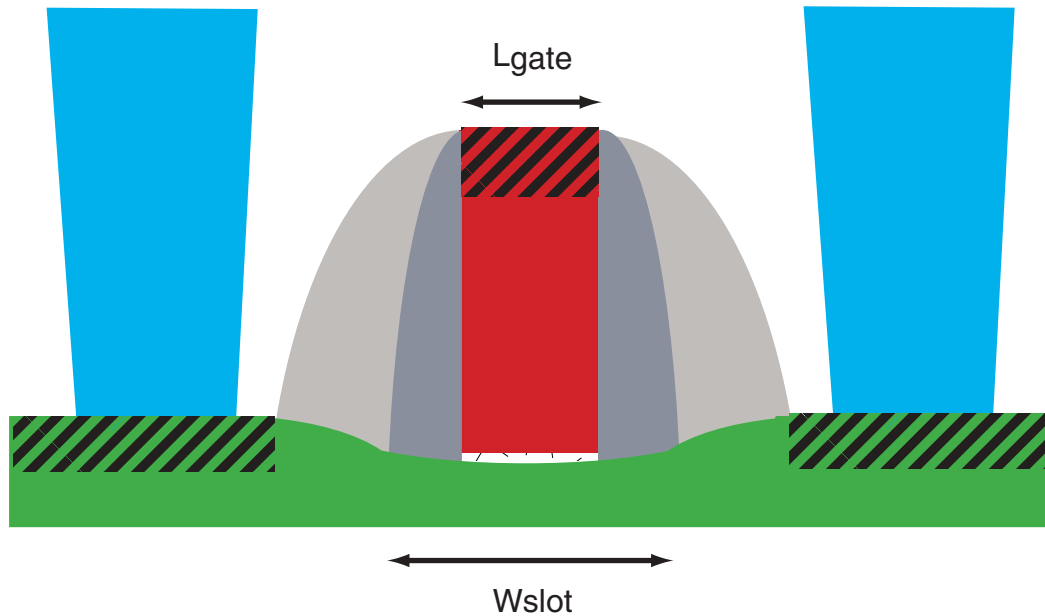
Schematic Cross Section of Locally Thinned Device
FIGURE DN-1

Silicided Poly and Active Features

Following polysilicon definition, all exposed polysilicon and active regions are silicided. This silicide layer has a sheet resistance on the order of 25 Ω/square. As a result, all undoped poly and active features become conductive. In addition, any exposed diodes resulting from abutment of opposite implants will be shorted by the silicide layer. This situation is illustrated in figure DN-2.

The NSD-PSD Diode is shorted by silicide.

FIGURE DN-2

It is strongly recommended that when silicided active or poly is used as a conductor, the feature be doped with NSD or PSD. While this is not essential to device operation, it reduces the risk that defects in the silicide will adversely affect circuit yield.

Floating MOS Body Effects

Unlike bulk CMOS devices, fully depleted SOI devices do not require body contacts. Thus, the body node is often left floating. In this case, the floating body voltage is affected by diode current, impact ionization, GIDL, and capacitance displacement current. It is also possible to implement a body contact, in which case the body contact current also contributes to this voltage. For body contacted devices, the body contact series resistance can be large, so floating body effects can not be completely discounted. The impact of floating body effects on device characteristics and related design considerations are discussed in detail in the notes which follow. Several body contact layout options are presented.

Chemical-Mechanical Polishing

Planarization of ILD layers can result in a layout-dependent dielectric thickness distribution. In some cases, this can cause wide variation in interconnect capacitance, and may affect circuit yield. When polysilicon and metal features are evenly distributed across the wafer, this variation is minimized, and the CMP process is better controlled. In order to reduce process variations, constraints have been placed on metal and poly pattern densities. Further details are presented in the notes which follow.

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Standard NMOS and PMOS Devices

Just as in bulk CMOS, a MOS device is defined by the intersection of active and poly. In mesa-isolated SOI, the active area corresponds to a thin silicon island. This is doped with a threshold adjust implant, in this case CBN or CBP, for NMOS and PMOS devices respectively. The source and drain drift region implants, as well as the source and drain degenerate implants, are both controlled using the NSD and PSD layers. Figure DN-3 shows the layout for a standard 0.6 μm by 0.18 μm NMOS device.
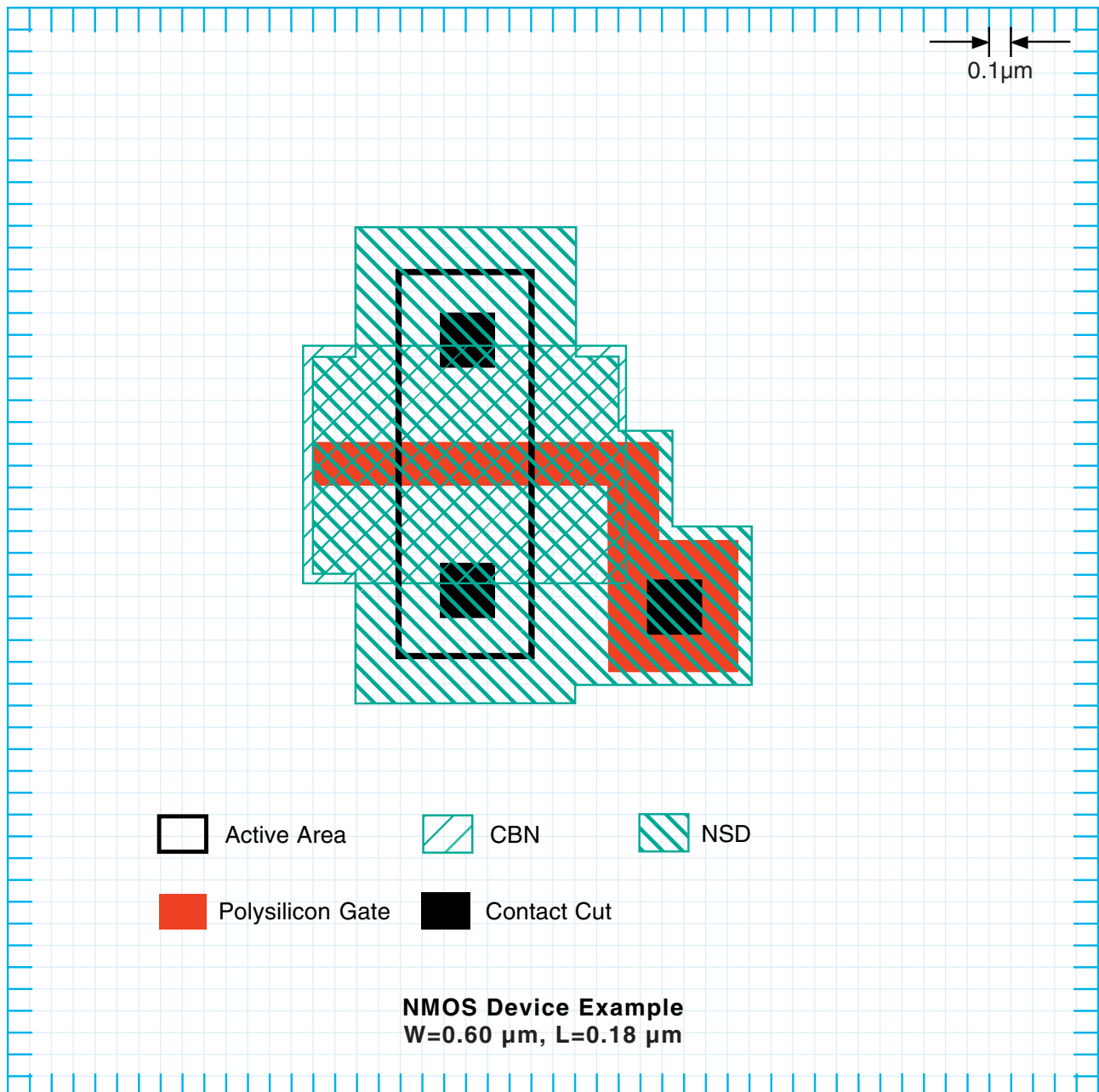

0.1μm

Active Area   CBN   NSD

Polysilicon Gate   Contact Cut

NMOS Device Example
W=0.60 μm, L=0.18 μm

FIGURE DN-3

MITLL 0.18 μm Low Power FDSOI CMOS Design Notes and Examples

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"Dog Bone" Transistors

A minimum geometry 0.5 μm by 0.18 μm device is illustrated in figure DN-4. Note the "dog bone" shape of the active area. Rule 9.5 defines the minimum gate extension poly spacing to contact surround active area to be 0.25 μm. This rule, which is particularly applicable to "dog bone" transistors, is in contrast to rule 9.4, which defines the minimum field poly spacing to active area to be 0.35 μm. In figure DN-4, the distances corresponding to rules 9.4 and 9.5
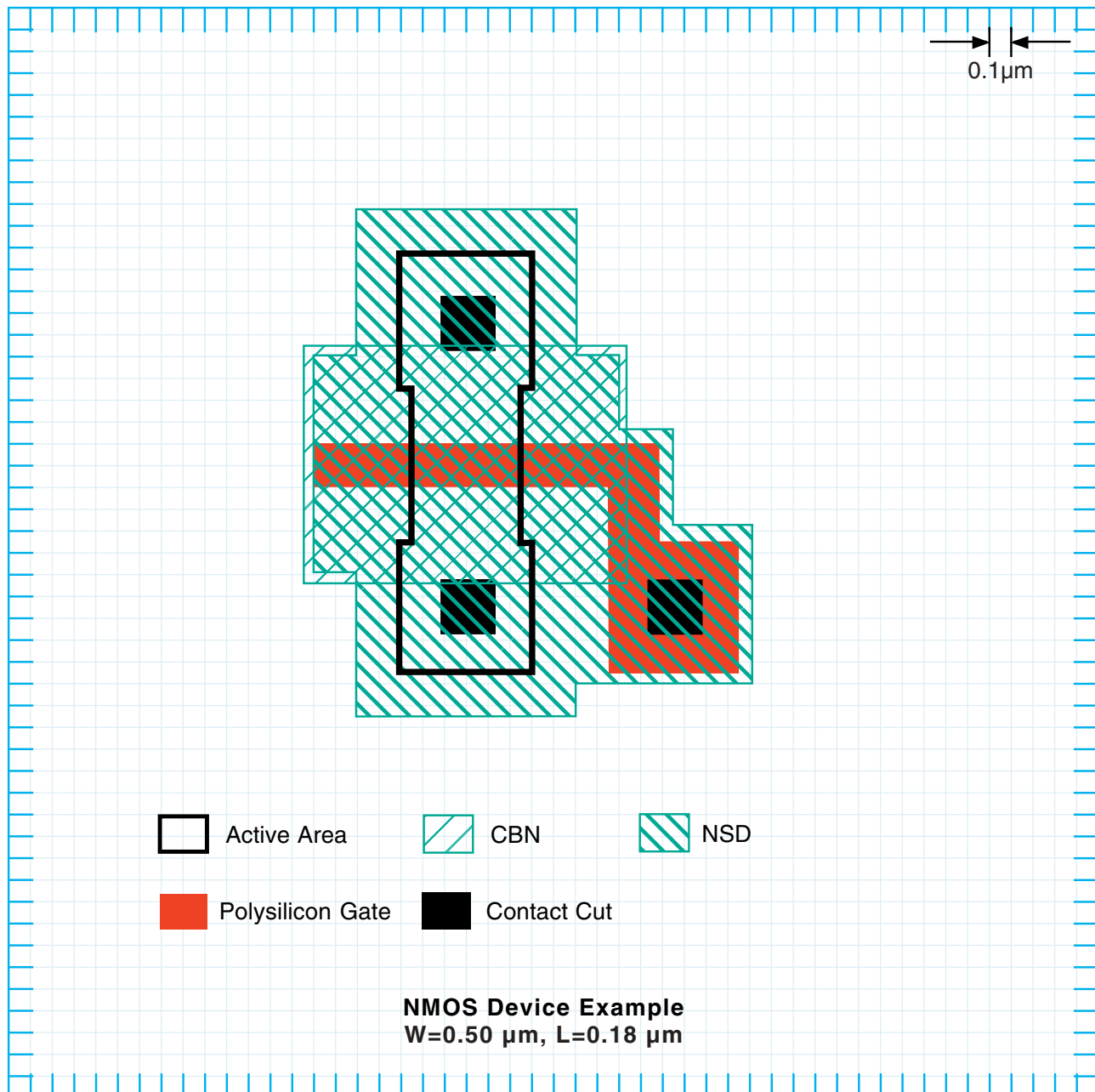

0.1μm

| | Active Area | | CBN | | NSD |

Polysilicon Gate   Contact Cut

NMOS Device Example
W=0.50 μm, L=0.18 μm

FIGURE DN-4

MITLL 0.18 µm Low Power FDSOI CMOS Design Notes and Examples
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are at their minimum allowed values. For devices in which gate length control is especially important, the distance from gate extension poly to active, corresponding to rule 9.5, should be increased to 0.35 µm.

NMOS and PMOS Body Implant Surrounds

Figure DN-5 shows a sample layout of a 0.6 µm by 0.18 µm PMOS device. Note that the CBP surround on the PMOS channel is the same as the CBN surround on the NMOS channel
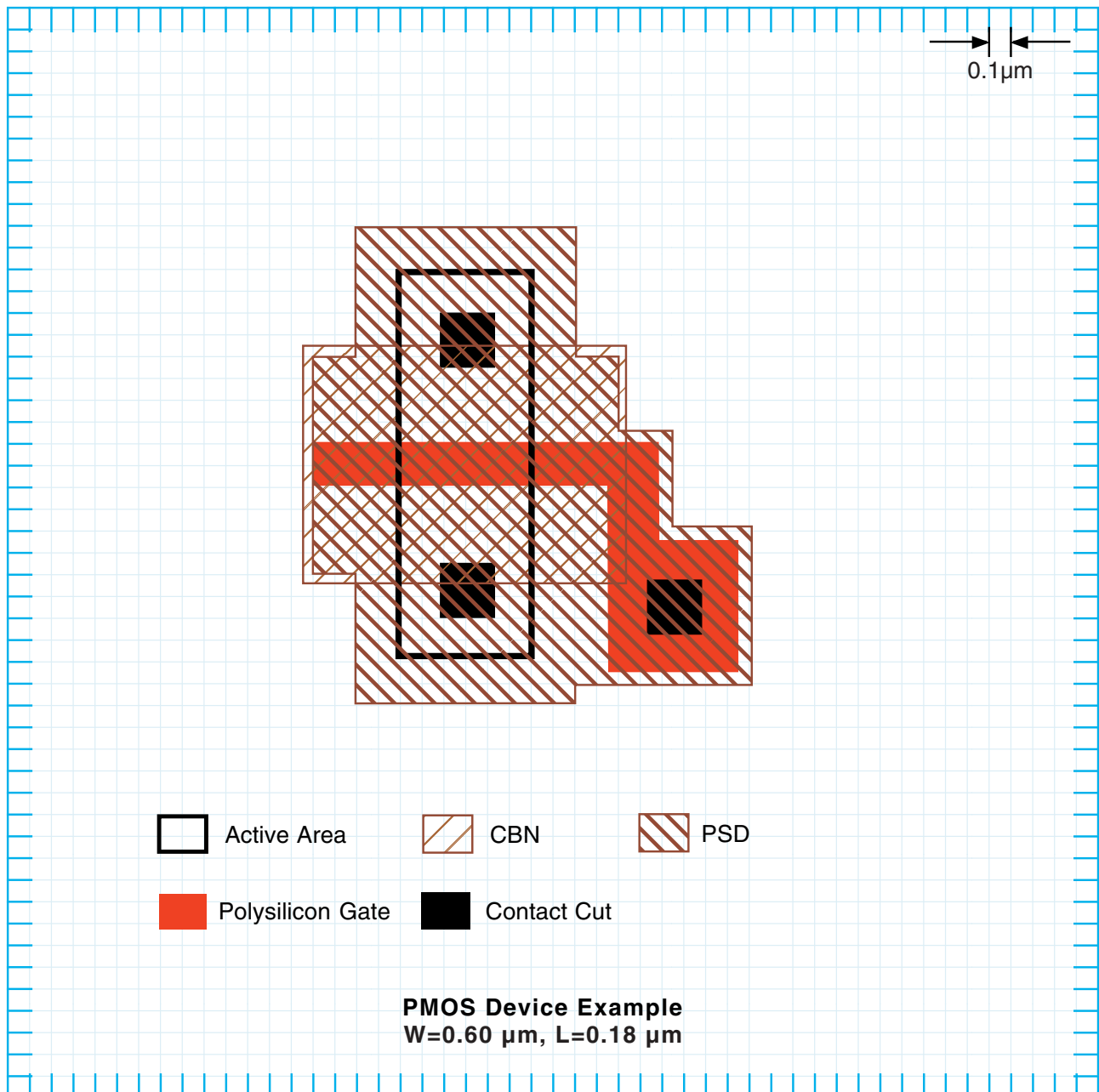

0.1µm

Active Area   CBN   PSD

Polysilicon Gate   Contact Cut

PMOS Device Example
W=0.60 µm, L=0.18 µm

FIGURE DN-5

illustrated in figures DN-3 and DN-4. An attempt has been made to make the layout rules for the MITLL FDSOI process symmetric, with CBN rules corresponding to CBP rules, and NSD rules corresponding to PSD rules.

Edge Effects

Since this is a mesa-isolated process, the standard NMOS and PMOS devices illustrated in figures DN-3 through DN-5 each include parasitic MOS devices at the island edges. A schematic cross section of a typical device is shown in figure DN-6. These parasitic edge devices result in poor threshold voltage control. In addition, they have been shown to increase device noise considerably, sometimes by several orders of magnitude. In the majority of MITLL FDSOI process versions, these edge effects are minimized through the use of a sidewall implant. (An alternative process option that is available in selected process versions uses shallow trench isolation to effectively planarize the active area topography over which the polysilicon is formed.) It is important that the designer understand that post-processing of layout data will be performed in order to create the appropriate sidewall implant masks.

In addition, it should be understood that it is possible to completely eliminate edge effects by designing with devices that have no edge as drawn. See the section on "Special Purpose MOS Structures" for more information on edgeless devices.
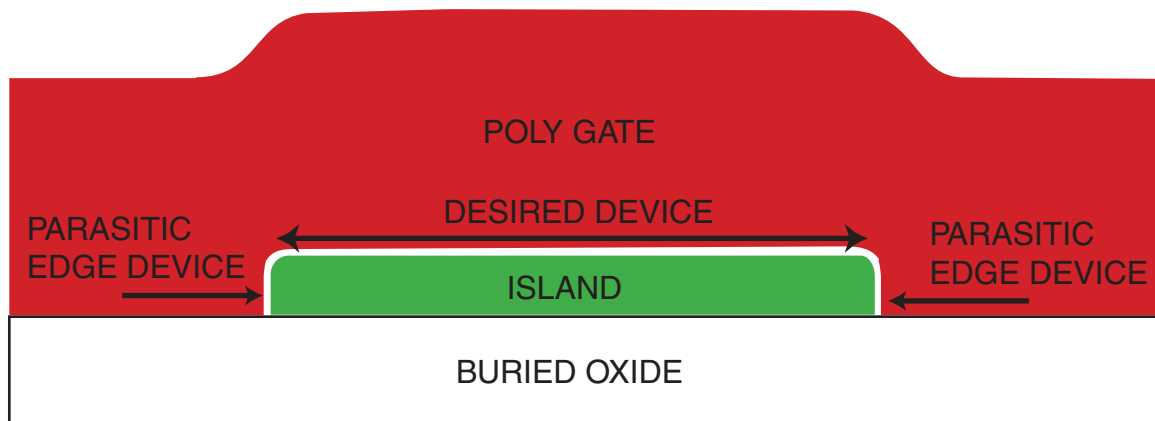

FIGURE DN-6

Layout Post-processing For Sidewall Implants

To avoid formation of parasitic edge transistors, layout data will be post-processed by MITLL to allow for sidewall implants. This operation will create the required sidewall implant mask layers, and will adjust the size of active islands slightly to ensure that MOS channel widths correspond to the drawn data. This post-processing is important for proper operation of MOS devices. Occasionally, it is necessary in a design to suppress this post-processing. This is

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most often the case when non-standard devices such as depletion-type MOS transistors are used. The ACTXPP layer is provided to allow for such cases. This active island layer will receive no sidewall post processing. If you plan to use this layer in a design, please contact MITLL for more information on its proper use.

An illustration of a typical post-processed MOS layout is shown in figure DN-7. Note that the drawn active area has been oversized to form ACTEXP, and that sidewall implant regions defined by SWNCH have been generated. Note that the device width is now determined by
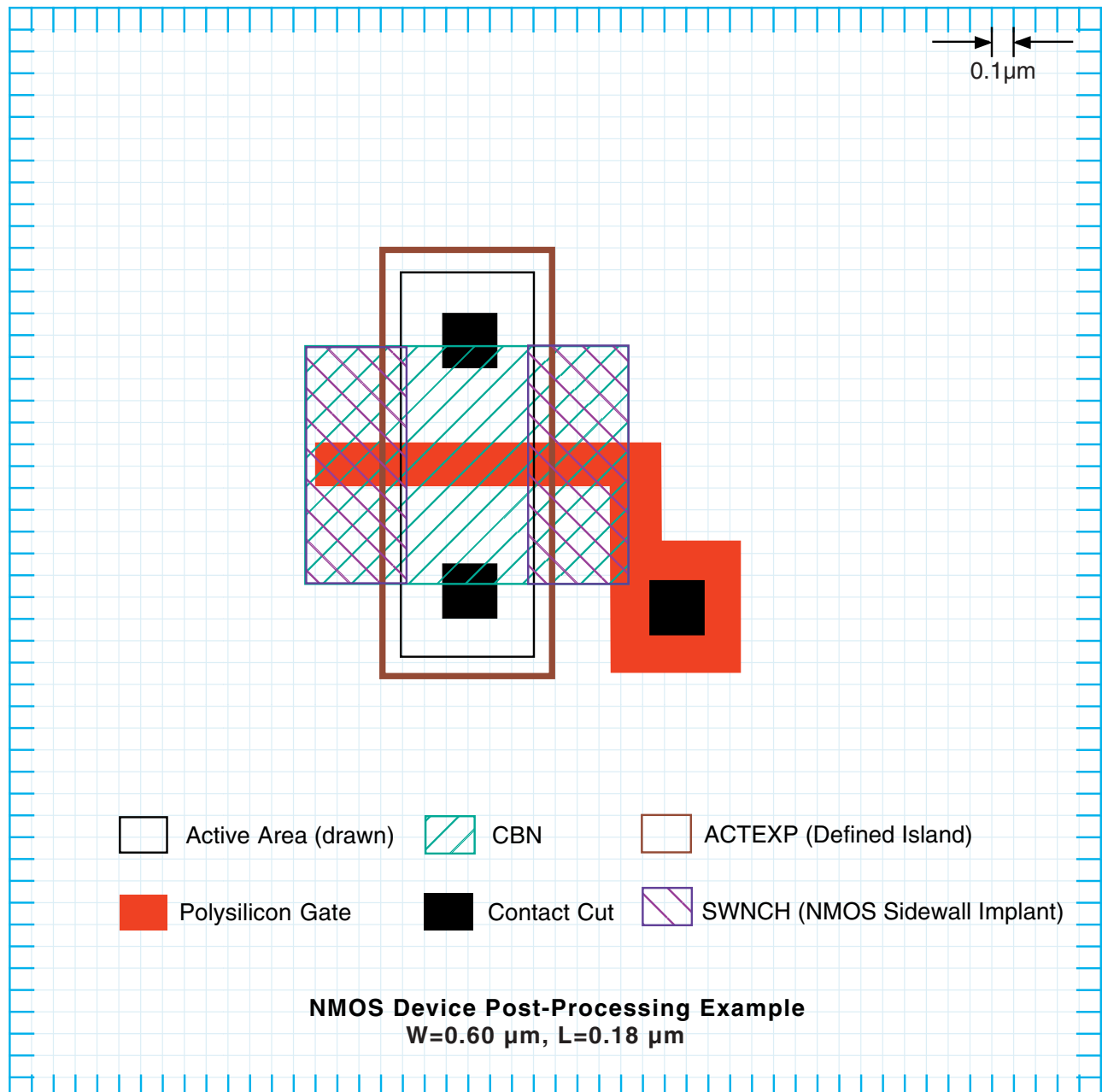

0.1µm

| | Active Area (drawn) | | CBN | | ACTEXP (Defined Island) |
| | Polysilicon Gate | | Contact Cut | | SWNCH (NMOS Sidewall Implant) |

NMOS Device Post-Processing Example
W=0.60 µm, L=0.18 µm

FIGURE DN-7

the boundaries created by the sidewall implants, and not by the island edge. The automatic generation algorithm and corresponding sidewall implant process is designed so that this diffusion-determined width of the device corresponds to the drawn active width.

The generated layers ACTEXP and SWNCH are never drawn by the designer. These are generated by MITLL, and the rules for generation of these layers are determined by process-related tradeoffs. Hence, the sidewall implant mask will not necessarily look like that shown in figure DN-7. The designer should keep in mind that post-processing will be performed on the layout, and that further information on the specifics of the sidewall process is available from MITLL on a case-by-case basis.

To eliminate edge effects, a number of possible edgeless device structures are suggested. These include the ring structure, the H-gate, and the source-side body contacted device. Examples are presented in the "Special Purpose MOS Structures" section of these notes.

Effect of Floating Body on Drain Current

The floating body node of SOI MOS devices can be considered as the base of a parasitic bipolar transistor. At higher drain-source voltages, impact ionization current charges this node, resulting in the "kink effect." Typical drain current characteristics are included in the "Device Characteristics" section of this guide. At room temperature, a good body contact has been shown to eliminate this kink. This is confirmed by tests of several H-gate and source-side body contacted device structures. At cryogenic temperatures, however, the body contacts failed to eliminate the kink effect. Body contact designs are discussed in the "Special Purpose MOS Structures" section of these notes. It is strongly recommended that sensitive devices be biased below the kink region.

Effect of Floating Body on Noise

A large increase in device noise has been observed in the kink region. For this reason, it is recommended that noise-sensitive devices be biased below the kink.

Special Purpose MOS Structures

In addition to the standard NMOS and PMOS layouts described in the previous section, several special purpose MOS layouts are described in this section.

Edgeless Annular Devices

Figure DN-8 shows an edgeless annular PMOS. Edge effects are eliminated, resulting in better threshold control and lower noise. The device width is approximately equal to the
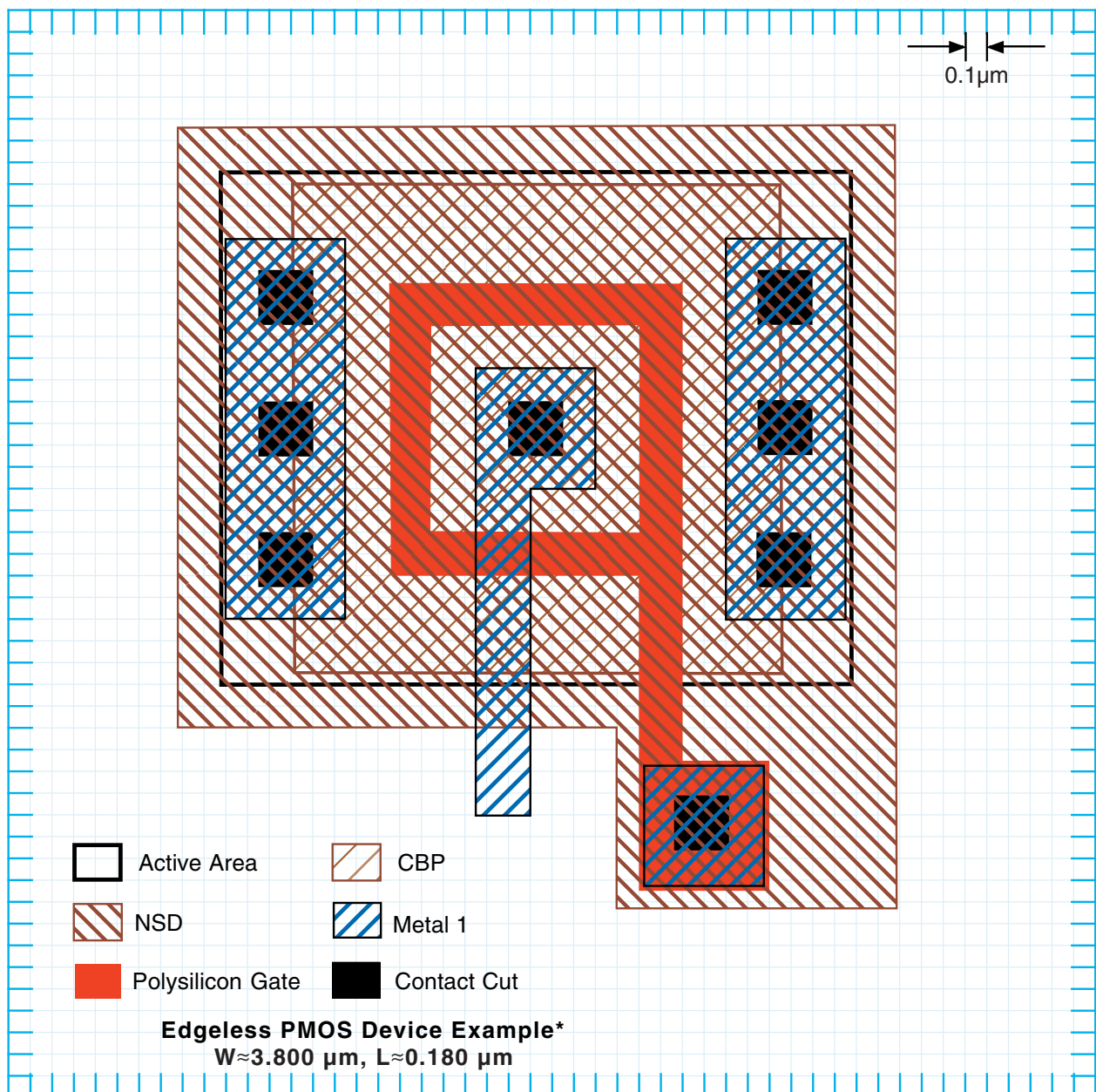

0.1µm

Active Area	CBP
NSD	Metal 1
Polysilicon Gate	Contact Cut

Edgeless PMOS Device Example*
W≈3.800 µm, L≈0.180 µm

FIGURE DN-8

inside perimeter of the gate. It should be noted that sharp drawn corners are rounded and bloated by optical effects, changing the effective physical length and width. This effect is reduced in structures that do not have sharp corners. Matching of ring gate MOS devices has not been characterized.

Source-Side Body Contacted (SBC) Devices

The layout for an 8 µm by 0.5 µm source-side body contacted PMOS device is illustrated in figure DN-9. On the source side of the device, PSD has been replaced with NSD in three sections to create body contacts. The diode formed between NSD and PSD regions is shorted by silicide. No metal contact to the body contact regions is required, as they are already shorted to the source.   Since the body of every SBC device is shorted to the source by silicide, the device is asymmetric, and thus the source and drain can not be exchanged.
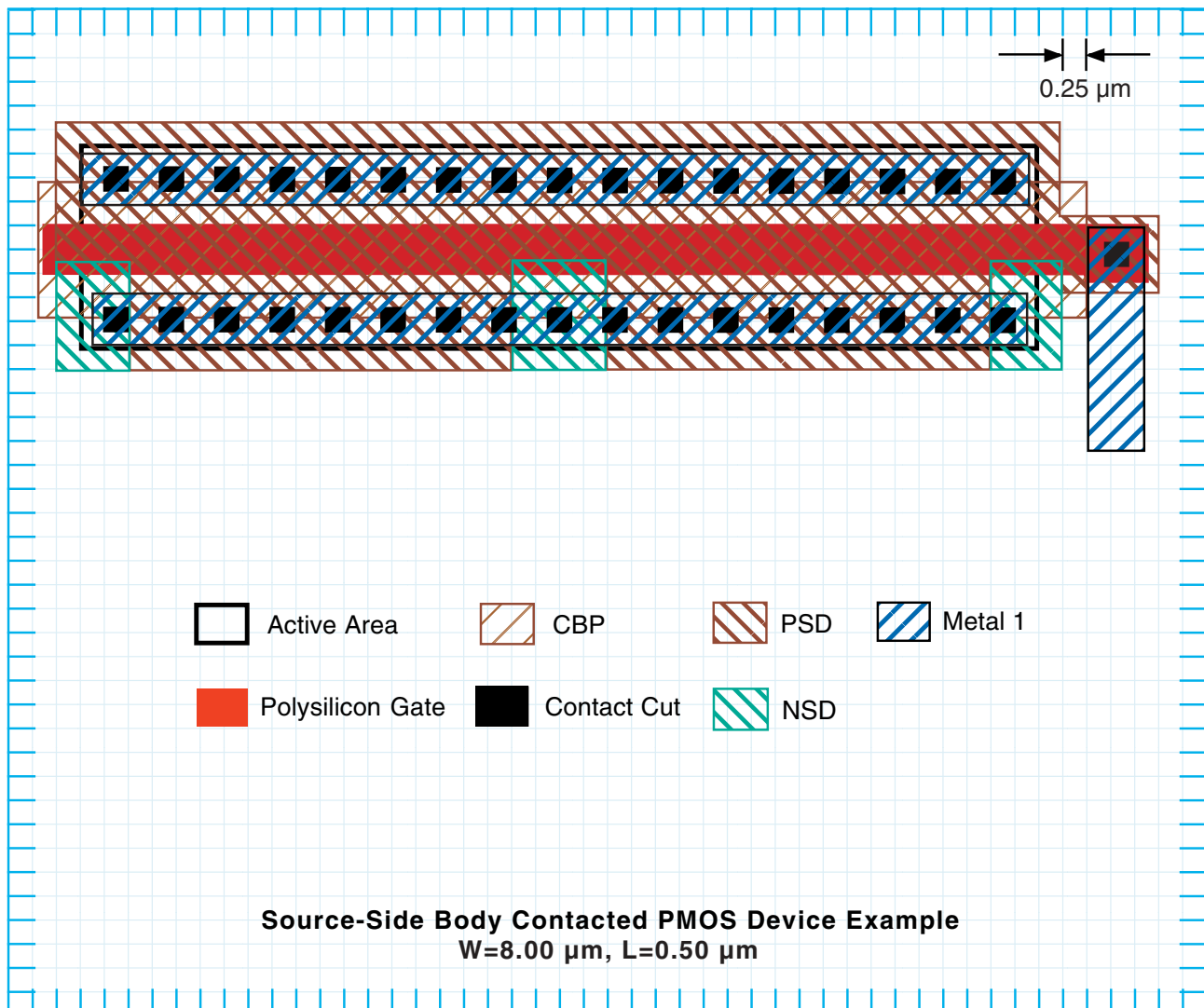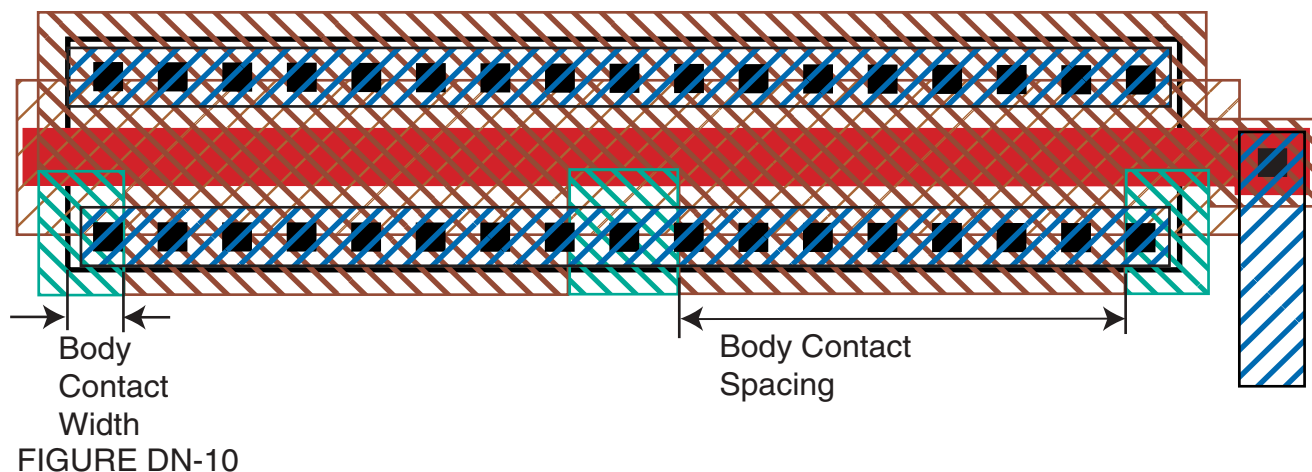

Source-Side Body Contacted PMOS Device Example
W=8.00 µm, L=0.50 µm

FIGURE DN-9

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Body
Contact
Width

Body Contact
Spacing

FIGURE DN-10

For SBC devices at room temperature, a body contact separation of 8 µm effectively eliminated the DC kink at higher drain voltages. At cryogenic temperatures, these body contacts were not effective. Body contacts separated by less than 8 µm have not been characterized. A minimum body contact width of 0.5 µm is recommended. The definition of body contact width and spacing are illustrated in figure DN-10.

Note that the body contact NSD implants overlap the gate by 0.15 µm on the SBC device illustrated in figure DN-8. This is slightly larger than the minimum overlap of 0.1 µm specified by rules 12.9 and 13.9. A sufficient overlap of the body contact implant is necessary to ensure that alignment error does not affect body contact function. By increasing the overlap on both sides slightly to a more conservative 0.15 µm, yield may be increased.

It is also important to remember that device threshold is sensitive to gate doping, and local threshold variation can occur as a result of body contact implants. Care should be taken to ensure that matched transistors have identical regions of opposite-type poly doping.

In SBC Devices, the device width is determined by the body contact implant edges. Thus there is some error due to dopant diffusion. This should be taken into consideration when using a set of devices in which a particular ratio of transconductance values is desired. Due to dopant diffusion considerations, the effective width of narrow SBC devices is not precisely predictable.

The SBC structure in figures DN-9 and DN-10 may be considered to be edgeless in strong inversion, where current is dominated by drift. In subthreshold, there may be some small edge current contribution. The amount of edge current contribution in the latter case may be strongly affected by gate length, body contact width, and alignment error. However, this behavior is not well-characterized. It is recommended but not required that the CBN or CBP body implant be drawn with a 0.450 µm surround on the intersection of poly and active rather

than with a 0.450 µm surround on the channel region as specified in rules 4.2 and 5.2. This will help ensure that the active edges bordering the body contact regions receive sidewall implants.   Annular Gate SBC devices and H-gate devices may also be used to ensure that the device is truly edgeless. If you have any questions concerning the efficacy of a particular body contact geometry, please contact MITLL.

H-Gate Devices

The layout for an 8 µm by 0.5 µm H-gate PMOS device is illustrated in figure DN-11. In this structure, poly lines are used to prevent the diodes between NSD and PSD regions from being shorted by silicide. The width of these lines must be at least 0.2 µm to allow for a 0.1 µm overlap of both NSD and PSD. It is strongly recommended that these lines be drawn slightly wider, i.e. 0.3 µm to allow for a more conservative 0.15 µm overlap for higher yield.
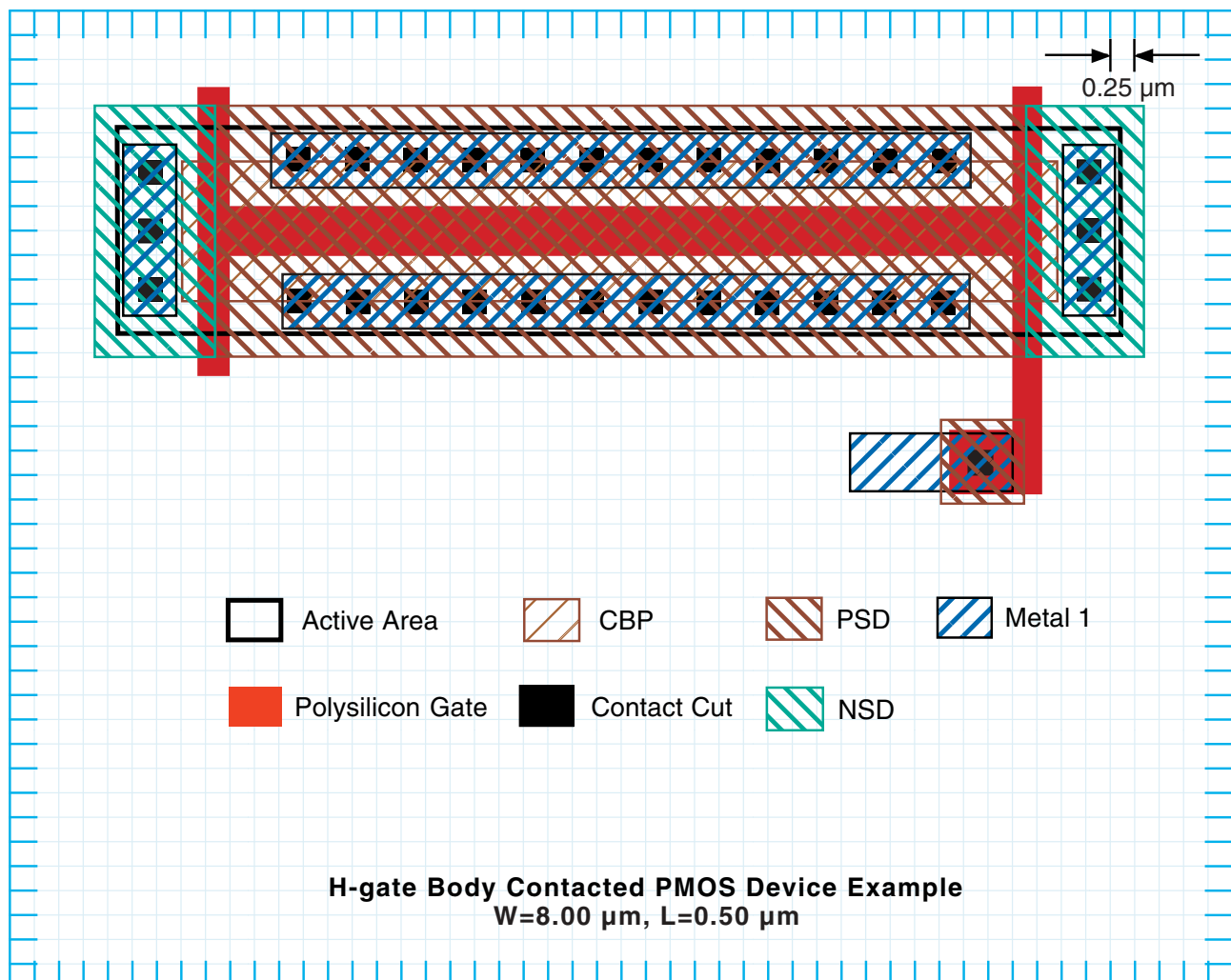

0.25 µm

| | Active Area | | CBP | | PSD | | Metal 1 |
| | Polysilicon Gate | | Contact Cut | | NSD | | |

H-gate Body Contacted PMOS Device Example
W=8.00 µm, L=0.50 µm

FIGURE DN-11

However, it is also recommended that these lines not exceed this 0.3 μm minimum feature width to maximize the effectiveness of the body contact.

For narrow transistors, the T-gate is a possible variation on the H-gate layout which provides a body contact while maintaining device symmetry between the source and drain. A T-gate is drawn with an H-gate like body contact on one edge of the channel, and a standard mesa edge on the other. Since the T-gate device is only edgeless on one side, parasitic edge effects are present in this structure.

The discussion of body contact effectiveness versus width and temperature for SBC devices also applies to H-gate and T-gate devices.

Abutting Devices

Since all exposed active and poly surfaces are silicided following poly deposition, abutting devices of opposite types may be used to save area. This is illustrated in figure DN-12.
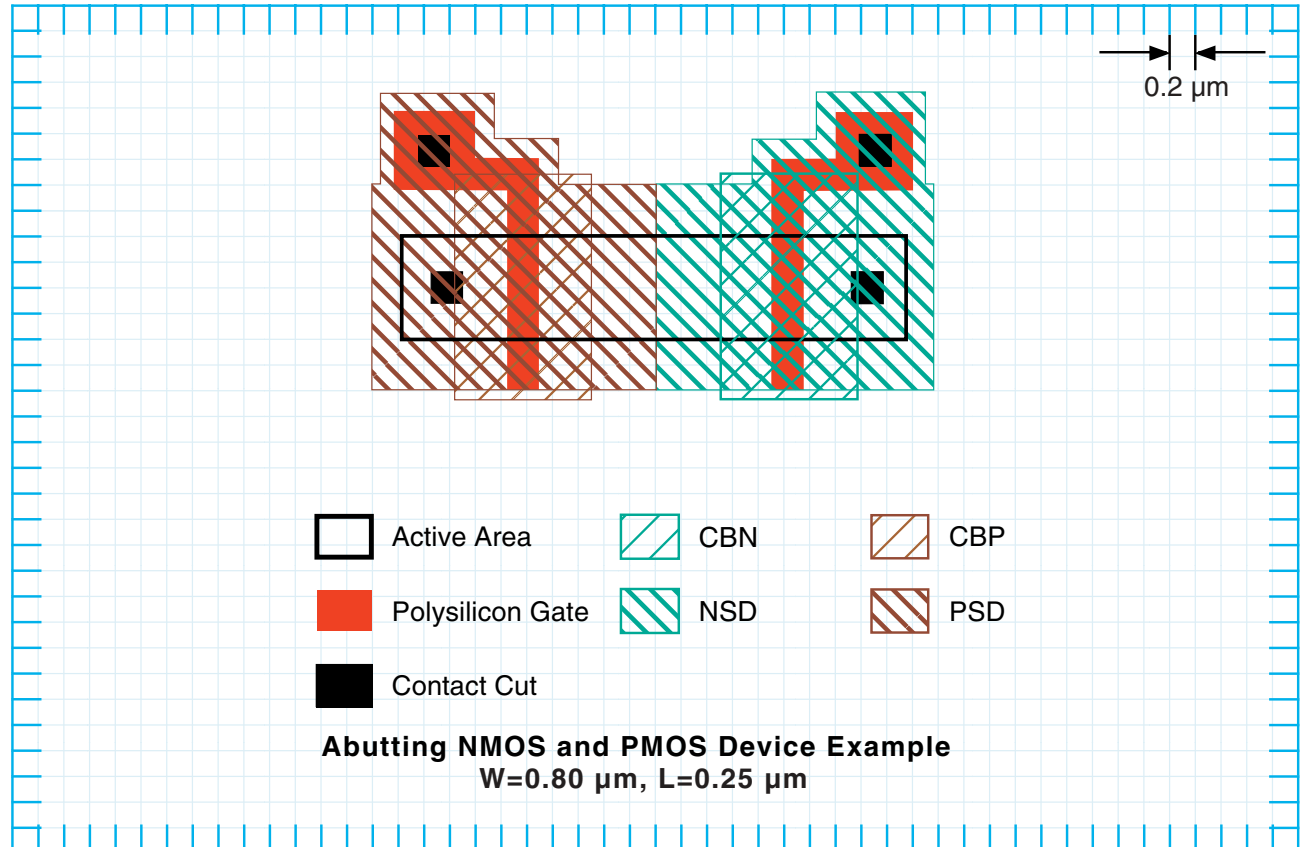

0.2 μm

Active Area	CBN	CBP
Polysilicon Gate	NSD	PSD
Contact Cut		

Abutting NMOS and PMOS Device Example
W=0.80 μm, L=0.25 μm

FIGURE DN-12

Diodes that would ordinarily be formed between such devices are shorted by silicide. Please note, however, that lateral diffusion of dopants in the silicide has not been well characterized. Rules have been included for the benefit of designers who wish to experiment with this feature. The designer should anticipate unexpected results when using abutting devices.

Conductive Lines

Long minimum-width and minimum-gap conductive lines should be avoided unless they are forced by capacitance or density considerations. This applies to all metal and silicided silicon lines. If long, wide parallel lines are used, increased line spacing should be considered.

It is strongly recommended that when silicided active or poly is used as a conductor, the feature should be doped with NSD or PSD. While this is not essential to device operation, it reduces the risk that defects in the silicide will reduce circuit yield. MITLL has attributed some circuit failures to long, undoped poly runs.

Rules 1.5, 1.6, 9.10, 9.11, 17.4, 17.5, 20.4, 20.5, 23.4, 23.5, 26.4, 26.5, 29.4, 29.5, 32.4, and 32.5 place constraints on active, poly and metal pattern densities. Even distribution of active, poly and metal will reduce process variations and increase yield.

Dense Contacts and Vias

Large dense contact and via arrays may cause CMP uniformity problems. Hence it is strongly recommended that for arrays of ten or more contacts and vias, the contact or via spacing be increased by at least 50%.

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Active, Poly and Metal Fill Patterns

Planarization and etch processes are facilitated by relatively uniform metal and poly pattern densities. Rules 1.5, 1.6, 9.10, 9.11, 17.4, 17.5, 20.4, 20.5, 23.4, 23.5, 26.4, 26.5, 29.4, 29.5, 32.4, and 32.5 place constraints on active, poly and metal pattern densities. Even distribution of active, poly and metal will reduce process variations and increase yield.

In order to meet active, poly and metal density constraints, dummy patterns should be added to the layout in open areas. The design layers ACTF, POLYF, M1F, M2F, M3F, M4F, M5F and MTLRFF are provided for this purpose. The poly reticle will be produced based on the union of POLYF with POLY. Likewise the metal reticles will be produced based on the union of M1F, M2F, M3F, M4F, M5F and MTLRFF with M1, M2, M3, M4, M5, and MTLRF respectively. The active island reticle will be produced based on the union of post-processed active layer ACTEXP and ACTF. This use of logical layers is intended to simplify computer-aided design. ACTF, POLYF, M1F, M2F, M3F, M4F, M5F and MTLRFF should only be used for fill features that do not contribute to the functionality of the design.

Fill patterns may be floating or grounded. For floating poly fill, the pattern illustrated in figure DN-15b is recommended. This consists of 3.7 µm poly squares with centers spaced 10 µm apart and 11 µm clearance to circuit poly. The resulting fill pattern density is about 14%. For
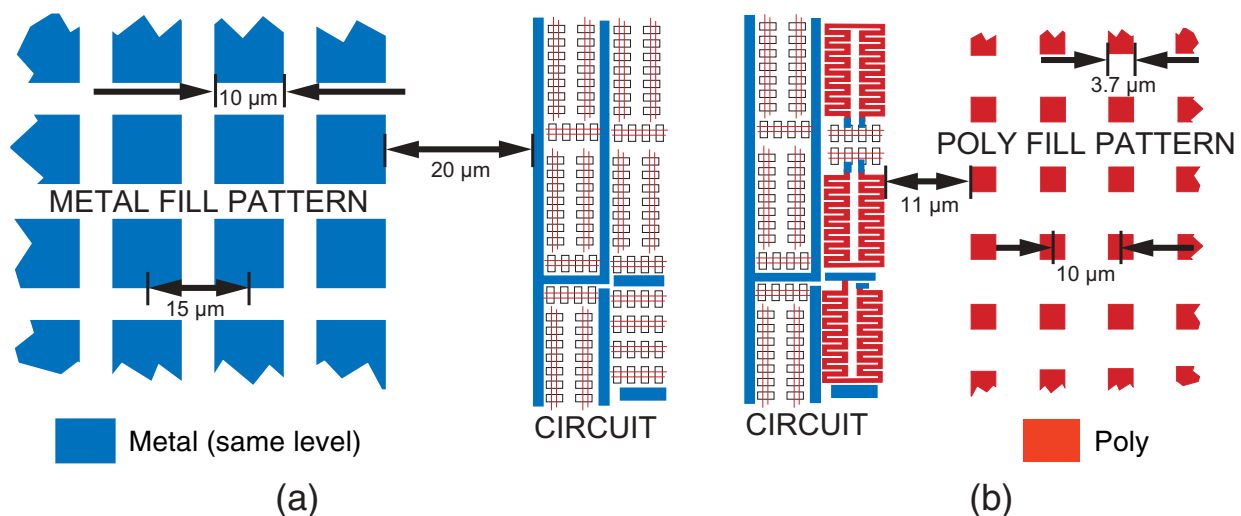

FIGURE DN-15

MITLL 0.18 µm Low Power FDSOI CMOS Design Notes and Examples

floating metal fill, the pattern illustrated in figure DN-15a is recommended. This consists of 10-µm metal squares with centers spaced 15 µm apart and 20 µm clearance to same-level circuit metal. The resulting fill pattern density is about 44%. For active islands, a fill pattern consisting of 7-µm squares on 10-µm centers gives a 49% pattern density.

Consideration of the parasitic capacitances to fill stuctures is essential. Unwanted coupling of signals through floating fill features is possible. In some sensitive circuit areas, the designer may choose to use grounded fill patterns to achieve required pattern densities. When grounded fill features are used, however, capacitances to fill patterns may still contribute to circuit delays. Therefore it is especially important that fill-related parasitics be included in simulations.

MITLL will generate fill patterns in unused areas unless the NOFILL layer is present. When NOFILL is used, it is the responsibility of the designer to ensure compliance with all layer density specifications. Non-compliant layouts will be rejected, unless MITLL has approved a written application for a waiver of density constraints. This application must be submitted at least one month in advance of the design submission deadline to allow for consultation with the designer and MITLL process engineers. Contact MITLL for more information.

Automatic Generation of Fill Patterns by MITLL

During layout post-processing, MITLL will generate fill patterns in open areas, provided that no feature exists on the NOFILL layer in that region. This routine is summarized here. Hote that the autogeneration routing is subject to change, and that it is strongly recommended that for timing-sensitive designs for which fill will be generated at MITLL, the designer should obtain a copy of the current fill generation algorithm for use during the design process. In addition, the post-autogeneration layout database will also be made available for simulation of fill effects. Also note that in the following description, several steps which ensure the elimination of sub-design rule gaps and spikes are not included. Also excluded are con-straints that prevent generation of fill patterns near 3-D vias.

FILL GENERATION ROUTINE

Step	Layer(s)	Description
1	Active, Poly	Active and poly are OR'ed together and scaled by 6 µm to form region ACTR1, and by 2 µm to form region ACTR2. A fill feature is then formed by the operation ACTR1 AND (NOT ACTR2). This leaves a 4 µm fence of active fill around the circuit area. This fence is shown in figure DN-15 (c).
2	Active	Squares of active fill are generated. These are 7 µm x 7 µm, with 10-µm centers. The standoff to existing ACT, POLY, ACTF or POLYF, including the fence of step 1, is 10 µm.
3	Poly	3.7 µm squares are generated with 10-µm centers by sizing the active fill features generated in step 2.

60

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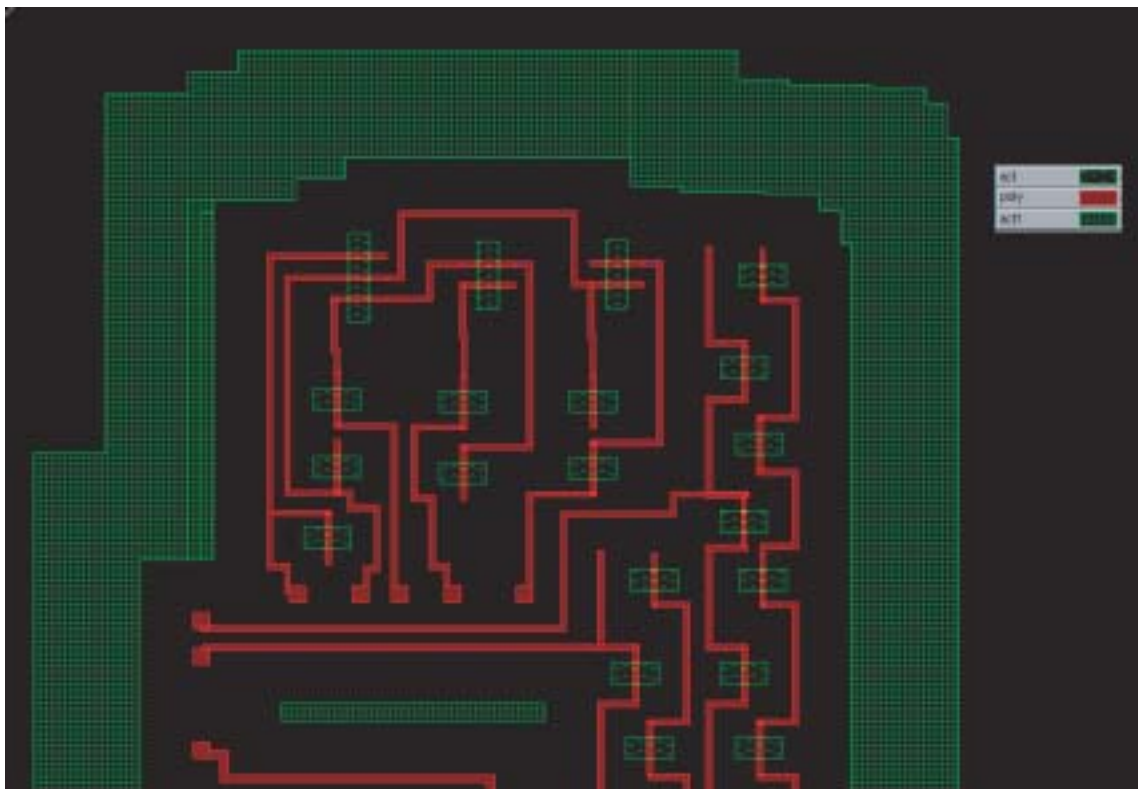
FIGURE DN-15 (c)

FILL GENERATION ROUTINE (cont.)

Step	Layer(s)	Description
4	All Metals	Metal fill features are generated as 10-µm squares on 15-µm centers. The standoff to existing metal is 20 µm and the standoff to existing metal fill is 5 µm.

Note that fill is generated for the entire top-level cell extent, except in regions which have the NOFILL flag layer.

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Layout Acceptance Rules

Design Grid

Layouts must be done to a 0.025 µm (25 nm) grid at the wafer. I.e. the smallest fundamental unit (lambda) is 0.025 µm and all polygon corners in the layout **must** be on a 0.025 µm grid. **Non-compliance with the 0.025 µm grid may lead to reticle errors and unpredictable results.** Submissions with structures, sub-structures, or extents placed off this grid will not be accepted.

Layout Database Format

GDSII is the preferred form for all layout submissions. CIF is an acceptable alternative if GDSII is not possible. A list of GDSII layer numbers and CIF layer names is included in the "Design Layers" section of this guide.

In the layout database, the precision must be 1000 with a unit length in µm (1E-6).

Any round-ended paths (GDS PATH TYPE 1) must be flattened to polygons prior to submission.

All data must be placed inside the intended rectangular extent of the top structure. Any data placed outside will result in additional fill pattern generation in that region during post-processing, and consequently will "grow" the submission to a larger unintended extent.

The following GDS data types or attributes are not supported and should not be in-cluded:

> BOX
> NODE
> ABSOLUTE MAGNIFICATION
> ABSOLUTE ANGLES
> NON-ORTHOGONAL REFERENCES

Identifier in Top-Level Cells

All top-level cells must have instantiated within them a label containing a brief design identifier and the name of the submitting organization. It is strongly encouraged that this be drawn in top level metal so that chips may be more easily identified after fabrication.

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Contact Information Required

Accompanying all data, contact information must be provided for the contributor so that we may follow up with questions and other information.

Mandatory Rule Set

This section lists the minimum rule set that **must** be followed in order for a layout to be accepted for inclusion in an MITLL FDSOI multiproject run. Deliberate violation of the rules listed below requires the explicit permission of MITLL. The purpose of this rules subset is to protect other designs on the run. It is incumbant on the designer to accept all responsibility for the effects of rules violations on his own design.

General Polygon and Path Rules

Rule	Description	Constraint
0.1	Minimum feature width	0.200 μm
0.2	Minimum feature spacing	0.200 μm
0.3	Acute angles	prohibited

Density Rules (enforced after execution of MITLL fill generation script)

Rule	Description	Constraint
1.5	Required minimum active density within any 1 mm x 1 mm window	40%
1.6	Required maximum active density within any 1 mm x 1 mm window	40%
9.10	Required minimum poly density within any 1 mm x 1 mm window	10%
9.11	Required maximum poly density within any 1 mm x 1 mm window	20%
17.4	Required minimum metal 1 density within any 1 mm x 1 mm window	30%
17.5	Required maximum metal 1 density within any 1 mm x 1 mm window	50%
20.4	Required minimum metal 2 density within any 1 mm x 1 mm window	30%
20.5	Required maximum metal 2 density within any 1 mm x 1 mm window	50%
32.4	Required minimum MTLRF density within any 1 mm x 1 mm window	30%
32.5	Required maximum MTLRF density within any 1 mm x 1 mm window	50%

MITLL 0.18 µm Low Power FDSOI CMOS Submission Guidelines
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Important Note

MITLL reserves the right to modify the submission requirements at any time. It is strongly recommended that designs be made compliant with all design rules so that with future modifications to autogeneration routines, mask specifications, etc., the design data remains compatible with the layout post-processing, mask fabrication and wafer fabrication processes.

MITLL 0.18 µm Low Power FDSOI CMOS Device Models

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Spice Parameters (BSIM3v3.2)

The following NMOS SPICE parameters were derived from measured I(V) curves on recently fabricated FDSOI transistors using Silvaco's UTMOST parameter extraction tool. The model fits the data very well except that the kink effect is *not* represented. The PMOS parameters were derived with much less precision but they represent the on and off current of recent devices reasonably well. **For the convenience of the designer, these models assume that the device width and length will be specified as drawn.** Thus a device with a 0.18 µm gate as fabricated is specified as having a drawn gate length of 0.2 µm.

The parameters are to be used in the bulk Si MOSFET model BSIM3v3.2. The body effect parameters K1 and K2 have been adjusted to properly represent the dependence of threshold voltage on source to *wafer* voltage instead of the source to *body* voltage which SPICE thinks is being modeled. For this subterfuge to work correctly, the designer's SPICE netlist should include a fictitious contact between each NMOS body and VSS and between each PMOS body and VDD. For body-contacted devices, this fictitious contact should replace the actual body contact connection. Note that there is an implicit assumption that the wafer effect is dominant over the body effect. This condition holds true in FDSOI for most bias conditions. The body effect may become significant for some weak inversion bias conditions; hence for body contacted devices in weak inversion, this model may not be optimal.

The parameter CJ represents capacitance of the source and drain regions to the wafer through the buried oxide, modeled as being nearly voltage independent. The value given is the worst case for a 190-nm buried oxide, representing the DC capacitance to a substrate inversion layer below the buried oxide. For anything but very low frequency the actual "junction" capacitance will include a wide depletion layer in the SOI handle wafer and hence will be about 40% of the value given for the digital process. For the RF process a thicker buried oxide is used which reduces the worst case value by a factor of two, and the depletion layer will be much thicker. If any participants in previous multiproject runs have results which quantify the effective junction capacitance in FDSOI, MITLL would like to hear about it.

The kink effect causes an abrupt increase in the slope of the $I_D(V_D)$ curves of longer channel nmos transistors at V_{DS} a little above 1 V, particularly at gate voltages close to threshold; see the graphs included in the "Device Characteristics" section of this Design Guide. The actual DC current in that region is higher than the modeled current, and the output conductance is much higher than the modeled value. The effect is frequency dependent, maximum at DC, and disappearing for frequencies in the MHz range. A program is now in progress to develop a SPICE model which correctly represents the kink effect in FDSOI transistors.

Note that these SPICE parameters are in Silvaco SmartSpice format. To use these models with HSPICE, set LEVEL=49 and delete the INTCAP and BERK parameters.

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```
.LIB soifet3
*NMOS parameters extracted from data from soifet3 w3 row4,col2, the same data
*sent to Pin Su at UC Berkeley for development of the improved FDSOI model.
*This parameter set is for the BULK bsim3v3.2 model, with parameters K1 and
*K2 adjusted to properly represent the effect of HANDLE WAFER voltage, not
*body voltage.  It includes measured values of gate overlap capacitance and
*"juction" capacitance (i.e. source and drain to handle wafer) in inversion
*or accumulation.  This probably grossly overstates the true CJ, which has
*to be determined by high frequency data fitting.  At worst, CJ for the
*NeoCAD runs will be half the value given, since the buried oxide will be
*twice as thick.  (See ~utmost_data/mos/s3w3/v32.l)
* DATE: Dec 20/01
* LOT: soifet3              WAF: 3
* DIE: r4c2                 DEV: 0.4/0.2d
* Temp= 22
.MODEL AllWandL nmos (                          LEVEL   = 8
+VERSION = 3.2          TNOM    = 22            TOX     = 4.2E-9
+XJ      = 1E-7         NCH     = 6E17          NSUB    = 3E15
+VTH0    = 0.47         K1      = 0.01          K2      = 0.015
+K3      = 6            K3B     = 0             W0      = 0
+NLX     = 0            DVT0W   = 0             DVT1W   = 2E6
+DVT2W   = 0.1          DVT0    = 1.5           DVT1    = 0.35
+DVT2    = 0.12         U0      = 0.041         UA      = 0
+UB      = 1.2E-18      UC      = 0             VSAT    = 8E4
+A0      = 0            AGS     = 0             B0      = 0
+B1      = 0            KETA    = 0             A1      = 0
+A2      = 0.99         RDSW    = 340           PRWG    = 0
+PRWB    = 0            WR      = 1             WINT    = 5E-8
+LINT    = 2.7E-8       DWG     = -9E-8         DWB     = 0
+VOFF    = -0.13        NFACTOR = 0.5           CIT     = 0
+CDSC    = 1E-3         CDSCD   = 0             CDSCB   = -5E-4
+ETA0    = 0.9          ETAB    = 0             DSUB    = 1
+PCLM    = 1.5          PDIBLC1 = 0             PDIBLC2 = 0
+PDIBLCB = 0            DROUT   = 0.3           PSCBE1  = 1E8
+PSCBE2  = 0            PVAG    = 0.5           DELTA   = 0.01
+NGATE   = 1E20         ALPHA0  = 1E-8          ALPHA1  = 0.1
+BETA0   = 22           PB      = 10            JS      = 0
+JSW     = 0            MOBMOD  = 1             PRT     = 0
+UTE     = -0.45        KT1     = -0.06         KT1L    = 0
+KT2     = 0            UA1     = 0             UB1     = 0
+UC1     = 0            AT      = 2E5           CAPMOD  = 2
+NQSMOD  = 0            ELM     = 5             XPART   = 0
+WL      = 0            WLN     = 1.11          WW      = 0
+WWN     = 1.5          WWL     = -3E-25        LL      = 0
+LLN     = 1            LW      = 3E-18         LWN     = 1.5
+LWL     = 0            CGSL    = 0             CGDL    = 0
+CKAPPA  = 0.6          CF      = 0             CLC     = 1E-7
+CLE     = 0.6          DWC     = -7.5E-8       CGDO    = 4E-10
+CGSO    = 4E-10        CGBO    = 0             CJ      = 1.7E-4
+MJ      = 0.5          CJSW    = 0             BINUNIT = 1
+IS      = 0            INTCAP  = 1             BERK    = -3          )
*
```

MITLL 0.18 μm Low Power FDSOI CMOS Device Models

(version 5.11.mp5, January 2002)

```
*This pmos model is estimated based on extrapolation plus limited data from
*soifet3 wafer1.
.MODEL EstimatedPmos pmos (                          LEVEL    = 8
+VERSION = 3.2          TNOM     = 22               TOX      = 4.2E-9
+XJ       = 1E-7        NCH      = 6E17             NSUB     = 3E15
+VTH0     = -0.4        K1       = 0.01             K2       = 0.015
+K3       = 1           K3B      = 0                W0       = 0
+NLX      = 0           DVT0W    = 0                DVT1W    = 0
+DVT2W    = 0           DVT0     = 6                DVT1     = 0.5
+DVT2     = 0.1         U0       = 5E-3             UA       = 0
+UB       = 0           UC       = 0                VSAT     = 8E4
+A0       = -10         AGS      = 0                B0       = 0
+B1       = 0           KETA     = 0                A1       = 0
+A2       = 0.4         RDSW     = 550              PRWG     = 0
+PRWB     = 0           WR       = 1                WINT     = 0
+LINT     = 0           DWG      = 0                DWB      = 0
+VOFF     = -0.1        NFACTOR  = 0                CIT      = 0
+CDSC     = 0           CDSCD    = 0                CDSCB    = 0
+ETA0     = 0.03        ETAB     = 0                DSUB     = 0.5
+PCLM     = 3           PDIBLC1  = 0.3              PDIBLC2  = 0
+PDIBLCB  = 0           DROUT    = 0.25             PSCBE1   = 6E8
+PSCBE2   = 1E-10       PVAG     = 0                DELTA    = 0.01
+NGATE    = 8E19        ALPHA0   = 1E-9             ALPHA1   = 0
+BETA0    = 22          PB       = 10
+JS       = 0           JSW      = 0                MOBMOD   = 1
+PRT      = 0           UTE      = -0.55            KT1      = -0.1
+KT1L     = 0           KT2      = 0                UA1      = 0
+UB1      = 0           UC1      = 0                AT       = 3E5
+CAPMOD   = 2           VFBCV    = 1                NQSMOD   = 0
+ELM      = 5           XPART    = 0                WL       = 0
+WLN      = 1           WW       = 0                WWN      = 1
+WWL      = 0           LL       = 0                LLN      = 1
+LW       = 0           LWN      = 1                LWL      = 0
+CGSL     = 0           CGDL     = 0                CKAPPA   = 0.6
+CF       = 0           CLC      = 1E-7             CLE      = 0.6
+DWC      = -7.5E-8     CGDO     = 4E-10            CGSO     = 4E-10
+CGBO     = 0           CJ       = 1.7E-4           MJ       = 0.5
+CJSW     = 0           CJSWG    = 0                MJSWG    = 0
+BINUNIT  = 1           IS       = 0                INTCAP   = 1
+BERK     = -3          N        = 1                 )
*
.ENDL soifet3
```

MITLL 0.18 µm Low Power FDSOI CMOS Device Models
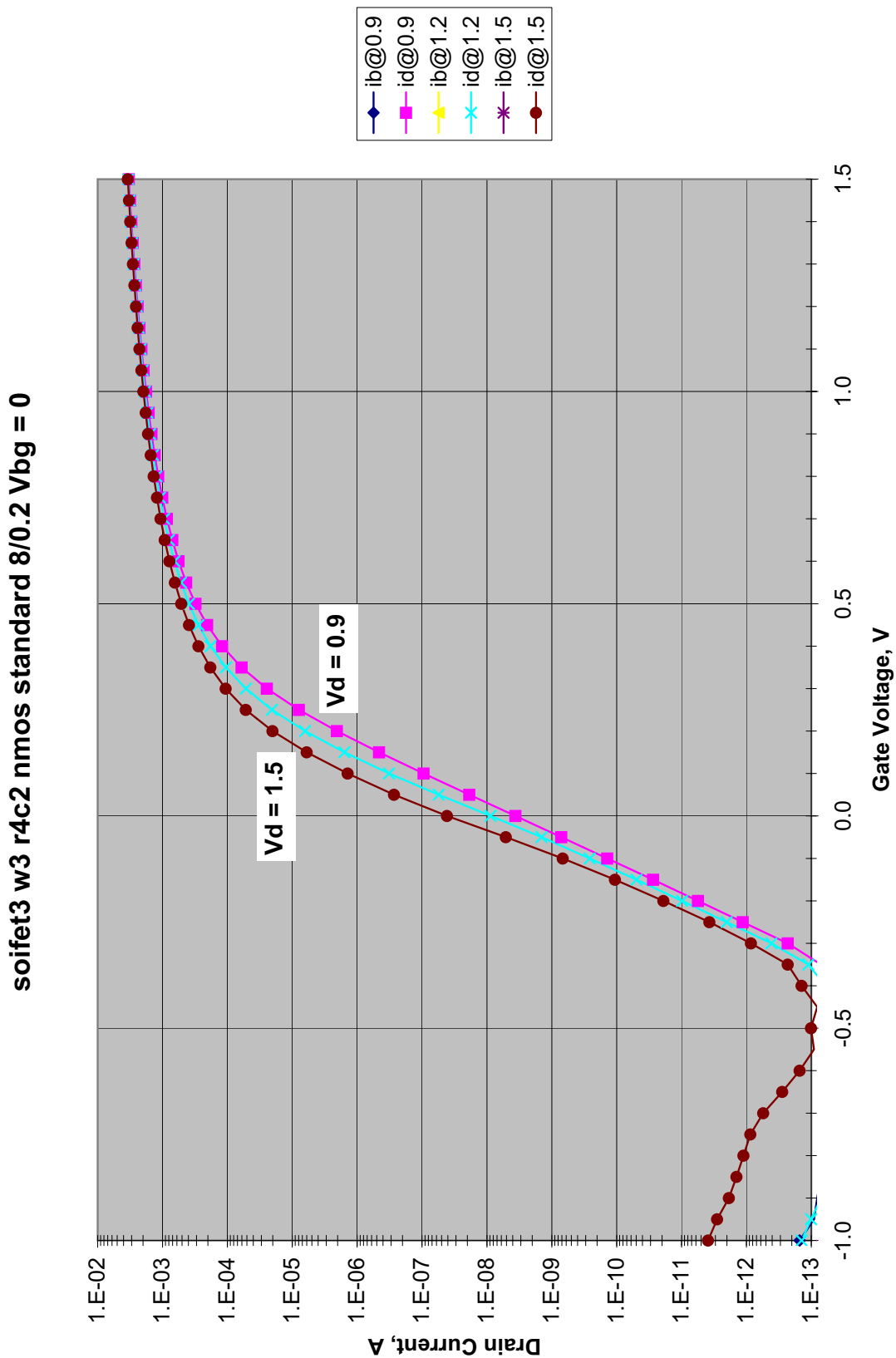(version 5.11.mp5, January 2002)

Device Characteristics (I-V Curves, etc.)

These graphs are typical NMOS and PMOS I(V) curves for the MITLL 0.18 µm low power FDSOI process. **All device sizes are given as drawn.** (A drawn 0.2 µm device will be fabricated with a 0.18 µm poly gate.)

The kink effect appears strongly on the 8 µm wide by 0.5 µm long NMOS device as an abrupt change in slope in the drain characteristic and an anomalously steep subthreshold slope in the gate characteristic. It is much less apparent in the 0.2 µm long NMOS transistor characteristics. The kink is not modelled by the present SPICE model, which assumes a bulk device.
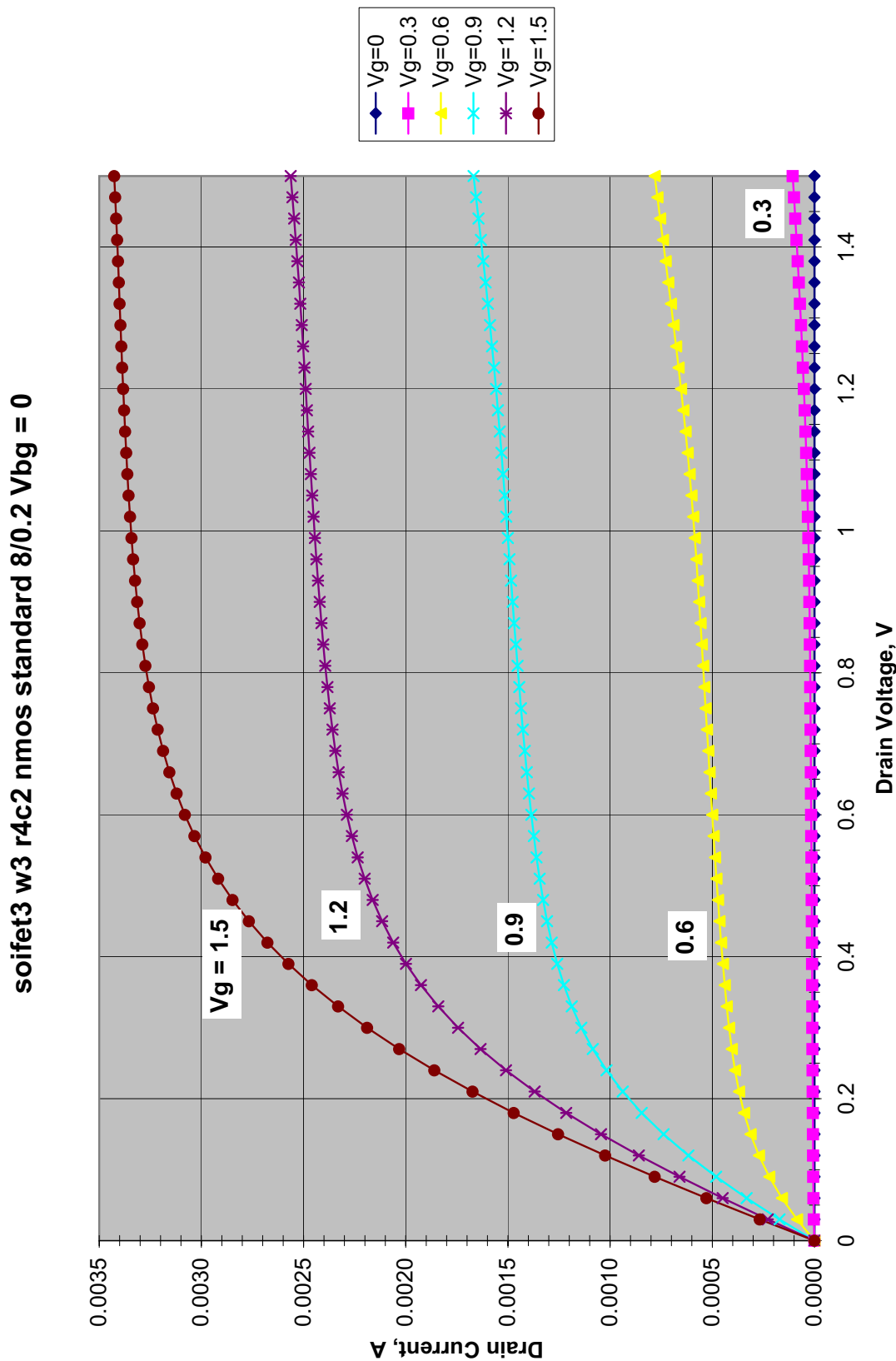
The PMOS curves are from a chip which is representative of the process to be used in upcoming fabrication runs, though they do not exactly fit the SPICE model in this guide. Note that there is no apparent kink effect; it does not occur in PMOS transistors at room temperature or above.

MITLL 0.18 μm Low Power FDSOI CMOS Device Models
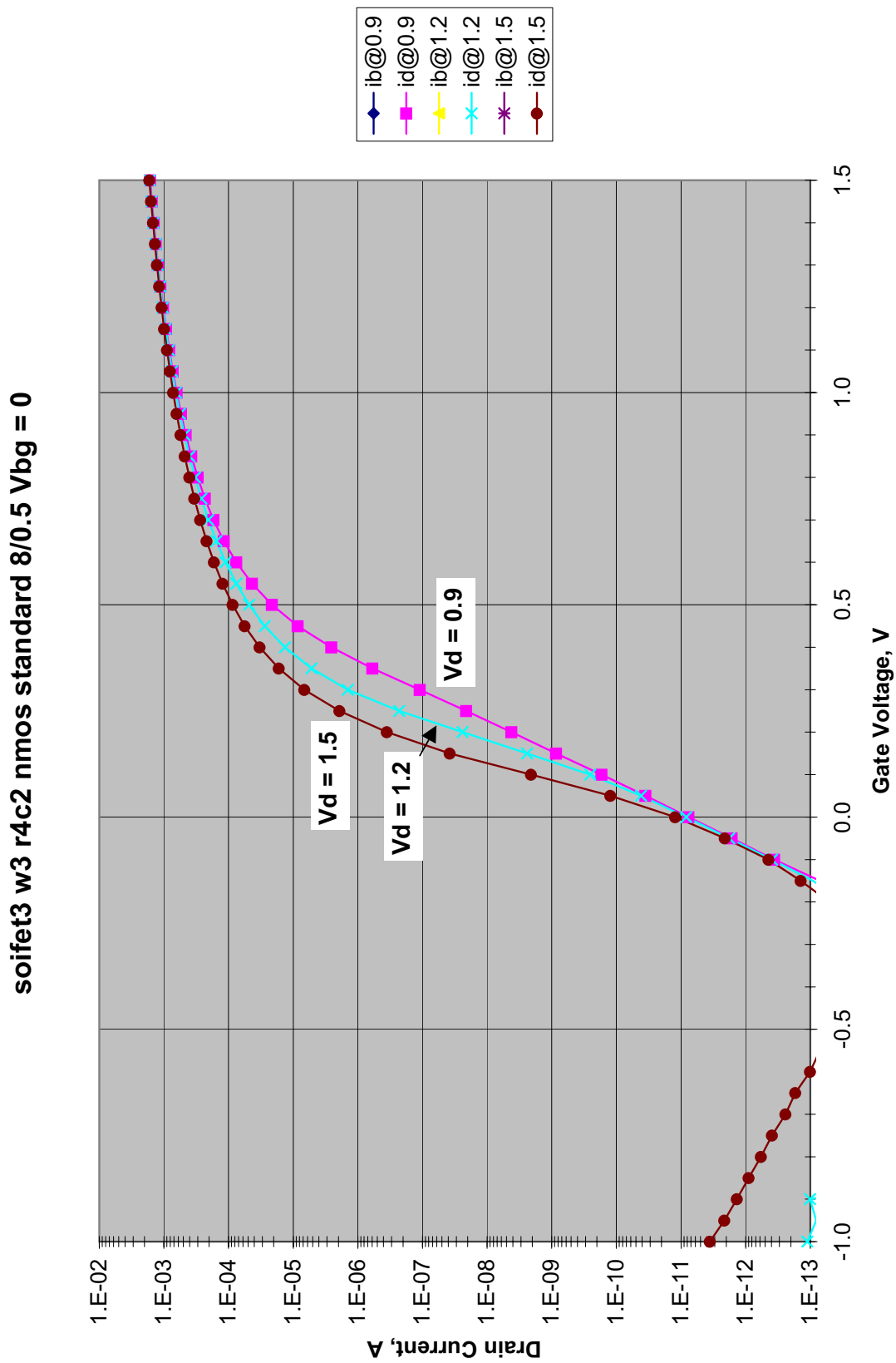
(version 5.11.mp5, January 2002)

soifet3 w3 r4c2 nmos standard 8/0.2 Vbg = 0

Vd = 0.9

Vd = 1.5

Legend:
- ib@0.9
- id@0.9
- ib@1.2
- id@1.2
- ib@1.5
- id@1.5

X-axis: Gate Voltage, V
Y-axis: Drain Current, A

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soifet3 w3 r4c2 nmos standard 8/0.2 Vbg = 0

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soifet3 w3 r4c2 nmos standard 8/0.5 Vbg = 0

Legend:
- ib@0.9
- id@0.9
- ib@1.2
- id@1.2
- ib@1.5
- id@1.5

Vd = 0.9
Vd = 1.2
Vd = 1.5

X-axis: Gate Voltage, V
Y-axis: Drain Current, A

MITLL 0.18 µm Low Power FDSOI CMOS Device Models
(version 5.11.mp5, January 2002)

Legend: Vg=0, Vg=0.3, Vg=0.6, Vg=0.9, Vg=1.2, Vg=1.5

soifet3 w3 r4c2 nmos standard 8/0.5 Vbg = 0

Drain Current, A (y-axis) vs Drain Voltage, V (x-axis)

Vg = 1.5

1.2

0.9

0.6

0.3

Kink
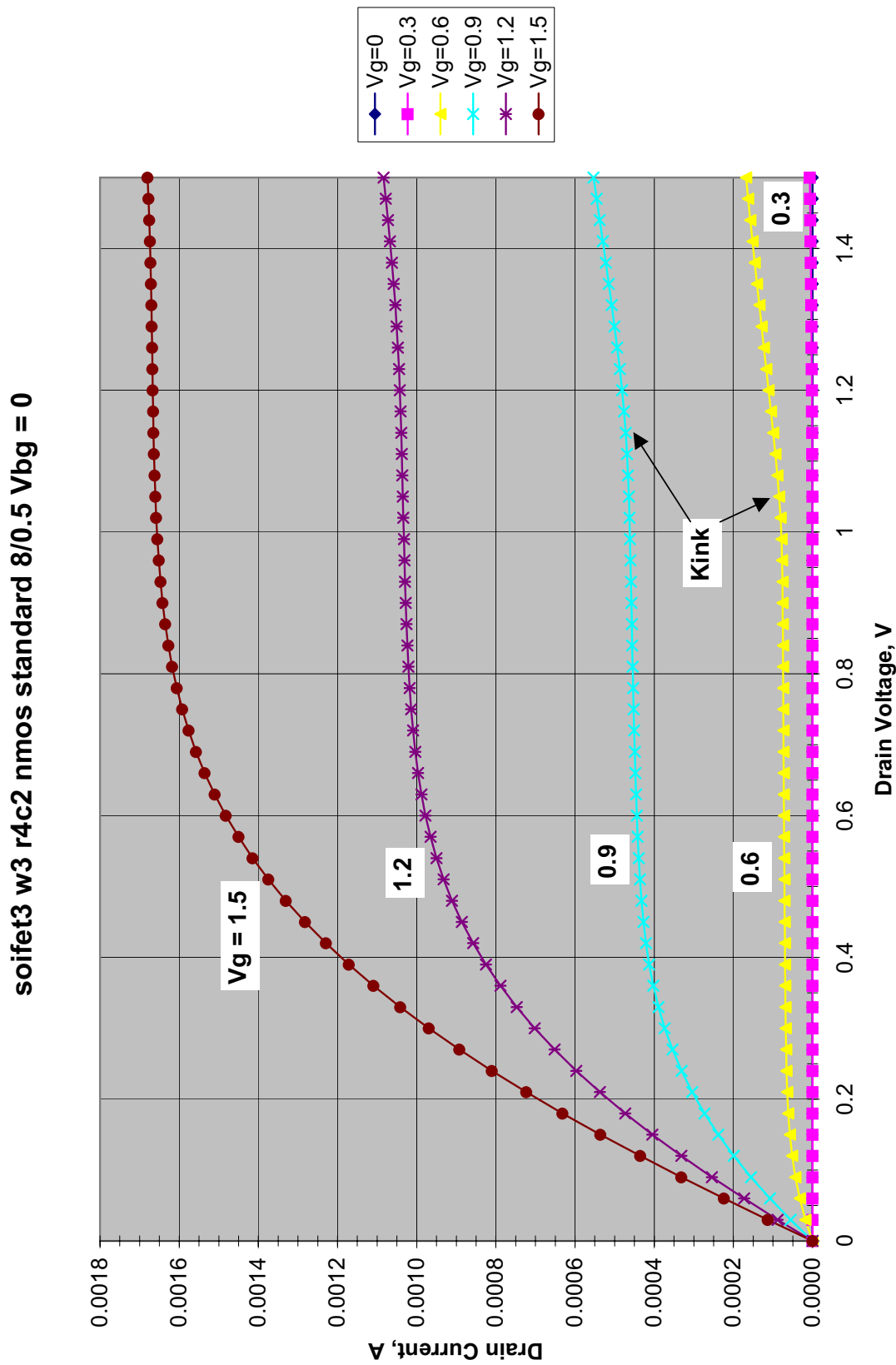
MITLL 0.18 µm Low Power FDSOI CMOS Device Models
(version 5.11.mp5, January 2002)

soifet w1 r3c4 pmos standard 8/0.2 Vd = -1.5V & 50mV
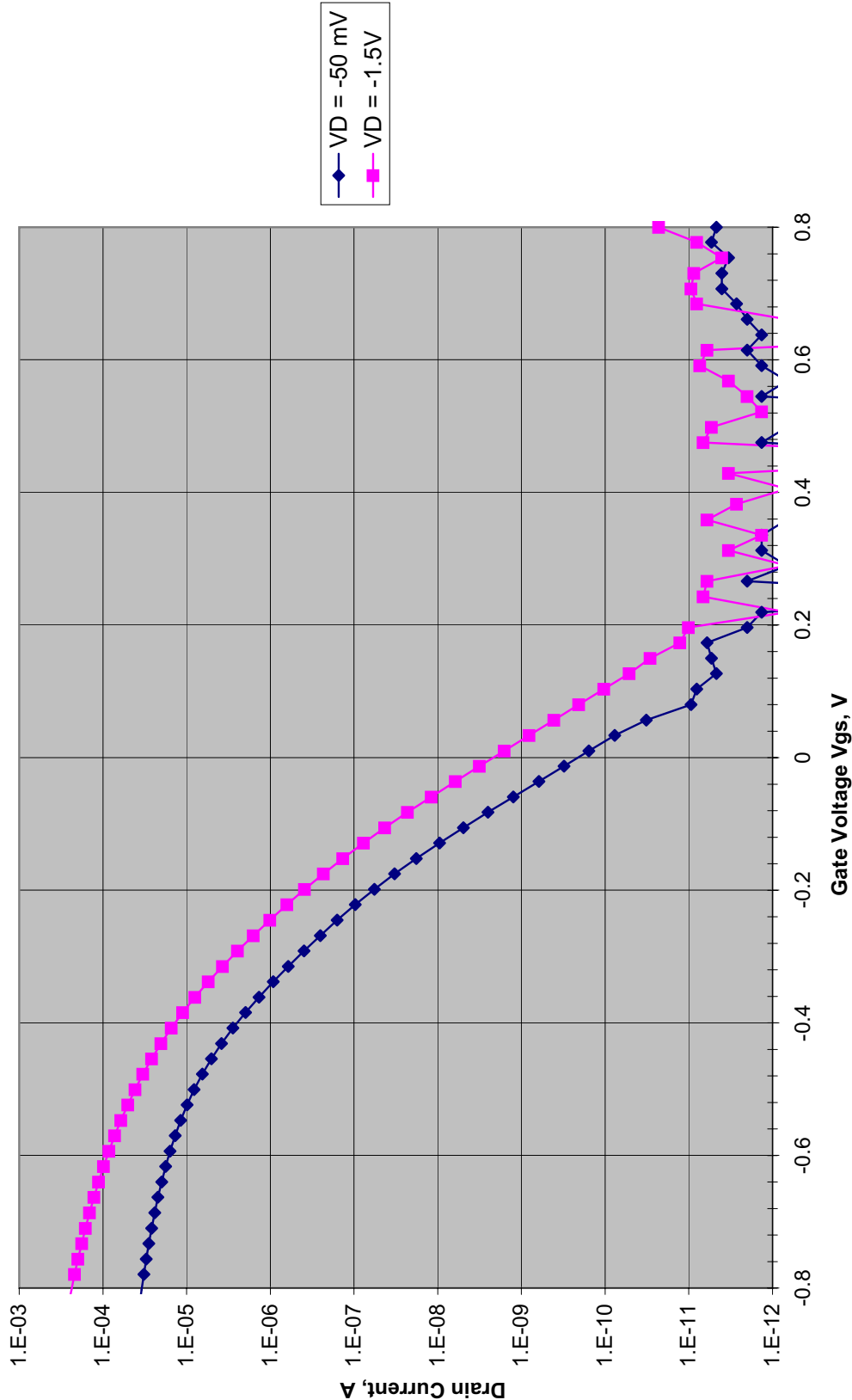
Legend:
- VD = -50 mV
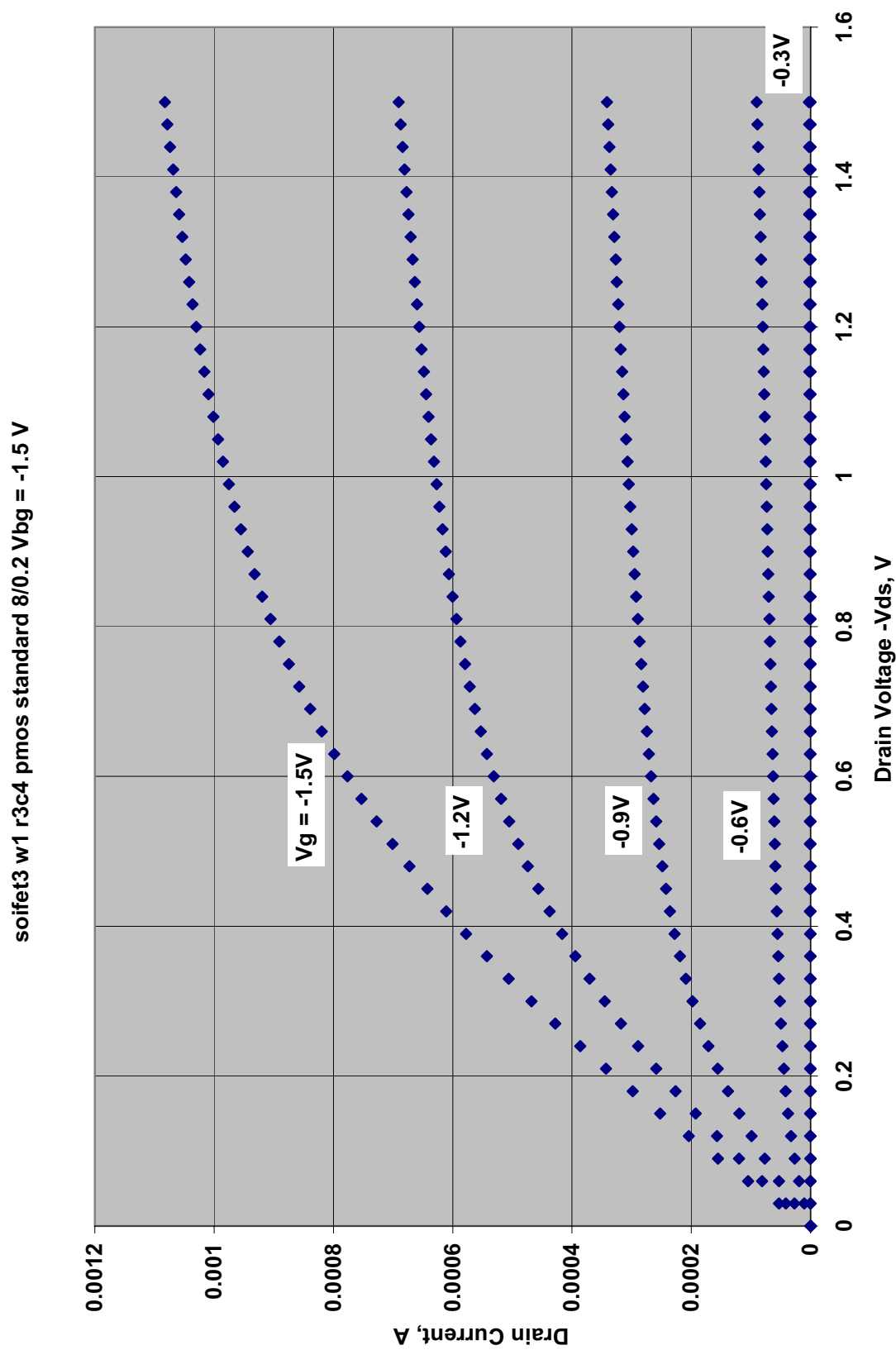- VD = -1.5V

X-axis: Gate Voltage Vgs, V
Y-axis: Drain Current, A

MITLL 0.18 μm Low Power FDSOI CMOS Device Models
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soifet3 w1 r3c4 pmos standard 8/0.2 Vbg = -1.5 V

Vg = -1.5V

-1.2V

-0.9V

-0.6V

-0.3V

Drain Voltage -Vds, V

Drain Current, A

MITLL 0.18 µm Low Power FDSOI CMOS Device Models
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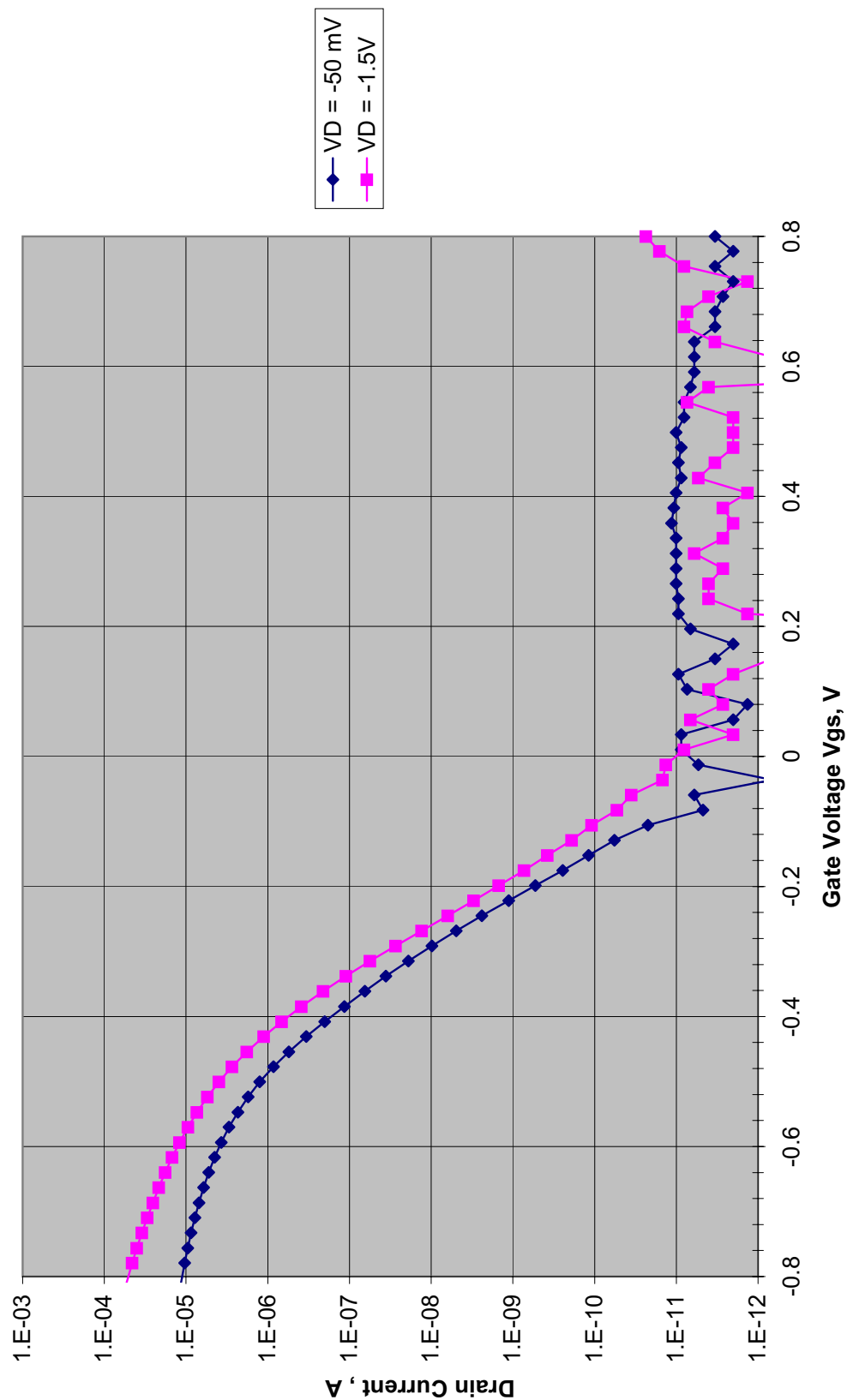
soifet3 w1 r3c4 pmos standard 8/0.5 Vd = -1.5V & 50mV

Legend:
- VD = -50 mV
- VD = -1.5V

X-axis: **Gate Voltage Vgs, V** (from -0.8 to 0.8)

Y-axis: **Drain Current , A** (from 1.E-03 to 1.E-12)

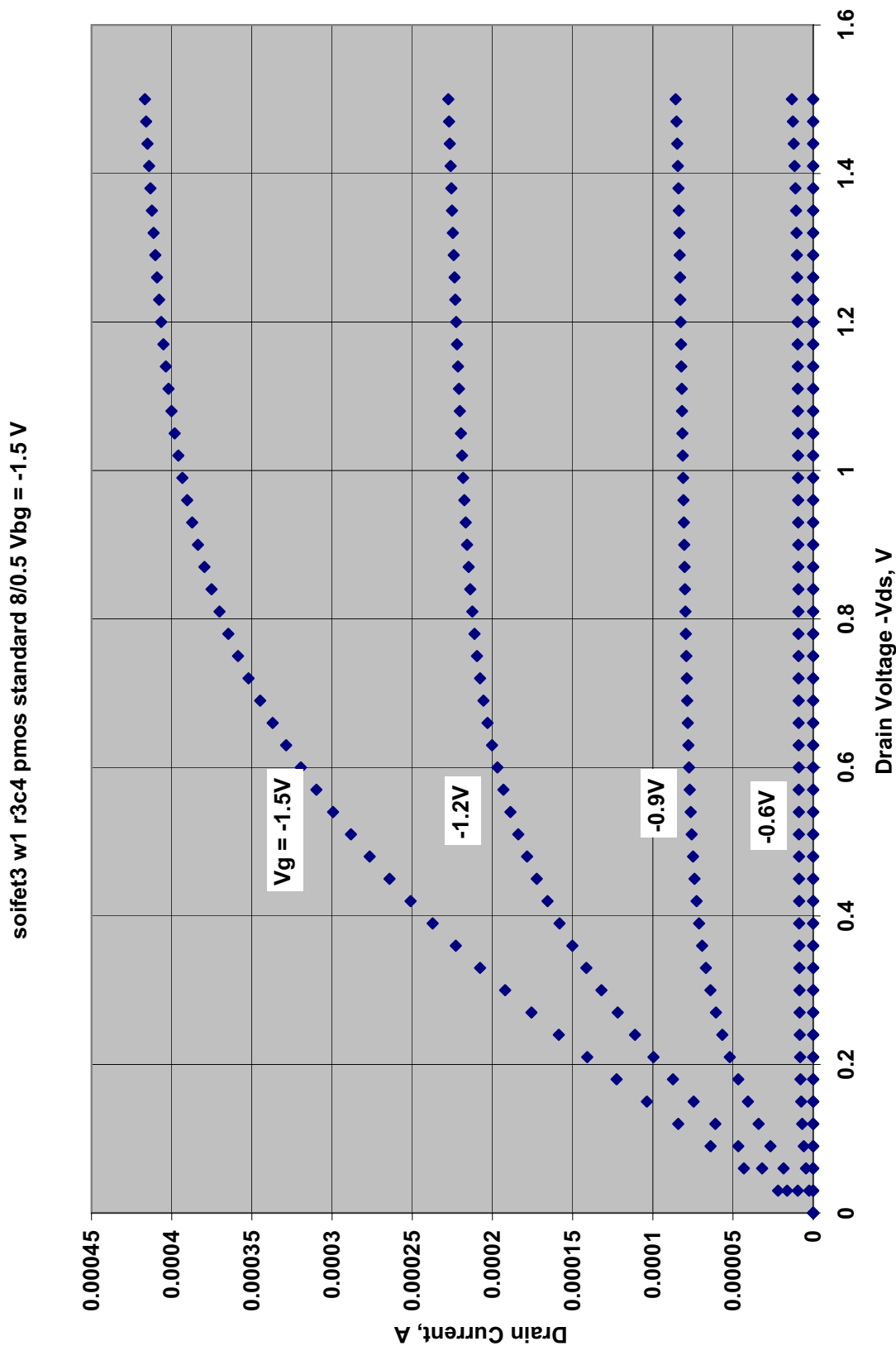# MITLL 0.18 μm Low Power FDSOI CMOS Device Models
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soifet3 w1 r3c4 pmos standard 8/0.5 Vbg = -1.5 V

Drain Current, A

Drain Voltage -Vds, V

Vg = -1.5V

-1.2V

-0.9V

-0.6V

MITLL 0.18 µm Low Power FDSOI CMOS Design Guide
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