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mstnews 2/05 on "Smart Textiles" in April 2005

Overview about microtechnologies for smart textiles and applications of smart textiles.

Deadline for press releases, short news, event announcements and advertisement orders: Mar 07, 2005

Date of distribution: April 01, 2005

mst|news

Dear Readers,

The term "microsystem" addresses two aspects: "micro" and "system". A system may be implemented without micro components or micro technology at all, but a single micro component that is not embedded in a technical system environment, or a single micro technology not in line with the whole process chain of a product production process, in most cases doesn't make much sense. The microsystems industry knows that "system" in reality means an approach considering the whole spectrum of relevant micro materials, machines and processes for manufacturing, handling, assembling, connecting and packaging as well as the complex network of interdependencies between all these items. As the complexity of the system solution increases, this network become more complex too, as in the case of hybrid concepts. "System" also means the task of finding a solution or a concept that combines and integrates a selection of the above-mentioned items in an optimal way and with the highest possible synergy effects to fulfil the final goal in the easiest and most cost-efficient way: To provide a new, innovative and - if possible - cheap product with higher functionality and performance than those offered by competitors.
This challenge is easily described with some sentences as above, but more or less difficult to master in industrial reality. Its high complexity and the lack of engineering experiences, tools and technical preconditions, such as the maturity of the micro technologies, production processes and equipment, is a serious barrier to the (in particular small and medium) enterprises for managing the system integration problems and making full use of microsystems technologies.
One technical field that is mandatory for successful system integration is the system design at the initial stage. mstnews will dedicate its June issue to the topic of "Design for Manufacturing", while manufacturing includes in our view more than mere machining processes. It also includes handling, assembly, testing, packaging and other production steps and their reliability!
Assembling and packaging technologies constitute another field that is essential for the success of system integration. Meanwhile this February issue of mstnews will give you an overview of different interesting developments and current trends in this field. We hope it will be fruitful and stimulating to you on your way to new microsystems solutions!

Bernhard Wybranski, chief editor

3D stacking module in front of some "elder stuff" from the history of assembly and packaging technology. The module represents a certain stage of development of self-organizing Microsystems with sensors, antenna, signal processing unit and energy supply (below the module), as implemented already at Fraunhofer IZM, Berlin

Main Topics of mstnews until 6/05

Issue	*Main Topics*	*Deadline for abstracts*
Apr. 05	Smart Textiles	passed
Jun. 05	Design for Manufacturing	Feb. 15, 2005
Aug. 05	Energy Self-supplying Microsystems	April 15, 2005
Oct. 05	Technology Prgrammes and Initiatives	June 15, 2005
Dec. 05	Ambient Assited Living	Aug. 15, 2005

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Managing Editor / mstnews Office:
Bernhard Wybranski, VDI/VDE-IT
Rheinstraße 10 B, 14513 Teltow, Germany
Phone: +49 3328 435-167
Fax: +49 3328 435-105
E-mail: mstnews@vdivde-it.de

Editors:
Alfons Botthof
Patric Salomon
Dr. Matthias Werner
Wiebke Ehret
(German MST Programme News)
Lutz John
(Assembly and Packaging)

Assistant Editors:
Annette Wittmann, Uwe Klädtke

Cover design:
Isabelle Brämer

Setting:
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Advanced Packaging - an important Cost and Success Factor for the Production of Microsystems

Lutz-Günter John

Our modern communication society cannot exist without a great many invisible electronic assistants. However, we are still in the initial phase of this development. In the near future new generations of microsystems with new integrated sensors, actuators and communication features concentrated in one functional device will be implemented. First examples are the new mobile phones with photo and camera and also PDA function. With sufficient display resolution and image definition the new generation of personal assistants can also connect video, movie and internet functions. Also GPS-based navigation systems with map source and many other on-demand functions will be possible. These microsystems will not only be linked with wireless local and global networks, but also with each other without the need for a computer or data communication centre. These developments will be based on a new generation of microsystems with embedded complex sensor, actuator and communication functions. The realization of these microsystems will not be feasible without technical advance in the miniaturization of integrated circuits.

Packaging technology plays an important part in the realization of microsystems. With the development and design of an electronic layout of a microsystem a solution must be found for its functional behaviour and also for optimal packaging, possible production cost and potential reliability.

Nowadays new ideas for products realized with highly integrated microsystems have an edge over discretely realized solutions in terms of production costs. Innovative integration technologies were used predominantly in products characterized by small size and high functionality as well as large volumes to justify high cost.

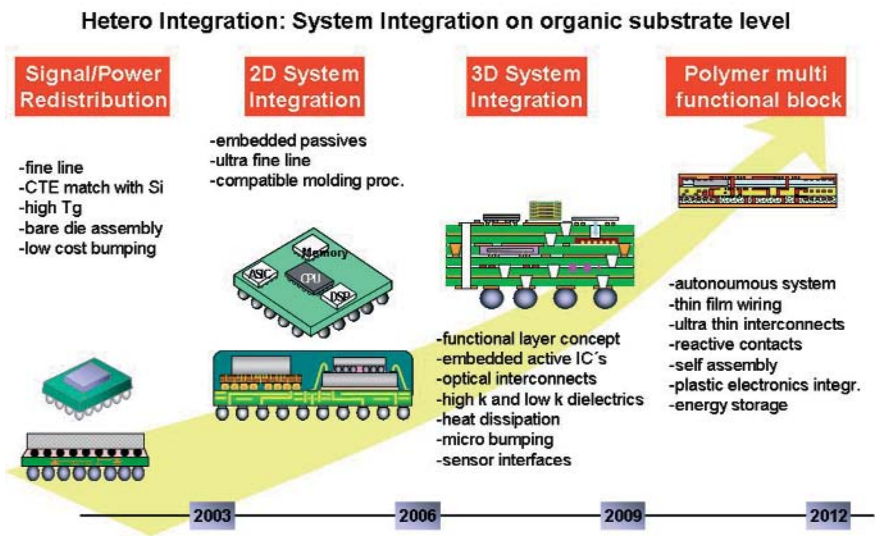

Figure 1: Hetero Integration roadmap on organic substrate level; (source: FhG-IZM, Berlin)

With the increasing use of bare dice likey flip chips and CSP and also of highly integrated circuits and ASICs with a high number of interconnections mature technologies and materials have become necessary to live up to this trend. This makes it also possible to realize components, sensors, actuators and microsystems with a high yield and lower cost. Therefore production cost is not so high any more in comparison with a discrete solution.

The approach to use silicon technology for complex monolithic integration has been realized only in a few cases of component setup, for instance pressure sensors, micro pumps and coupler structures for optical waveguides. In view of a technology base that differs too much, it is hard to combine different IC technologies on a single silicon wafer.

In contrast to the monolithic integration path, the emphasis has been placed on technologies with a hetero system integration aspect. Hetero integration seems the right way for

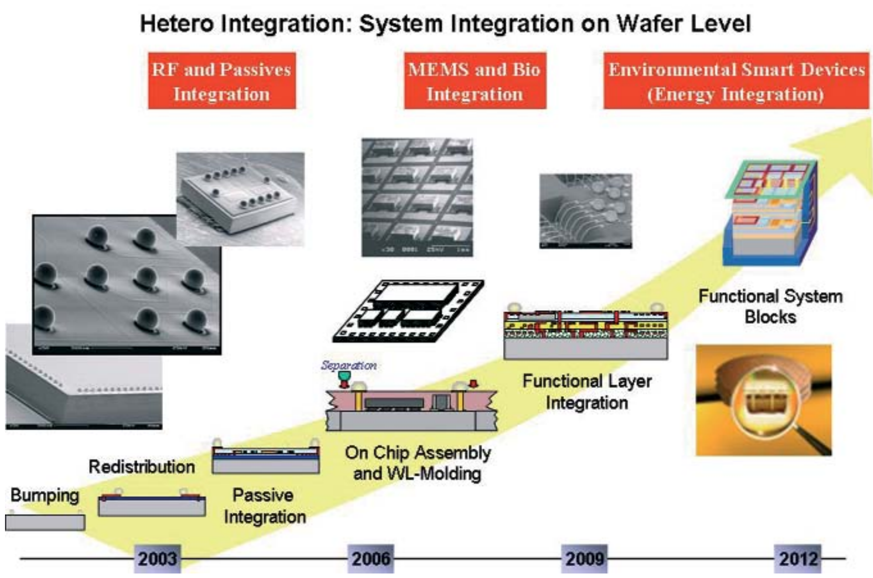

Figure 2: Hetero Integration roadmap on wafer level ; (source: FhG-IZM, Berlin)

Figure 3: 3D stacking technology for self-organizing microsystems; (source: FhG-IZM, Berlin)

good performance, lower cost and high reliability for the production of microsystems in any case. Therefore a great variety of packaging technologies was developed in close interconnection with new materials. Beside the IC-driven concepts of system integration like System on Chip (SoC), concepts such as System in Package (SiP) and System on Package (SoP) have lately won increasing acceptance. In these technologies more than one integrated circuit may be combined on one layer with passive components and also with several sensors and actuators. The advantages of these conceptions for microsystems are multifunctionality, high miniaturization and lower cost. In addition to these conceptions for system integration, well-known technologies have also become of more practical importance for the production of microsystems. For instance flexible organic substrates allow the realization of very compact and functional microsystems with the focus of a freely designed ergonomic and functional body. Otherwise their behaviour is good in terms of temperature and shock stress. 3D-MID technologies are increasingly being used because they show good system performance in their volume aspect.

From the existing technology trends in the field of packaging conceptions the following mainstreams for the development and production of microsystems may be deduced.

- 2D- and 3D- integration
  - Technologies for embedded passive and active components (e.g. chip in polymer)
  - Integration of MEMS, antennas, RF filters, switches and resonators
  - Research and usage of functional layers
  - Realization of optical interconnects in normal FR4 substrates or any other organic material and the realization of optical chip-to-chip connections
  - Technologies for chip-on-wafer packaging
  - Via technologies for 3D-integration
  - Research and use of nano- and biostructures
  - Design tools for 2D- und 3D-integration
- Housing technologies for the integration of electronic, mechanical, optical, fluidic and other components
- Developments of packaging technologies for microsystems for harsh environments
  - Packaging for high-temperature applications (> 125°C) und

Figure 4 System in Package for consumer applications

high-power solutions
- Packaging for bio-compatible materials for applications in the human body
- Use of alternative materials like paper and textiles
- Development and use of polymer materials for new conceptions of chipper microsystems

- Development of "green" packaging methods likely the use of lead-free solder and also the use of recyclable materials and techniques
- Development and use of new nano materials and nano techniques and components
- Support of new technologies with high productivity and low preparation costs, e. g. reel-to-reel conception
- Micro-Nano Integration
  - Packaging for interconnection from the nano world to the normal macro world via microsystems
  - Development of devices and components for the packaging of nano/microsystems (e.g. connectors, sensors, actuators, energy sources)
- Research and development of new technologies like self-assembly or addressing and transport of nano components
- Development of micro energy sources for the realization of autonomous energy microsystems

Figure 1 shows the roadmap of hetero integration based on organic substrates and Figure 2 another silicon wafer based variant.
Both development trends lead to the same vision: highly integrated 3D components with integrated sensors, actuators and power supply.

Apart from the work on the packaging and interconnection technology of these 3D packages, an equally intensive effort is being made to set up an autonomously organized communication network with so-called e-grains that are being developed at the Fraunhofer Institute of Reliability and Microintegration in Berlin (FhG-IZM). Figure 3 gives an idea of the size of 3D stacking modules compared with a one-cent piece.

In future packaging conceptions for system integration cannot be developed in isolation. The microsystems as part of our living world will become more and more important. Consumers through their acceptance and buying behaviour decide on the success of the level of integration at microsystems. Therefore the human-device interface has also become of great importance.

Contact:
Lutz-Günter John
VDI/VDE-IT, Germany
E-Mail: john@vdivde-it.de

System Integration in Microsystem Technology - Viewpoints of the German ZVEI on the Subject of Multifunctional Packages

Interview with Dr. Michael Burmeister, Managing Director Harting Mitronics AG

Question: Dr. Burmeister, in the last few months the Microsystems Technology Group of the German Association of Electronic Components and Systems (ZVEI) has been conducting an in-depth debate on the subject of packaging and interconnection technology for microsensors and microsystems. What do you think are the current trends in packaging and interconnection technologies of microsensors?
Answer: Two trends can be observed in this area. On the one hand, increasing use is being made of standard packages of the semiconductor industry in applications with large-scale manufacture as, for example, in automobile sensorics or in the consumer sector, while others, above all new markets for microsystems technology, require customized solutions with reduced numbers of pieces. That means that the number of variants in the field of sensorics is rising while piece numbers per variant are decreasing. Annual piece numbers of 100 million and more, as is customary for standard components, are limited to few applications for sensorics products. Therefore, the package has to be adapted to the prevailing marginal conditions for different applications of one and the same sensor chip. The manufacture of packages that have far higher piece numbers per product in the standard range is thus pushed into the sector of customized solution. In order to translate concepts into practice, wafer manufacturers have to rely on external engineering and production support. The consequence is the market entry of application-specific and multi-variant package solutions.

Q: Low volume production often entail high costs. May new mounting and connecting technologies also help to produce marketable products in case of lower piece numbers, too, and which important applications do you think multifunctional packages may have?
A: With standardization pressure decreasing, packages are more and more assuming specialized functions that the outer housing originally had, e.g. contacting with a network, screening from external influence or access to media like liquids, gases, etc. The package thus enables customer-specific formation of variants that was originally achieved with ASICs. The standardized chip is employed in various applications with different and multifunctional packages. 3D multifunctional packages also offer more optimization potential inthe system context. As an example, the combination of the housing function with the package can make sensors smaller and lighter. The number of connection interfaces will decrease and the achievable reliability thereby increase.

This, again, are a good approaches for marketable products.
Multifunctional packages are primarily suited to meet application-specific requirements. Automobile sensorics, industrial sensorics and medical applications in the field of diagnostics are the most important application fields. All three fields stand out for considerable growth dynamics, with medical applications developing the highest dynamics in view of a multitude of new functions. Apart from these "traditional" sectors, the setup of sensorics networks is seen as another important application field for multifunctional packages. From our viewpoint sensor networks will penetrate into all walks of life in future. In this way it will be possible for example to monitor bridges, buildings or forest areas by registering and transferring data such as temperature, humidity, vibrations or chemical processes.
However, these applications can only be developed if miniaturization is accompanied by marketable cost. It is therefore necessary to press ahead with the integration of heterogeneous components (e.g. sensors, antennas, processors, etc.) on the wafer level. This will give rise to System-in-Package (SiP) solutions in conjunction with innovative housing technologies like the MID technology. The current growth rates of SiP and MID technologies of over 40% show that this way holds out great promise.

Q: Dr. Burmeister, let me come back to this point again. Realizing microsystems requires coming to grips with a great variety of technologies. Would SMEs be able to benefit from these new developments at all?
A: Of course they would. Microsystems technology is an area where Germany is one of the world leaders, not least on account of the commitment of its SMEs. Nonetheless, the availability of the technology on the level of SMEs may and must be improved. This is especially true because this point is a key element in increasing value added, thereby strengthening leadership in this area in Germany and Europe.
On a technical level the networking of results achieved constitutes a major potential for opening up new fields of competence for SMEs. The subject of "multifunctional packages" may particularly profit from pooling and developing existing technologies.
Here a new field has come into being which stands out for a great multiplicity of potential applications. This holds many opportunities, especially for SMEs, but at the same time makes great demands on the availability of new materials as well as packaging technologies.
As an example, enhancing standardized solutions for specific applications is a pivotal element for market development. The results will be twofold: On the one hand, a technology proof will be able to overcome barriers to entry and, on the other hand, technologies may also become applicable for SMEs that are unable to pre-finance a technology proof of their own on cost grounds.

Q: You have just mentioned the financing aspect. May companies make this effort on their own or do you think the government should also make a contribution?
A: We believe that assistance from the government will have a special role to

play. We should not forget that within the framework of R&D projects supported by the government knowledge and technological know-how has been and is still being acquired on a grand scale that is still awaiting practical application. The impact will be broad-based if assistance is especially provided to SMEs in their development and application of multifunctional packages. If they succeed in demonstrating successful applications, inhibitions on the side of users will be reduced.

It is important not to confine ourselves to solely putting up demonstrators. Only qualified samples may be considered as proof of a technology. Application-wise, the point is to focus on high-sales applications with a clearly recognizable interest for practical application on the part of the partners involved. It is only consistent that those who possess knowledge must be asked and obliged to convert this into value added. The financial incentive to market technologies on a broad scale must be made a fiscal instrument of the policy of granting financial assistance. This is the only way to achieve the original objective: translating innovations into jobs.

Q: One last question: Has ZVEI already worked out concrete proposal for R&D priorities?

A: The debate has certainly not ended yet, but is possible to point out some priorities already now which are crucial for the development of multifunctional packages:

- Processing and integration technologies on the wafer level as base technologies for future integrated sensor systems (e.g. Inter Chip Via Technology or sputtering technologies...);
- Packaging materials made of thermoplastics like LCP and PA, etc.;
- Micro 3D circuit carriers that may be produced by laser techniques, injection moulding and premould technology;
- Packaging and interconnection technologies on 3D substrates such as Wafer Bonding, Thin Chip Integration, Flip Chip, adhesive bonding technologies and plastic bumps;
- Packaging concepts with media access, viz. mechanical connection of chip to exterior world (nozzles, channels, lenses, filters, etc.);
- Combinations based on connector and strip conductor technologies;
- Antenna technologies in 3D housings;
- Packaging technologies for high-temperature applications;
- Combinations based on mechanical mounting technologies with the assembling of electronics components;
- Testing equipment for the production of new components.

Given the complexity of Multifunctional Packages and the interaction between individual components and technologies, it seems to be sensible to base developments on applications and to link government assistance with model process flows. This will avoid isolated and self-detached solutions that have no relevance for the market and to place the emphasis on the exemplary interaction of individual technologies in the product and process flow.

Thank you very much for this interesting talk, Dr. Burmeister. We wish you every success in your work in the ZVEI and in your company as well.

The interviewer was Dr. Randolf Schließer, VDI/VDE-IT
schliesser@vdivde-it.de

Recent Advances in System Integration and MEMS Packaging

Koen Snoeckx, Kris Baert, Chris Van Hoof and Eric Beyne

Interesting times lie ahead in the domain of 3D packaged applications. Continuous scaling and the rise of new technologies, such as MEMS, create a range of opportunities for applications that seemed hardly imaginable only a decade ago. For example the medical industry finds great interest in highly miniaturized sensors. But also the digital imaging industry makes the most of the latest developments in the microsystems technology domain. What follows is an overview of some important research issues and breakthrough technologies that bring these promising applications closer to reality.

The severe pressure on scaling of electronic devices has literally lifted the industry to a higher dimension. Stacking of dies and components in

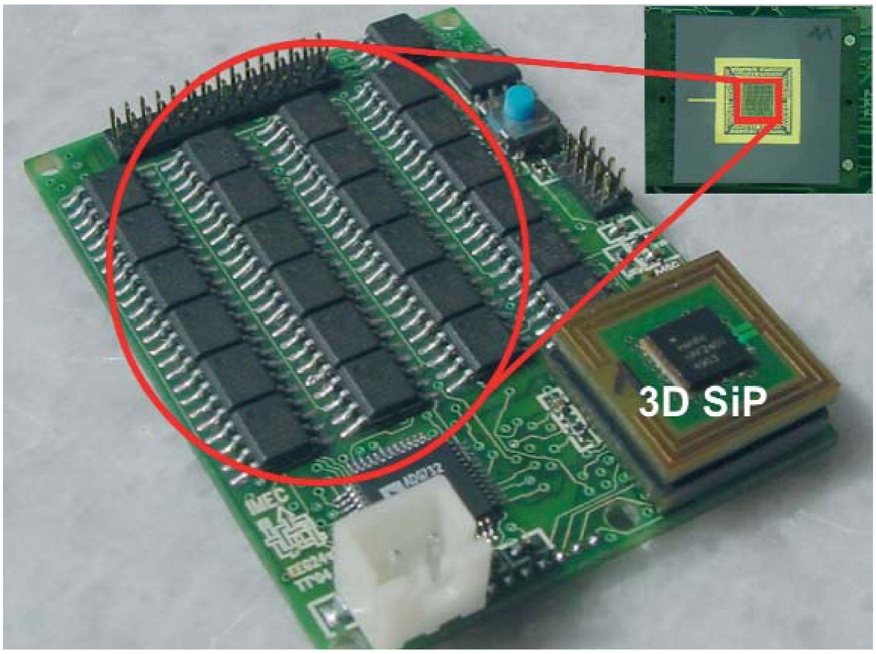

Figure 1: Integrated 3D SiP sensor platform (bottom right of the board) in an EEG/ECG module. Indicated analog electronics are now processed as a single chip (inset)]

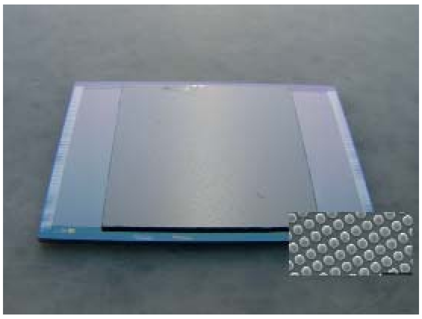

Figure 2: Solder bumped 1Mpixel CMOS image sensor with high-density parallel integration scheme with 10µm bump pitches (inset)]

the Z-axis appears on the menu of any research facility involved in this domain. Also IMEC, the Belgian research center on nano-electronics and nanotechnology, has conducted a decent amount of work on 3D systems-in-a-package (SiP) in recent years.

3D stacks

IMEC's approach consists in dividing the 3D stack into individual subsystems, such as e.g. antenna, RF front-end, radio baseband, main application hardware, MEMS sensors, power management and power generation. The subsystems can be stacked on top of each other, realizing a dense 3D-SiP. The advantage is that each subsystem can be fully tested before final assembly, avoiding the known good die problem. Several devices that illustrate this approach have already been reported: a 5GHz wireless LAN transceiver including antenna on the package, a complete Bluetooth radio (baseband and RF) measuring only 7 by 7mm and an extreme low power autonomous 2.4GHz 1cm³ SiP sensor platform (including antenna) [1].

The last example plays a central part in IMEC's development of a fully autonomous wireless intelligent sensor. Within the Human++ program, a complete body area network is being developed for patient monitoring. The outcome of the program, expected around 2010, will give an answer to the demands of the medical and wellness industry for portable and discrete monitoring systems. One of the technology drivers behind Human++ is an integrated 24 channel EEG and 1 channel ECG unit for use on the human body. The current status is a 1cm³ SiP containing the DSP and communication components, mounted on a board with the necessary analog electronics for signal processing. The latter account for more than 80% of the current surface and make the entire device size more or less a package of cigarettes. [Figure1] This becomes a different story when stated that the referred 80% are now integrated into a single chip that's smaller than a fingernail.

Die stacking

But there's still a long way to go and some important obstacles to take. Current 3D stacks have typical dimensions around one or a few cm³ and are built with standard components available on the market. For further development of miniaturized devices, interconnection technologies that enable the stacking of layers of chips and integration of MEMS are key.

Massive parallel hybrid integration schemes, using through wafer vias and solder bumps, can allow high-

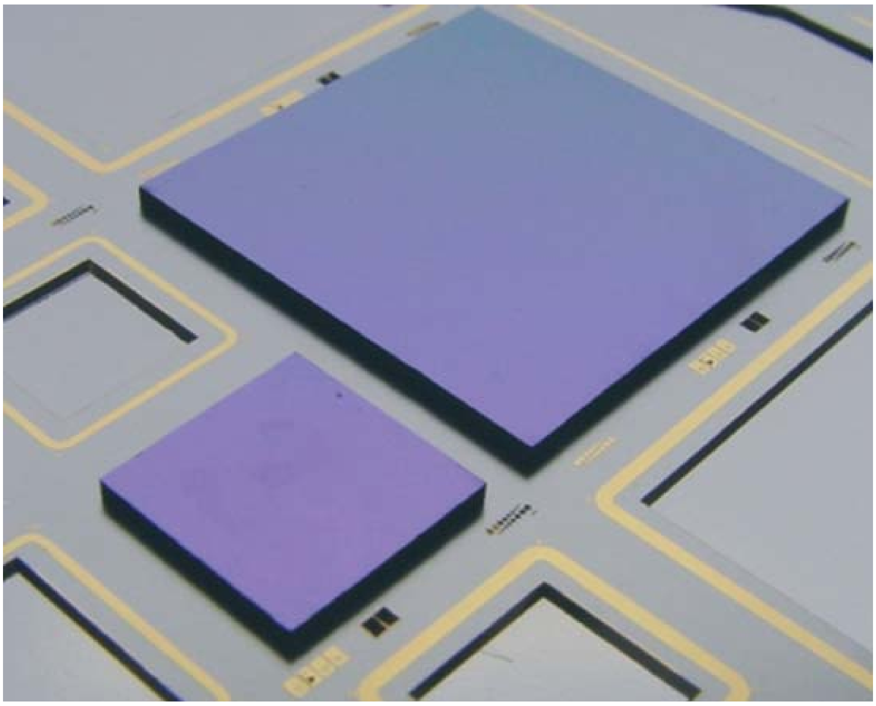

Figure 3: Illustration of hermetic metal sealing through the indent reflow sealing approach.

yield assembly. Solder bumps are already used to interconnect megapixel imager sensors to ASIC read-out circuitry [Figure2]. These, as well as image devices for printers or displays, require local interconnect between each imaging pixel and its read-out circuitry, creating the need for high density 2-dimensional integration. IMEC demonstrated arrays with a pitch as small as 10 µm.
Bumps can easily be realized by electroplating or evaporation on the top and/or bottom substrate. Plan-parallelism is a key issue to achieve connection yields up to 99,5%.
To achieve additional miniaturization at system level, innovative methods for thinning, handling and deposition of dies in thin-film platforms have been developed. Its possible to thin dies down to 10µm without causing damage to their functionality. The thin dies can be embedded in a thin-film process and further interconnection can be performed on wafer level, avoiding connections via flip-chip or wire bonding.
Even smaller devices can be achieved when the MEMS component is processed directly on top of its ASIC. By using polySiGe as the MEMS structural material, this can perfectly be realized. One example, developed at IMEC, is a poly-SiGe gyroscope processed on top of standard 5-level-metal CMOS, to be presented in February at the ISSCC conference in San Francisco. Furthermore, the poly-SiGe material is also suited for use as a thin-film cap.

MEMS packaging

MEMS components are indispensable in autonomous 3D sensor nodes. Since MEMS are highly susceptible to post-processing damage and are therefore not compatible with many conventional packaging processes, a typical MEMS packaging sequence starts at zero level. Simple wafer-to-wafer or die-to-wafer assembly techniques using BCB seals prove to be a valuable and reliable option in a variety of situations, requiring only fairly straightforward techniques. Polymer sealing has proven to be topography tolerant, easy to pattern, feasible at low temperatures - while in the meantime compatible with higher ones - and more than sufficiently resistant to thermal and mechanical stress. One limitation is that using polymers results in "semi-hermetic" seals. These guarantee a humidity barrier and effective protection against aggressive assembly operations, and may even provide a humidity barrier during the device lifetime of MEMS switches [2].
When full hermeticity (e.g. for vacuum packaging) is required, Sn- or In-based seals [Figure 3] are the best choice, even if demanding a more complex process sequence that will include for example pre-solder metallizations on the MEMS. But the result outweighs the complications. Using indent reflow sealingit is possible tocontrol the ambient in a zero-level package in terms of internal pressure and filling gas. But on long-term and for specific applications, outgassing remains a tricky barrier to overcome and the incorporation of getter material can be required. With these techniques, caps with a thickness down to 50µm can be mounted. In order to also minimize lateral dimensions, thin-film based capping techniques can be used, but only at the expense of further process complexity and more device-specific process sequences [3].

Conclusion

Fully autonomous monitoring systems with the size of 1cm³ are very close to reality. Once advanced technologies such as wafer thinning and MEMS processing and packaging are optimized, further miniaturized devices will increasingly be demonstrated. And in a not too distant future, fascinating applications to improve our quality of life will undoubtedly appear on the market.

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Contact:

Koen Snoeckx is scientific editor at IMEC.
Kris Baert is vice-director of the integrated systems department at IMEC.
Chris Van Hoof is head of the integrated systems department at IMEC.
Eric Beyne is program director packaging at IMEC.

Field Configurable Assembly: Programmable Heterogeneous Integration at the Mesoscale

Alan O'Riordan and Gareth Redmond

Field Configurable Assembly is a novel programmable force field based heterogeneous integration technology. In this review, we demonstrate application of the method to rapid assembly of sub-100 micron GaAs-based light emitting diodes at silicon chip substrates. We also show that the method is compatible with post-process collective wiring techniques for fully planar hybrid integration of active devices.

Introduction

Mesoscale systems, i.e., systems that exploit mesoscale objects as highly functional device elements, are becoming more prevalent in the fields of electronics, optoelectronics, sensors, MEMS and MOEMS, and are typically fabricated using integration methods that involve microrobotic picking of individual devices followed by placement at selected regions at a chip surface. However, accurate placement of discrete devices is becoming difficult as device size continues to shrink, since adhesive forces (electrostatic, Van der Waals and capillary) between device and microtweezers begin to dominate relative to gravitational forces required for device release.

Therefore, a critical challenge, in the fabrication of future hybrid integrated systems that exploit mesoscale objects as active device elements, is the lack of availability of integration tools that enable successful manipulation and assembly of these devices into sparse or dense arrays at a chip surface. To address this challenge, we have recently reported development of a novel "hands-free" integration method, Field Configurable Assembly (FCA). In this method, electric fields, configured by selective addressing of receptor and counter electrode sites pre-patterned onto a silicon chip substrate, drive the electrophoretic transport, positioning and localisation, i.e., self-assembly, of mesoscale objects at each of the selected receptor electrode locations; see Figure 1.

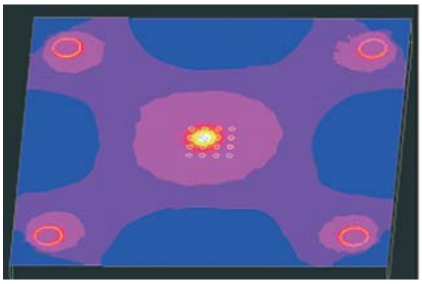

Figure 1: E-field simulation showing electric fields around a biased receptor electrode.

Device Assembly Using Electric Fields
To demonstrate the applicability and versatility of this novel method, we have applied FCA to serial and parallel self-assembly of a broad range of mesoscale components including 1 micron diameter latex beads, 50 micron diameter and 80 micron diameter 670 nm emitting GaAs based light emitting diodes (LEDs), at silicon chip assembly substrates [1].

As a platform for demonstration of FCA, simple silicon chip substrates typically comprise 4 x 4 arrays of receptor electrodes (100 micron diameter 250 micron pitch) implemented in disc-and-torus formats with circular counter electrodes (500 micron diameter) located at the four corners of each array. Conducting interconnection tracks are employed to contact each electrode to a unique contact pad located on the periphery of the chip substrate. To prevent electric fields associated with the interconnection tracks adversely interfering with site selective assembly, silicon chip substrates are overlaid with a conductive metal shield layer sandwiched between two bisbenzocyclobutene (BCB) polymer layers. To facilitate electrical addressing of the electrodes, vias are opened in all three layers above each of the receptor and counter electrodes and contact pads by optical lithography and etching; see Figure 2.

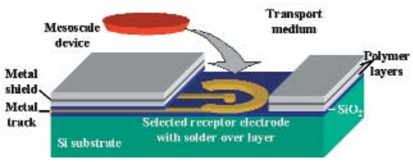

Figure 2: Schematic of device assembly at a silicon chip substrate.

In this electric field assisted assembly method, voltage biases must be applied to selected receptor and counter electrodes. To this end, the FCA electrical addressing system comprises a DC power supply connected to a multiplexer unit, which, via probe card connection to the contact pads on the assembly substrate (chip or wafer), enables programmable addressing of the entire receptor and counter electrode array under PC-based LabVIEW™ control. In this manner, the electric field distribution around any receptor electrode site(s) may be configured as desired.

Prior to assembly, mesoscale components, e.g., 80 micron diameter LEDs are first suspended in a suitable transport medium and then randomly dispensed on the surface of a silicon. To achieve FCA, application of a voltage bias to a selected receptor electrode (typically -20 V versus the counter electrodes, resulting in an electric field strength, E = 6.66 x 103 V/m) is sufficient to drive the electrophoretic transport and localisation of a LED device at the selected site; see Figure 3.

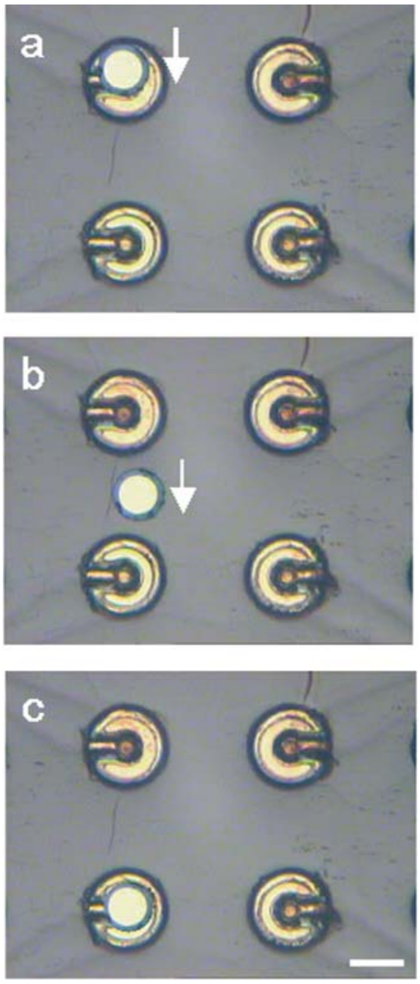

Figure 3: (a) - (c) Video image frames showing FCA of an 80 micron GaAs-based LED.

Following assembly, devices may be permanently bonded to respective receptor electrodes by reflow of Sn/Au solder layers overlaying the receptor electrodes. To complete packaging of the assembled devices, a top metal contact is deposited, following a planarisation step, to facilitate direct electrical addressing of each device. Typical I/V characteristics, measured for LEDs assembled and integrated in this manner demonstrate standard GaAs p-n junction behaviour with a voltage threshold of just over 1.7 V for light emission; see Figure 4.

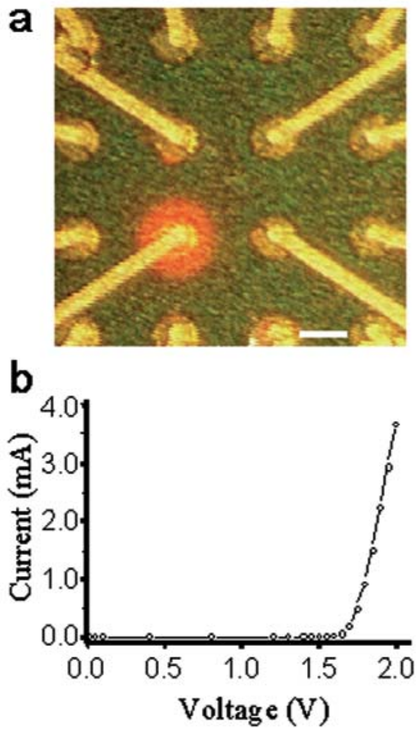

Figure 4: (a) Optical micrograph a fully packaged LED, (b) I/V characteristic.

Conclusion
In this review, we have shown "hands-free" assembly and integration of sub-100 micron GaAs-based light emitting diodes at silicon chip substrates using a new technique, Field Configurable Assembly. Although we have used LEDs as model functional mesoscale devices, the technique is applicable to either serial or parallel self-assembly of a wide range of device types at a broad variety of substrates. Future applications for this novel assembly technology could range from nanoelectronics through nanophotonics to nanoscale biotechnology.

References
[1] O'Riordan, A.; Delaney, P. & Redmond, G., Nano Lett. 4, 761 (2004).

Contact
Gareth Redmond
Tyndall National Institute, Lee Maltings, Prospect Row, Cork, Ireland.
Email gareth.redmond@tyndall.ie
www.tyndall.ie/nanotech

Contactless Handling of Micro Parts

M. Franzkowiak, S. Grünwald, M. Schilp, A. Zitzmann, J. Heinzl and M. F. Zaeh

Microsystems are assembled out of parts that have functional surfaces with fragile structures. These new characteristics pose a challenge to handling technologies for micro parts, as any mechanical contact can result in damage to a gripped part and, consequently, to the destruction of the whole microsystem. To reduce this yield loss any contact between micro parts and handling equipment should be eliminated. This requirement can be met by three innovative approaches to contactless handling presented in this article.

Air Cushion Gripper

The principle of an air cushion gripper (Figure 1) is based on a vacuum pre-stressed air bearing. The gripper includes several arrays of pressure and vacuum nozzles. Located on the bottom side, these create an air cush-

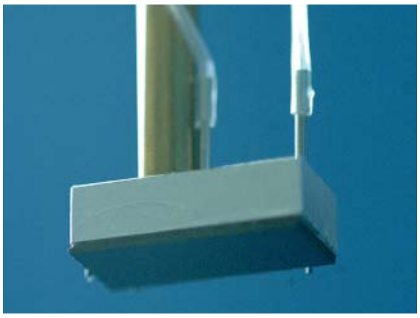

Figure 1: Air cushion gripper

ion, separating the gripper and the micro part, which is levitated underneath the gripper.

To grip a part the high and the low pressure must be adjustable. The weight of the part has to be in equilibrium with the pushing and pulling forces exerted by the air cushion. A stable equilibrium is reached at a gap of about 10 microns between the air cushion gripper and the part.

In addition lateral forces must be applied to the part to provide accurate centring and to allow high accelerations in a pick-and-place process. The required centring device can be implemented by simple mechanical stops that must be adjustable to the size of the part. A new contactless centring can be realised by using a fluid dynamic effect. As a precondition, air must be sucked into the gap between gripper and part. Additionally the gripper surface must be congruent to the part surface. Under these circum-stances a small region of low pressure is built up on the part's lateral surface. If the gripped part is in an off-centre position the difference between the low pressure and the ambient pressure on the opposing part sides generates a resulting force against the direction of displacement. This effect provides a stable lateral positioning of the gripped part.

Ultrasonic Levitation

Levitation effects within ultrasonic fields are based on a squeeze film or acoustic standing waves.
A new application of squeeze film levitation is the contactless handling of MEMS. The ultrasonic source is a Langevin Bolt Transducer (Figure 2), which has a constant work (resonance) frequency of 30 kHz.

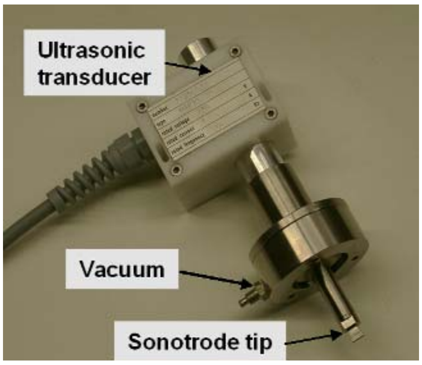

Figure 2: Squeeze film vacuum gripper

The sonotrode is hollow-bored and easily exchangeable. The oscillation amplitude at the sonotrode tip reaches values between 10 and 30 µm. Parts can be picked from above by the combination of ultrasonic and vacuum. The vacuum forces the parts to the gripper surface. The air cushion generated by the high frequency oscillation of the sonotrode produces a repulsive force on the part. Finally there is an equilibrium of these two forces and the weight of the handled part. The most important demand for the function of the contactless handler is a safe and reliable lateral centring of parts. Similar to the air cushion gripper, it is possible to centre the part below the gripper by fluid dynamic effects.
A further phenomenon that can be used for handling parts without contact, is the levitation based on the acoustic standing wave. The arrangement consists of a reflector and a vibrating sonotrode and is called a resonator. The distance between both elements is an integer multiple of half the wavelength. The front ends can be planar or concave. In the resonator, small parts are levitated in the pressure nodes of the standing wave.

To stabilise and manipulate a part in the sound field the effect shown in Figure 3 can be used. The red colour indicates the increase of sound velocity at the edges of an object placed in the sound field. This increase leads to a pressure reduction. Using additional surfaces this phenomenon is used in present investigations to improve the positioning and orientation accuracy of parts in the sound field.

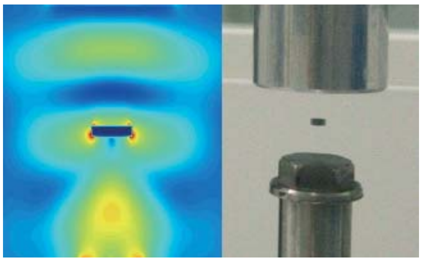
Figure 3: Sound velocity around a part in a standing wave (left) and arrangement of sonotrode, reflector, and levitated part (right)

Summary and Outlook

The contactless grippers presented here show several advantages compared to conventional tactile grippers. A homogeneously distributed force enables sensitive gripping of fragile parts. Thus parts can be gripped at their functional surfaces, eliminating the need to design extra gripping areas increasing the part size. Additionally, non-contact centring principles do not exceed the part size, as no mechanical boundaries are needed. In consequence the distance between mounted parts can be minimised. Disadvantages are the low flexibility to different part shapes and the need of additional equipment, like ultrasonic sources and pressure supply. This work is part of the research cooperation "Mikroproduktionstechnik - ForMikroProd" and sponsored by the Bayerische Forschungsstiftung.

Contact:
Michael Franzkowiak
Institute for Machine Tools and Industrial Management at the Technical University of Munich, Germany
Boltzmannstr. 15
85747 Garching
Phone: +49 89 289 15436

Prof. Dr.-Ing. Joachim Heinzl
Dipl.-Ing. (FH) Stefan Grünwald
Professorship for Instrumentation Engineering and Microtechnics
Prof. Dr.-Ing. Michael F. Zaeh
Dipl.-Ing. Michael Franzkowiak
Dipl.-Ing. Michael Schilp
Dipl.-Ing. Adolf Zitzmann.
Institute for Machine Tools and Industrial Management at the Technical University of Munich, Germany

Optical Fibre Array Manufacture using Electrostatic Actuation

Dominik Weiland and Marc Desmulliez

A method to manufacture two-dimensional bundles of optical single mode fibres is described in this article. Submicron translational alignment accuracy is being implemented by this method. An array of micro holes, each surrounded by four electrodes, was produced using the LIGA process. Electrostatic fields between the electrodes and a metal coated optical single mode fibre inserted into such a hole were used to position the fibre inside the hole. High positioning accuracy can be realised by combining electrostatic movement and optical monitoring of the actual fibre position in a closed loop feedback alignment system.

MISEC

The Microsystems Engineering Centre (MISEC) situated at Heriot Watt University, Edinburgh, Scotland, comprises expertise in wide areas of micro engineering of 7 members of the academic staff and over 20 research associates and PhD researchers. MISEC specialises in micro-actuators, RF-MEMS and advanced assembly of MEMS.

Introduction

Requirements for two-dimensional arrays of optical single mode fibres (SMF) are expected to increase as arrays of micro machined optical emitters and detectors are now starting to become commercially available. Such arrays are forecast to be used in a growing number of possible applications in optics that require large bandwidth communication systems, switching systems and fibre array coupling elements. Current methods to produce such arrays are mainly based on passive alignment techniques that mostly use Silicon etched one- or two-dimensional arrays or micro ferrules, into which the SMF are placed. At present none of the reported passive or active alignment methods can overcome the misalignment caused by fabrication tolerances of the SMFs and at the same time be used to manufacture two-dimensional arrays.

Micro Holder

An array of micro holes, each surrounded by four electrodes, was produced using two methods: a modified LIGA process and a photo-etched glass process in collaboration with IMM Mainz. The ends of the SMFs are to be coated with a thin, conductive metal layer and inserted into individual holes, which have been filled with UV curable glue beforehand. The diameter of the insertion holes is bigger than the outer diameter of the metal-coated fibre, therefore allowing uncomplicated insertion and some movement of the fibre inside the hole as required for an active alignment

Continuation on page 34

Workshops on Microtechnical Thermal Sensors Announced

Temperature takes a special place among the physical dimensions because each energy conversion produces a heat quantity which in turn affects the temperature of the environment Furthermore, many sensors are based on thermal principles since temperature is a dimension which can be measured with relative simplicity.
In addition to the determination of object temperature, it is possible to detect the radiation energy emitted by a body (infrared sensors). Other quantities, too, like flow rate, dew point and thus air humidity, inclination, or heat conductivity can be measured besides examining, locally and at high resolution, the energy balance of physical, chemical, or biological processes (calorimetry). For this reason, a large number of well-known and technically employed sensors are based on temperature measurements.
Finally, thermal energy can in parts even be converted into electrical energy by means of the Seebeck effect. Such thermoelectric generators are gaining increasing importance for the power supply of autarkic microsystems.
On the other hand, the physical laws that permit this vast diversity of possible applications also lead to a certain difficulty in the application of thermal sensors, which is the considerable cross-sensitivity to environment parameters. Basically, the challenge in developing a thermal sensor lies in transporting the desired amount of heat to the gauging element and to convert it to a measurable change in temperature without parasitic thermal effects. This requires appropriate design and adequate layout of thermal resistances. Microsystem engineering offers very good chances for the realisation of these goals: Thin silicon nitride membranes feature very large thermal resistances and offer extremely small thermal capacities. Silicon has a large heat conductance and can be machined very precisely.
A workshop on this topic took place at the Institute for Micro and Information Technology in Villingen-Schwenningen in September 2004. Representatives of industry and science portrayed the various thermal sensor principles and offered their experience for sensor development, application, and commercialisation. This workshop was very much welcomed by a large audience from industry. In order to offer this kind of access to latest technical results also to developers in other regions, the workshop shall be repeated with speakers from European industry and research institutes at various locations all over Germany in 2005.

The next two workshops will be supported by the IRC Northern Germany to facilitate SMEs entrance to this special sensor know-how. Further information of the events and dates will be published on the IRC's web page

www.irc-norddeutschland.de

EVENTS

Courses of FSRM - Training in Microsystems:

- March 03 - 04, 2005
  Microfluidics: Pipetting, Dispensing and Microarrays
  Freiburg - Germany
- March 07 -08, 2005
  Reliability + Test of Microsystems
  Zurich - Switzerland
- March 10 - 11, 2005
  Characterization + Modification of Micro- and Nano-structures
  Barcelona - Spain

www.fsrm.ch

March 07-08, 2005
µSys Berlin - Microsystems fair and congress
www.mikrosys-berlin.de
Berlin - Germany

March 10, 2005
Free Seminar "The Challenges of Testing MEMS"
www.memmunity.com
Dortmund - Germany

March 17 - 18, 2005
9th International Forum on Advanced Microsystems for Automotive Applications AMAA
www.amaa.de
Berlin - Germany

March 21 - 24, 2005
NSTI - CEI Nanotechnology Course Series
Spring 2005 European Programme
www.nsti.org/courses
Davos - Switzerland

March 22-23, 2005
2nd Int'l Workshop on Nano & Bio-Electronics Packaging
www.prc.gatech.edu/nanobiopack
Atlanta, Georgia - USA

April 04-08, 2005
VisionOnline Course: "Advanced Nanotechnology - Materials, Processes, Structures and Applications"
Contact: julie@tfi-ltd.co.uk
Cork - Ireland

April 06-08, 2005
ECIO'05 - 12th European Conference on Integrated Optics
www.minatec.com/ECIO05/
Grenoble - France

April 10 - 13, 2005
Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT)
www.ceramics.org/meetings/am2005
Baltimore, Maryland - USA.

April 11, 2005
MEMS/MST Industry Forum of SEMI Europe
www.semi.org/semiconeuropa
Munich - Germany

April 11-15, 2005
MicroTechnology Int'l Exhibition
at Hannover Int'l Industrial Fair
www.schau-Platz.de/nano
www.hannovermesse.de/
and with **Product Market Microtechnology**
www.ivam.de
Hannover - Germany

April 13-15, 2005
ISOEN 2005 - Int'l Symposium on Olfaction and Electronic Noses
www.isoen2005.org/
Barcelona - Spain

April 17 - 20, 2005
MEMS V - ASME 5th Annual MEMS Technology Seminar
Early bird rate until Mar. 01, 2005 !
www.asme.org/education/techsem/MEMS/
Minneapolis, MN - USA

April 20 - 21, 2005
World Nano-Economic Congress Europe
www.world-nano.com
Dublin, Ireland

April 26-29, 2005
Microsystemtechnik 2005
Special fair for MST and Ultra Precision Engineering
microsystemtechnik.schall-messen.de/de/microsystemtechnik
Sinsheim - Germany

May 08-11, 2005
euspen 5th Int'l Conference & 7th Annual General Meeting
http://euspen2005.univ-montp2.fr/
Montpellier - France

May 08-12, 2005
2005 NSTI Nanotechnology Conference & Trade Show
www.nsti.org/Nanotech2005/
Anaheim, CA - USA

May 10-12,2005
SENSOR+TEST 2005
12th Int'l Trade Fair and Conferences for Sensorics, Measuring and Testing Technologies
www.sensorfairs.de
Nuremberg - Germany

June 01 - 03, 2005
DTIP 05 - Design, Test, Integration and Packaging of MEMS/MOEMS
http://tima.imag.fr/Conferences/dtip
Montreux - Switzerland

June 05 - 09,2005
Transducers '05
Reduced fee for registering boothes until March 31, 2005!
www.transducers05.org
COEX, Seoul - Korea

Call for Papers

June 22 - 25, 2005
MIXDES 2005
12th Int'l Conference "Mixed Design of Integrated Circuits and Systems"
Paper due date: Feb 28, 2005
www.mixdes.org
Krakow - Poland

Aug 28 - Sept 02, 2005
Optics and Optoelectronics
Abstracts due date: Feb 14, 2005
http://spie.org/events/poland
Warsaw - Poland

Sep 04 - 06, 2005
MME 05 - MicroMechanics Europe
Abstracts due date: June 10, 2005
www.mc2.chalmers.se/mc2/conferences/MME05/
Göteborg - Sweden

Sept 12 - 16, 2005
Optical Systems Design 2005
Conference, plenary presentations, courses, tabletop exhibition
Abstracts due date: Feb 28, 2005
http://spie.org/events/eod
Jena - Germany

Oct 05-06, 2005
Micro System Technologies 2005
Main topic fro 2005: Microsystem Packaging and Fabrication
Abstract due date: Feb 25, 2005
www.mesago.de/mst
Munich - Germany

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EV Group's IQ Aligner to Support Promerus LLC's Work on Materials for Advanced Wafer-level Packaging

EV Group (EVG), a leading manufacturer of MEMS, nano and semiconductor wafer-processing equipment, reported about the shipping and successfully installation of an IQ Aligner at Promerus LLC, a leading developer of advanced materials for applications in the semiconductor, optoelectronic and semiconductor packaging markets.

Promerus will use the IQ aligner for development of next generation wafer-level packaging materials. The advanced-packaging capabilities of the IQ Aligner, which offers customers a lower cost of ownership, include photolithographic processes to perform IC packaging at wafer level in prototype or volume production. With both 200mm and 300mm wafer-size capability, EVG's IQ Aligners offer full-field exposure, and large gap and dark-field mask alignment.

Promerus is a technology driven organization providing advanced electronic materials for the next generation of applications in the semiconductor, optoelectronic and semiconductor packaging markets. As a U.S. based subsidiary of Sumitomo Bakelite Co., Ltd., Promerus strives to deliver value to its customers and to provide a challenging and rewarding environment for its employees. More information id available at www.Promerus.com

EV Group - founded in 1980 - is a global supplier of wafer bonders, aligners, photoresist coaters, cleaners and inspection systems for semiconductor, MEMS and emerging nanotechnology markets. EV Group holds the dominant share of the market for wafer bonding equipment (especially SOI bonding) and is a leader in lithography for advanced packaging and nanotechnology. Headquartered in Schärding, Austria, EV Group operates via a global customer support network, with subsidiaries in Tempe, Arizona; Albany, New York; Yokohama and Fukuoka, Japan; and Chung-Li, Taiwan. For more information please visit www.EVGroup.com

Sieves and Meshes from TECAN are Bio-world's Most Accurate

Sieves and meshes, for the most demanding medical, pharmaceutical and bio-engineering needs, are now available from Tecan, a company based at Dorset, UK. They can be produced in standard and bespoke forms to offer, screening, filtering and particulate processing accuracy levels which are unmatched in the industry. By employing leading-edge Photo Electro-Forming (PEF) techniques, believed to be the most advanced in the world, the company is producing high-accuracy sieves with super-fine apertures which are highly consistent across the mesh. The sieves can be supplied in ASTM (American Society for Testing and Materials) standard frames, and unlike traditional frames, can meet or exceed the standard's aperture tolerance requirements.

PEF produces highly-accurate sieves with repeatable consistency, at the lowest possible cost. Typical applications include medical, pharmaceutical and food processing markets demanding the highest standards. The new sieves are fabricated in hard nickel, as opposed to the traditional soft nickel, this significantly boosts operational life, especially where abrasive materials are being processed, such as industrial diamonds. Sieves can be supplied in standard three-inch polycarbonate diameter frames, or eight-inch stainless steel frames, the latter can be full-depth (two-inch) or half-depth (one-inch). In all cases, the sieves may be specified with or without integral hard-nickel support grids. Furthermore, the company can also supply sieves with no frames, again with or without integral support grids. All apertures are highly accurate and, regardless of the aperture size, or shape (square / round), have tolerances of +/- 2µm.

More information is available at www.tecan.co.uk

enablingMNT Report on Test and Measurement Equipment and Services

Unlike electronic devices, where only electrical parameters need to be tested, MNT devices require precise measurement of multi domain and interrelated parameters. Testing of MNT products is much more complex then testing of standard electronic components. As MNT devices move from R&D and low volume to high volumes, metrology becomes increasingly important, while accurate, reliable and valid testing is a key to improving the quality and yield of MST/MEMS devices. Demands on test equipment shift to throughput and automatic handling of products and data. The latest in a series of enablingMNT reports offers information about used technologies and companies active in this area.

In general enablingMNT offers information on the complete supply chain that enables a flexible and economical MNT manufacturing: the service and equipment suppliers of micro and nanotechnology such as foundries, design & engineering companies, front end equipment suppliers, etc. The reports are available at 280 each. In addition to the series of reports, enablingMNT also offers consultancy. www.enablingmnt.com

DARPA Intends to Support Process Run Submissions to be Executed through the MEMS Exchange Network

Recently the US Defense Advanced Research Projects Agency DARPA published a Broad Agency Announcement (BAA), specifically BAA-05-12, soliciting proposals for funding opportunities related to the MEMS Exchange. Specifically, DARPA intends to support process run submissions from the community that will be executed through the MEMS Exchange network of foundries. Preferably, these process run submissions should demonstrate and challenge the fabrication capabilities of the MEMS Exchange. This is a unique opportunity for US MEMS developers to get funding support from DARPA to help cover the fabrication cost of implementing their MEMS devices through the MEMS Exchange while simultaneously obtaining innovative MEMS devices that would be otherwise difficult or impossible to realize. DARPA , the leading Governmental organization in the United States for the advancement of MEMS technology , is sponsor of the MEMS Exchange program as well as . The primary charter of the MEMS Exchange has been the establishment, operation, and refinement of a unique fabrication resource, which has been providing fabrication services to the entire MEMS community since it was established in 1999. The MEMS Exchange has developed into a national fabrication resource that allows MEMS developers from anywhere in the country to implement their MEMS devices with far easier access and greater design and

process freedom than from any other source. Please review the solicitation at the DARPA Web site:
http://www.darpa.mil/baa/#eto

Competitive Call For an Additional Project Partner at SHIFT (Excerpt)
The project "IST-IP-507745-SHIFT", Smart High-Integration Flex Technologies currently active in the Sixth Framework programme of the European Community requires the participation of a new project partner to carry out Large Area Panel (LAP) processing tasks: HiCOFlex (http://www.hightec.ch/index1.html) processes shall be transferred to existing 12" x 12" or 24" x 24" facilities. Expansion of LAP processes to the processing of polyimide, sputtering and photolithographic processing of conductors shall be developed. A defined set of process steps shall be carried out. Proposers should possess the infrastructure necessary. The duration of participation is expected as June 2005 to December 2007. Total Commission funding available is 170.000 for research activities (estimated 320.000, to be supported by Commission funding up to 50%), small additional training as well as consortium management activities (to be supported by EC funding up to 100%). The proposal should be submitted in English Language. Date of close of call : March 16, 2005 Time of close of call - 17h00 Brussels time.
The full call text, also indicating the defined process steps to execute, and further information is available at
www.vdivde-it.de/portale/shift/
or from the project co-ordinator
IMEC/INTEC/TFCG,
Mr. Jan Vanfleteren
e-mail: Jan.Vanfleteren@elis.ugent.be

Yole Collaborated with 2 World Famous Technical Experts to Contribute to the Realization of Common Market Analysis
End of last year, Yole Développement has collaborated with 2 world famous technical experts to contribute to the realization of common market analysis. The 1st report was released in December 2004 in collaboration with Glennan Microsystems Inc. (US). This publication describes new developments and market opportunities for MEMS in harsh environments. Until recently, MEMS devices were limited to standard environment use. Now, extended applications are possible using new materials such as SiC or SOI. With the remarkable contribution of QinetiQ (UK), the "MEMS on IC" study analyzes the technology and the applications of MEMS integration. This report (Nov. 2004) explains how the market share of integrated MEMS will grow from 41% in 2003 to almost 50% within 2 years. Indeed, the MEMS business is under strong reorganization. Since the last few years, there has been a strong involvement of IC manufacturers to find new opportunities business in MEMS, especially in large volume markets.
Yole is in contact continuously with worldwide key players to help them to understand the markets and technology trends MEMS and compound semiconductors markets.
Reports to be released in 2005 are:

- Optical MEMS applications for non telecom markets (B$3 market in 2008)
- Emerging markets for microfluidic applications (B$2 market in 2010)
- MEMS for applications in mobile phones (M$ 250 market in 2008)

Read all about Yole at
http://www.yole.fr

MicroNanoWorld - Munich Fair Sets up a New Brand
Munich Fair GmbH, the organizer of several well renowned technology fairs at the new fairground in Munich, Germany, has set up MicroNanoWorld, a new brand as "roof" for all activities in the fields of micro- and nanotechnologies. According to the particular fair or congress, MicroNanoWorld will be particularly focussed. MicroNanoWorld at Productronica 2005 will focus on solutions for micro and nano production. It will show processes, process chains and process equipment for all needs in production of microsystems. The technical scope of MicroNanoWorld will include assembly, connection and packaging technologies, materials, simulation and design methods and tools, equipment for production, assembly, placement, handling and mounting as well as ultra precision machine tools, bonders, measurement equipment, complete process chains and so on. Further focal points are the "MicroSystemsTechnology User Forum", the "Product Market Microtechnology" and live presentations at demo production lines.
MicroNanoWorld at electronica 2006 however will be the industry platform for micro and nanotechnical products and their applications. Focal points are micro-components, -sensors, -actuators and -systems, displays and various branch specific applications. Another focal point is the "World of MEMS" in the field of semiconductors.
This approach enables the new brand MicroNanoWorld to represent the whole value creation chain and allows to benefit in an optimal amount from the well established and worldwide well renowned fairs Productronica and electronica. More information will be given in the next mstnews issue and will soon be available at
www.messe-muenchen.de/id/26013

Colibrys Acquires Applied MEMS Business from I/O
Merged Entity will be a Leading Global Provider of Advanced MEMS Technology
Input/Output, Inc. (NYSE: IO) and Colibrys SA, a privately held firm based in Neuchâtel, Switzerland, announced in the end of 2004 that Colibrys has completed the acquisition of the Applied MEMS subsidiary from I/O in an all-stock transaction. Colibrys designs and manufactures high-performance MEMS products and offers contract manufacturing services for MEMS devices to customers in the defense, aerospace, telecommunications, life sciences, industrial imaging, and energy industries. The new company, which will retain the name Colibrys and remain headquartered in Switzerland, will become one of the largest and most technologically advanced firms in the global MEMS industry. I/O will retain a minority equity interest in the new company and hold one seat on the Colibrys Board of Directors. I/O also will retain ownership of all intellectual property associated with the Applied MEMS business and will license this technology to Colibrys as part of the transaction. Moving forward, Colibrys will be the supplier to I/O of MEMS accelerometers used in the company's VectorSeis digital, full-wave seismic sensors while I/O will have preferential rights to Colibrys' MEMS technology for seismic applications involving natural resource extraction. Additional information is available at:
www.i-o.com/About_us/News_Room

NEXUS and EC Representation at the "Healthy Opportunities from Small Technologies Forum", Melbourne, Australia, Dec 2004

How can we connect cells, bytes and molecules with R&D, industry and inventors - that was the subject of a two-day international forum held in Melbourne, Australia, recently. The second Asia-Pacific MicroNano Commercialisation Workshop, 9-10 Dec 2004, was designed to build a more cohesive and focused business environment for the commercialisation of micro and nano technologies in the Asia-Pacific region.
The 2004 workshop was run as a two-day forum with the theme "Healthy Opportunities from Small Technologies". The term 'small technologies' refers to the integration of micro-, nano- and biotechnologies with information technology. The workshops provided networking opportunities for the commercial development of small technologies in health care, as well as the chance to share views.
The event focused on the impact of small technologies on the future of health care in terms of the business development environment and the challenges posed to society by the increasing prevalence of these technologies. With over 20 key speakers from the US, Europe and the Asia-Pacific regions, the forum attracted more than 200 key health stakeholders. Representatives from companies, academic institutions, government, the media and the broader community provided a stimulating exchange of ideas through presentations and panel discussions. Case studies in key emerging technologies included: biomaterials for implants and tissue regeneration; diagnostics and imaging through biosensors; therapeutics in new drug delivery systems; and associated prospects for the personalisation of health care through information technology.

The European Commission was well represented by Dirk Beernaert, Head of Unit, Micro and Nanosystems, Integration, Information Society Technologies (IST), who gave a keynote address on European direction and strategy for the exploitation of 'smart' micro and nano technologies for the ambient intelligent environment. The NEXUS Association was represented by Steering Committee member Patric Salomon, who delivered an overview on NEXUS' role and added value in launching the User-supplier Clubs. His presentation highlighted the success of the NEXUS User-supplier Club "Medical" (led by Diana Hodgins, ETB), the development of a technology-application roadmap and the launch of new user-driven international collaborative projects in the medical sector. Organisations in Victoria are looking for the implementation of ideas similar to the NEXUS concept in order to increase exploitation of results from the well-developed academic R&D infrastructure in the Melbourne area.

The forum was part of the Victorian Government's ongoing development strategy for small technologies with a focus on applications. The Victorian Government is facilitating the establishment of the Australian Small Technologies Alliance (www.smalltech.org.au) through the formation of 'sector initiative groups' (SIGs) - an approach similar to the NEXUS User-supplier Clubs. It is expected that a number of SIGs will develop as a lead-up to the industry-focused 2nd National Nanotechnology Conference, 26-28 Sep 2005, Melbourne, Australia (www.mateng.asn.au/Nano2005/TechProg.htm). The Alliance will help promote international linkages and strategic partnerships to exploit the emerging business of nanotechnology and microtechnology in key sectors, including health, textiles, food, automotive and materials.

Australian companies and research centres are already actively engaging with European partners developing project proposals that address EU FP6 calls, especially in the area of medical and health applications of small technologies. Australia offers its European partners: unique scientific and technical excellence; access to the Asia-Pacific region; and access to Australia's well-developed, compliant and regulated health care system. Australia also has a thriving biotechnology industry.

Contacts:
Harry Buskes
E-Mail: harry.buskes@iird.vic.gov.au
Michael Krien
E-Mail: michael.krien@iird.vic.gov.au
DIIRD Victoria, Australia
www.innovation.vic.gov.au

Andrew Campitelli
MiniFAB (Aust) Pty Ltd, Australia
E-Mail: andrewcampitelli@MiniFAB.com.au
www.MiniFAB.com.au

Patric Salomo, 4M2C, Germany
E-Mail: patric.salomon@4m2c.com

A new NEXUS USC/MWG on "Ambient Intelligent Environment"

The creation of a new, combined, NEXUS User-Supplier-Club (USC) and Methodology Working Group (MWG) to focus on the Ambient Intelligent Environment from a micro/nano technology (MNT) perspective was discussed at a meeting of experts on the 13th of March 2005 in Prague. Attending this meeting were representatives from industry, academia, research and NEXUS who have all agreed to formally launch this new USC/MWG with the following specific aims:

- To clarify the opportunity offered by the ambient intelligent environment to MNT
- Establish a forum for engaging users, human factor experts and technologists and
- Widen the scope of ambient intelligence beyond that of the smart home.

To this end, this initiating group has undertaken to disseminate information and attract participation at forthcoming meetings.

Contact:
Dr Ayman El-Fatatry
E-Mail: a.el-fatatry@lboro.ac.uk

"4M Network of Excellence" to Organise First International Conference on "Multi-Material Micro Manufacture", Karlsruhe, 29 Jun - 1 Jul 2005

Broadening the range of microsystems-based products and simultaneously multiplying their capabilities requires the integration of new materials and precision-engineering technologies for their processing with IC-based, batch-fabrication processes. The present suite of microtechnologies will not be able alone to meet the manufacturing demands for high aspect ratio structures, enhanced forced microactuation, improved environment resistance and high-precision microcomponents. These are the biggest challenges to micro product development and at the same represent promising research and development areas for innovation and value creation. In this context, the main goal of the Conference is to provide a forum for experts from industry and academia to share the results of their in-depth investigations and engage in interdisciplinary discussions about micro-technologies for batch-processing of metals, polymers and ceramics, and the development of new production platforms for multi-material micro products.

The conference will take place at the Centre for Advanced Technological and Environmental Training of Forschungszentrum Karlsruhe (www.fzk.de), Germany.

Papers are invited on all aspects of manufacturing of metal, polymer and ceramic microstructures and their application in microsystems-based products, in particular, but not limited to:

Micro-TECHNOLOGIES
- Polymer Processing
- Processing of Metals
- Processing of Ceramics
- Metrology
- Assembly and Packaging

APPLICATIONS
- Microoptics
- Microfluidics
- Micro-Sensors and Actuators

Submission of Abstracts shall be electronic only at:
www.4m-net.org/4M_Conference
Deadline: 31 March 2005

Contact:
Dr. Stefan Dimov (Co-Chair)
Jeanette Whyte (Conf. Secretary)
Cardiff University, UK
E-mail: whytejc@cf.ac.uk
www.4m-net.org

The NEXUS Market Analysis for Microsystems III to be Available in Sep 2005

Since 1998, the NEXUS Market Analysis for Microsystems has been the most recognized source of market figures for Microsystems worldwide. The Task Force Market Analysis led by WTC is currently preparing the updated report entitled **"Market Analysis for Microsystems III 2004-2009"**. This follows on from the highly successful 1996-2002 and 2000-2005 report that has become industry standard. The updated report will be available in Sep 2005.

New features of the upcoming report:
- New products: MEMS Microphones, MEMS based RFID tags, Micro-reaction products, Micro energy sources, Micro pumps
- New application fields: Logistics, Ambient intelligence
- Regional analysis: North America / Europe / Asia / Rest of the World

Task Force core members:
- Henning Wicht, Chairman, WTC (D)
- Ayman El Fatatry, BAE Systems (UK),
- Friedrich Götz, FH Gelsenkirchen (D)
- Henne van Heeren, EM3 (NL)
- Jérémie Bouchaud, WTC, (D)

Contact:
Henning Wicht
E-Mail: Henning.wicht@wtc-consult.de

NEXUS Contact

NEXUS News is provided to NEXUS members and other interested mst-news readers by the NEXUS Association.

The NEXUS Association is partly funded through the NEXUSPLUS project within the EC IST programme in FP6 to:

- Disseminate and cross-fertilise between FP6 Integrated Projects and Networks of Excellence.
- Increase ACC participation in NEXUS activities and within EC FP6 projects.

NEXUS Office
c/o Leti, France
E-mail: NEXUS@cea.fr
www.nexus-mems.com

NEXUS News Contact
Patric Salomon, Germany
NEXUS News Editor
4M2C PATRIC SALOMON GmbH
E-mail: nexus-news@4m2c.com

NEXUS Membership

NEXUS Membership is open to all companies and institutes, worldwide, that are able to contribute expertise in areas relevant to microsystems technology.
To apply for membership, complete the online questionnaire for the NEXUS Who's who on the NEXUS website:
www.nexus-mems.com

2003 - Restart of Microsystems Activity

After a difficult year in 2002, caused by a global economic downturn, 2003 has shown a promising business recovery. This was demonstrated, for example, by an increase in the total value of quotations by 43% and of orders by 70% (see table below).

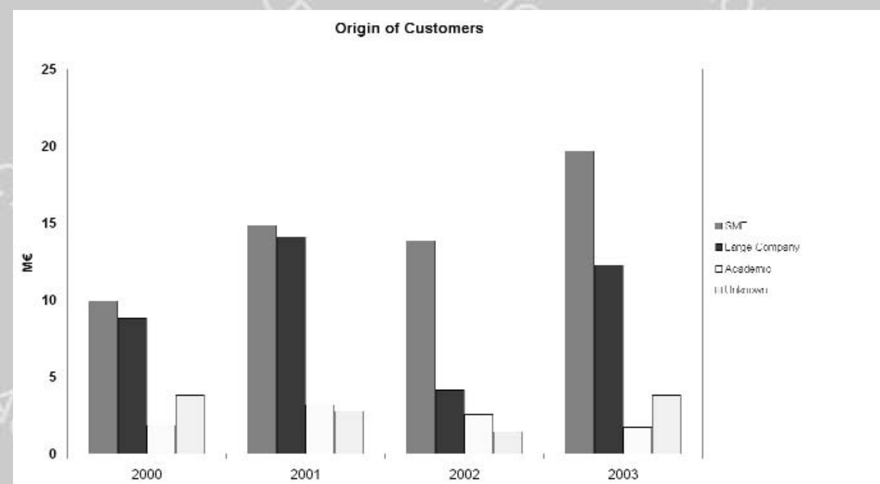
The launch of the Framework 6 program in 2003 has been reflected in the results with approximately 6.2 M of the budget being directed to European Commission funded projects. Large enterprises are the most active with Europractice partners in European projects, with only 11% involvement of SMEs and 20% from academic partners.

	2000	2001	2002	2003
Number of Partners providing data	44	45	49	47
Number of Contacts	1105	1114	1362	1443
Number of quotations	505	612	500	571
Total budget of quotations	38.7 M€	47.0 M€	47.3 M€	68.6 M€
Average Budget	76 K€	76.8 K€	94.6 K€	120.1 K€
Number of contracts	347	379	365	351
Total budget of contracts	24.3 M€	34.8 M€	21.9 M€	37.7 M€
Average Budget	70.0 K€	91.8 K€	60 K€	107.4 K€

The activity of larger companies has recovered to the level of 2001 and SMEs continue to be more and more active, (see diagram 1). In contrast, since 2001, the turnover from the academic sector continues to decrease, due principally to a reduction in the average budget for each programme.

In Europractice 4, SMEs generate 58% of business while large companies account for 36%.

Noteworthy in the ranking of the most proactive countries are the USA, in third place, with a total turnover of 5 M (13.6% of business) and Israel in 7th place. Despite a significant level of activity in quoting to Japanese companies, the resulting level of business remains very low (few k).

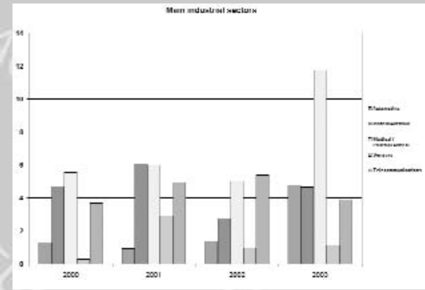


"Origin of Customer"

Business with partners from Eastern Europe is taking off rapidly. During the first two years of Europractice 4, the total budget was 0.75M , 90% of which was in 2003. This provides a clear indication that efforts to integrate the industrial and academic partners from the ACC are becoming effective.

The major European countries are France, Germany, The Netherlands and Norway (with 7%), and the UK and Switzerland.

As in previous years, the biggest drivers come from the medical, instrumentation and telecommunication sectors, with an upturn in the automotive sector in 2004. Business in the medical and pharmaceutical sectors has increased by a factor of two compared to the three previous years (from about 6M to 12M).



"Main industrial sectors"

In conclusion: 2003 has been a very good year in terms of quotations and turnover. The application of Microsystems in the medical and pharmaceutical sectors is increasingly important and the business generated by ACC partners has taken off.

During Europractice 3, the leverage effect of the European Commission funding was close to a factor 5 on the Microsystems business. With the economic downturn year 2002, this factor decreased to 3 but, with the business recovery, the leverage effect was superior to 5 this year, demonstrating an excellent level of return.

www.europractice.com

Review of the five EuroTraining Train-the-Trainers Courses

The EuroTraining project is approaching the end of its third cycle. In harmony with the previous two cycles, the main objective of this third phase of the EuroTraining project has been to provide means to step up the development of European knowledge in microsystems and microelectronics-based components and subsystems technology. The Train-the-Trainers action, a vital component within the project, supported this objective by providing dynamic education for those who teach. Train-the-Trainers addressed new challenges faced by teachers of electronics technologies. It was a response to the call for a change in teachers' competence and thinking, caused primarily by the multidisciplinary and fast-changing nature of advancing technologies.

In a first step a gap analysis among universities of the NAS countries was carried out to determine relevant course topics, level and program, course providers and lecturers, sites, etc.
The gap analysis showed that there was a most significant need for courses of microelectronics and microsystems design, applications and marketing.
It was also discovered that there was no tradition, even not any example, for the organization of such a high-level intensive course on these topics in the region. The help of Technology for Industry Ltd, experienced EuroTraining Partner from UK, and VisionOnline, another EC-sponsored project, was requested to give a good start to the Train-the-Trainers action, and to provide a model for the organization of the courses.

The following Train-the-Trainers courses were provided in four different NAS countries:
1. Microelectronics and Microengineering, May 12-16, 2003, Budapest, Hungary.

2. Design Techniques and Tools for Low-Power Digital Systems, December 14-18, 2003, Cluj-Napoca, Romania.

3.-4. Sensors and Actuators based on Microelectronics and MEMS Technology or Design and Complex Characterization of High Performance PCB Structures, two-day parallel courses, May 12-13, 2004, Technical University of Sofia, Bulgaria.

5. Microelectronic Sensors and Actuators with Biomedical Applications, four-day intensive course, 6-9 Dec 2004, Warsaw University of Technology, Poland.

Conclusions
The special objective of the Train-the-Trainers action of the EuroTraining Project, that is to provide knowledge transfer for the trainers (professors, instructors, teachers) in the Newly Associated States (NAS, now called NMS or ACC) of the European Union, was successfully realized. Five intensive courses, with a total of 17 lecturing days, in four sites of different NAS countries were provided for altogether 153 attendees, by the contribution of recognized West and East European professors.

About 80% of the participants were young academics, active or prospective teachers (PhD students, young researchers, post-docs) from NAS countries, who showed very high interest in the new disciplines of microsystems and MEMS technologies, design techniques and tools, microsensors and actuators, biosensors, and the great many applications lectured during the five courses.

The Train-the-Trainers action improved European coverage and gave an impetus to the development of European knowledge in microsystems and microelectronics-based components and subsystems technology, regarding the aspects as follows:

- The scientific level, educational and technological skill of ca 140 East European trainers of microsystem engineering was improved by this EC-sponsored West-to-East knowledge transfer action;
- 5 new courses were included into the EuroTraining Course Directory, all of them with the contribution of NAS lecturers;
- 4 new sites (Budapest, Cluj-Napoca, Sofia, Warsaw), all from NAS (Hungary, Romania, Bulgaria and Poland) were touched by the success of the West-to-East knowledge transfer;
- 5 new course providers from NAS joined their ca 60 Western counterparts in the EuroTraining Course Directory, namely: Budapest University of Technology and Economics, Politehnica University of Bucharest, Warsaw University of Technology, Wroclaw University of Technology, and Institute of Electron Technology (Warsaw);
- 12 recognized professors from 7 European countries (including 3 NAS) were contributing to the success of the knowledge transfer action;
- on the basis of the lectured courses, 4 new Distance Learning courses were developed and included into the EuroTraining Course Directory;
- most of the lecturers joined the EuroTraining Microsystems Training Service, a new program for those who already work on a degree course, to combine competences, knowledge and know-how and to share educational resources.

Contact
EuroTraining office
E-Mail: eurotraining@polito.it
www.eurotraining.net

Europractice at Hanover Fair, 11-15 April 2005

Europractice will have a booth at this year's Hanover Fair. The booth will be shared with the EC-funded Network of Excellence "Design for Micro & Nano Manufacture (PATENT-DfMM)" and will be located within the IVAM pavilion at the "Microtechnology special area", Exhibition Hall 15, Booth D 36.

Contact:
Patric Salomon
4M2C, Germany
info@4m2c.com

International Cooperation Forum on "Wireless Systems for Biomedical Applications & Devices" on 25 - 26 April 2005

Wireless technologies do more and more dominate and simplify our daily lives. This development is not only restricted to the well-known applications in consumer markets. 'Wireless' is also a keyword for a multitude of technologies and applications in the biomedical area that improve the quality of life and reduce the costs of patient care. Telemedicine and invasive monitoring, active implants and camera pills as well as PDAs for medical information systems are only some of the various and very different examples within this dynamic and fast evolving field in biomedical technology & application.

The multiple and very different wireless technologies in combination with the high demands as well as the various risks in development, production and marketing of biomedical devices - such as quality standards, regulations and the differences between the national healthcare systems - do render this field very complex and complicated. Multidisciplinary know-how and international cooperation is the only way to tackle this situation.

This is why the Biomedical Competence Centre MEDICS is preparing the International Cooperation Forum on Wireless Systems for Biomedical Applications & Devices. The Forum is based on the well-known and successful 'one-to-one' concept. That means, participants have the possibility to select registered organisations they wish to meet in a match-making process prior to the event. The goal of the Forum is to establish valuable business contacts between technology & service providers and users coming from R&D and clinical institutes, SMEs and LEs. Therefore, the Cooperation Forum focuses on decision-makers in product, technology and R&D management.

Date: 25 - 26 April 2005
Venue: Fraunhofer-Institut für Biomedizinische Technik (IBMT), 66280 Sulzbach, Germany
Deadline for registration and questionnaire submission: 4 March 2005
Deadline for the selection of organisations you wish to meet: 1 April 2005
The Forum participation will be limited to 50 organisations.

Registration and further information:
www.medics-network.com/wireless

Contact:
Fraunhofer IBMT - MEDICS Coordination Office, Germany
Andreas Schneider, Head of MEDICS
Email: medics@medics-network.com
www.medics-network.com

MEMSOI - New Pricing Policy for the MPW Service

For the 6th year of operation of the MEMSOI Multi-Project Wafer service TRONIC'S reduces the cost of the service for both commercial and academic organisations in order to facilitate access to SOI MEMS prototypes. As usual a sliding scale price is offered when ordering multiple locations. For each location the customer gets 20 dies packaged at the wafer level.

Price/location/run	Corporate	Academic
For 1 location	6,500 €	4,200 €
For 2-3 locations	5,800 €	3,500 €
For 4-5 locations	4,500 €	3,000 €

The 2005 MEMSOI MPW schedule is shown in the following table.

Run	Design submission (GDSII format)	Delivery (20 chips)
21	Feb. 1 - 2005	May 31 - 2005
22	April 1 - 2005	July 31 - 2005
23	July 1 - 2005	Oct. 31 - 2005
24	Oct. 1 - 2005	Jan. 31 - 2006

Design guidelines and a Coventor design kit are available upon request.

Contact
TRONIC'S Microsystems, France
Vincent Gaff
Email: memsoi@tronics-mst.com

EP Contact

EUROPRACTICE News is provided to mstnews readers by EUROPRACTICE Microsystems Service for Europe.

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EUROPRACTICE Programme Manager:
Leonello Dori
European Commission, DG INFSO C2
E-mail: Leonello.Dori@cec.eu.int

EUROPRACTICE News Editor:
Patric Salomon
4M2C PATRIC SALOMON GmbH
E-mail: ep-news@4m2c.com

For information on specific activities within Europractice, please contact Competence Centers, Design Houses and Manufacturing Centers directly. Contact information can be found at www.europractice.com

NoE PATENT-DfMM to accept additional Project Partners

The EC-funded Network of Excellence PATENT-DfMM aims to build a new technical community to address the problems of designing Micro & Nano Technology based products that are reliable, testable and manufacturable. PATENT-DfMM has identified a need for additional partners in the following areas:

- Design for Testability
- Packaging of Fluidic based Devices and Systems
- Fluidics and Bio-MEMS Reliability Engineering

A "Call for new Contractors" is planned to be published on the project's website in Jan 2005. The call is scheduled to be open until 28 Feb 2005 for proposals from universities, research centres and companies who have a proven international reputation in the above fields. As the existing partners have committed a significant resource of their own to the programme in preparation, negotiation and in-kind support to the objectives of the project, applicants should clearly demonstrate not only what skills and resources they would make available to the NoE but also what their institute or company will contribute.

Contact:
Andrew Richardson,
Lancaster University, UK
E-Mail: A.Richardson@lancaster.ac.uk
www.patent-dfmm.org

DfMM Training and Business Development Projects launched

Being an FP6 Network of Excellence, PATENT-DfMM has a very flexible approach to distribute budgets within the project. In an annual (internal) review, which is supported by the Industry Advisory Board (IAB), priorities for the next period will be set. Internal calls for project proposals are launched throughout the year.

The following internal projects have been launched recently:

Training Course Development

Course of MEMS Failure Analysis (IMEC)

Course in MEMS Packaging, Modelling & Analysis (IZM, IEF, ULAN, HWU, IMEC)

Distance Learning Course in MEMS Modelling (ULAN)

PATENT-DfMM Business Development

Access Service for MNT based Sensors (Qinetiq, ULAN, 4M2C).

This project will build a concept to extend the Europractice INTEGRAM service to DfMM and Packaging forming a core dissemination route for the PATENT-DfMM services portfolio.

PATENT-DfMM SME Support

Application of MEMS Test Strategies to MEMS for Detecting Faults in Aircraft Wiring (ULAN, BCF Designs, HWU).

Integration of DfT and test know-how into a new MEMS device to be designed and commercialised by an SME. Success will result in investment in the NoE PATENT-DfMM.

More information is available from the PATENT-DfMM website www.patent-dfmm.org

Andrew Richardson
Patric Salomon

Industry Partners sought for "Bio-sensor Design for Testability Project"

This project is running under the NoE PATENT-DfMM WP1 and involves MESA+ (Twente), LIRMM (Montpellier) and Lancaster University. Work has to date been based around published devices. The team are now looking for a good combination point between the design for Testability (DfT) techniques and the specific properties of the integrated bio-sensor system to give an appropriate DfT structure and compensation circuitry to the bio-sensor array.

We are looking for an industrial partner who can provide a demonstrator and a manufacturing route for prototypes. As a result of the project, the industry partner will receive detailed information about the DfT strategies developed and the project partner's work.

Contact:
Hong Liu, Lancaster University, UK
E-Mail: h.liu@Lancaster.ac.uk
Hans Kerkhoff, MESA+, The Netherlands
E-Mail: H.G.Kerkhoff@utwente.nl

PhD Job Opportunity at Lancaster University: Management & Coordination Support Officer

Lancaster University is seeking applications from highly motivated individuals to join the PATENT-DfMM project coordination team that currently consists of legal and contract specialists, financial support and overall project coordination. Duties would include:

- General project management including monitoring of deliverables and support to the project management board
- Business Development including investigation of risk and contractual issues associated with business models, building inventories of skills and expertise and portfolio development for the technical
- Coordination of funding requests and support to the universities research support office in account management.

Contact:
Andrew Richardson
Lancaster University, UK
E-Mail: A.Richardson@lancaster.ac.uk

DfMM Contact

DfMM News is provided to mst-news readers by the project "Design for Micro & Nano Manufacture (Patent-DfMM)", a Network of Excellence funded by the European Commission DG INFSO E5 within the Information Society Technologies (IST) Programme of FP6.

The NoE Patent-DfMM aims to establish a collaborative team to provide European industry with support in the field of "design for micro nano manufacture" to ensure that problems affecting the manufacture and reliability of products based on micro nano technologies (MNT) can be addressed before prototype and pre-production.

NoE Patent-DfMM Co-ordinator:
Andrew Richardson
University of Lancaster, UK
E-mail:
A.Richardson@Lancaster.ac.uk

NoE Patent-DfMM News Editor:
Patric Salomon
4M2C PATRIC SALOMON GmbH
E-mail: DfMM-news@4m2c.com

www.patent-dfmm.org

Technical Committee and Board Labelling Meeting Held in Paris on 16th and 17th December 2004

Technical Committee and Board labelling meeting held in Paris on 16th and 17th December 2004
Two proposals were evaluated during this meeting, viz. EPADMID and SMARTIS. Here are their titles:

- **EPADIMD** (European Platform for Advanced Active Implantable Medical Devices) EM91
- **SMARTIS** (Smart Thin Films on Alumina Substrate) EM95

SMARTIS got the EURIMUS label and EPADIMD will be re-evaluated following the request for a technical addendum.

Telemarketing action
In order to promote EURIMUS and spur on the setting up of new projects, a telemarketing action will be launched at the beginning of 2005. This action will be an opportunity for the EURIMUS Office to identify new project ideas or potential future partners and, if necessary, help the consortiums to build up their proposals (finding partners, checking with them if the proposals fit the EURIMUS objectives, getting in touch with public authorities, giving advice for writing proposals, etc.).
Two circles will be in the focus for this action: existing EURIMUS partners and potential new partners.
Thanks in advance to the people that are contacted for welcoming the EURIMUS collaborators in charge of this telemarketing action and for answering their questionnaire.

Brainstorming action
During the latest EURIMUS Board meeting, a presentation of the mature technologies available in the five institutes members of the EURIMUS Board was given by each representative (Fraunhofer IZM (D), CSEM (CH), IMEC (B), CEA-LETI (F) and SINTEF (NO)). The idea was to present to the industrials Board members the technologies available to set up new EURIMUS projects. All the participants were very interested in this initiative and some ideas will certainly generate new projects. This initiative will be re-launched regularly and enlarged to all the institutes members of EURIMUS.
This technical information could soon be available on the EURIMUS website to open discussions outside the EURIMUS Board and Technical Committee members and then provide new projects.

In the following the EURIMUS Board competence grid:

Materials	CNR
Design & simulation	Memscap, IMEC, VTT, Sintef, CEA-LETI, CSEM, Sonion
Basic processes	CNM, MIC, CEA-LETI, CSEM
Manufacturing	ST, Memscap, SensoNor/Infineon
Pack. Assembly & Test	Sonion, FhG-IZM

Communication	Transport	Medical	Energy	Process control	Aerospace
ST Micro. Sonion EADS	Fiat VTI Hamlin Sensonor/Infineon Temic Conti	Sonion MEMSCAP	Schlumberger Sensonor	Mondragon	EADS Thales Avio MEMSCAP

Geo-science	Environment	Ecommerce	Consumer products	Computer games
Schlumberger	Schlumberger	Schlumberger	Olivetti Mondragon	Thales MM Logitech

EURIMUS calls in 2005
Warning: New procedure:
In this calendar a deadline has been set for Project Outlines (PO) and Full Project Proposals (FPP) registrations. All the coordinators will have to send their proposals by email to the EURIMUS Office for registration a couple of weeks before the deadline for submissions (see calendar for deadlines) expires.

Changes for the fourth call:
As mentioned in the latest MST News issue, two calls will be launched in 2005 (calls 3 and 4). But the second call of the year (call 4) will have dates differing from those given earlier. Here is the updated calendar:

EURIMUS Contact

EURIMUS OFFICE
Phone: +33 438 78 36 38
Fax: +33 438 78 56 70
E-Mail: EURIMUS@cea.fr
www.eurimus.com

	Call n°3	Call n°4
Call launches	**Thursday, 13th January**	**Thursday, 4th August**
Closing date for PO registration	Friday, 11th February	Friday, 9th September
Closing date for PO submission	Thursday, 3rd March	Thursday, 22nd September
TC evaluation meeting	Friday, 11th March	Friday 30th September
Closing date for FPP registration	Friday, 8th April	Friday, 28th October
Closing date for FPP submission	Thursday, 28th April	Thursday, 17th November
TC evaluation meeting	Thursday, 12th May	Thursday, 1st December
Board labelling meeting	Friday, 13th May	Friday, 2nd December

Function Follows Form - How to use the Advantages of Flexible Circuits

Flexible circuits are gaining ground. Their success is based on the new possibilities of flexible modelling, of making movable connections, of reducing weight and space as well as high reliabilities under dynamic stress. These are exactly the characteristics required by applications for automobile and automation technology, for mobile communication devices or medical technology.
Acting on this trend, VDI/VDE-IT, in cooperation with partners in industry and research, presents the live production of a module on a flexible circuit board. The experts of the Fraunhofer Institute IZM, while demonstrating the assembly line, will explain the special technological conditions, specific requirements concerning the handling of flex material and criteria of decision for the use of flexible circuit boards.
Four demonstration isles will support these presentations, where the capabilities and advantages of flexible circuits are shown on the basis of the latest R&D results and products. Applications in the fields of logistics, medicine, automation and communications will be on display to represent their manifold uses.
The portrayal of the project results of the BMBF's "Microsystems" programme will complete the presentation.
For further information about the presentation, please contact:
VDI/VDE Innovation + Technik GmbH
Lutz-Günter John,
Phone: +49 3328 435 158
E-Mail: john@vdivde-it.de

You can Develop Microsystems More Easily and for Less Money - With the Right Tools

The development of efficient microsystems sometimes consumes a lot of time and money. Many different micro technologies and different physical principles have to be integrated and brought in line - mostly in hybrid systems. The results are immensely capable systems - but most of the time only after a great effort has been made.
The fastest and most efficient way for developers to achieve their goal is the use of computer-aided tools for the design or the simulation of new microsystems or their components. These tools allow the best product design, because several variants can be tested in a simple way. The efficiency of the designed systems will thus be optimized and their chances on the market improved significantly.
Indeed, small- and medium-sized companies (SMEs) are often not able to afford this kind of CAD tools, because, especially at the beginning, significant investments, expensive courses and training for the staff are unavoidable.
The support given by the Federal Ministry of Education and Research (BMBF) will enable SMEs to use new computer-aided design tools for their next project already. Under its "Microsystems 2005" programme the BMBF is allocating 2.5 million Euros, focused thematically on the "first use of computer-aided tools for design and simulation in microsystems technology". SMEs may send in their draft projects by the end of September 2005. Funding will start at once. Therefore, the sooner the drafts are made available, the earlier the authorization and thus the start of the project will be possible. Participation is limited to free-market companies whose annual turnover and balance sheet total do not exceed 40 million Euros and 27 million Euros, respectively and that employ a staff of 250 or less.
Specific projects for the development and advancement of microsystems or complex microsystems components will be funded. The application of computer-aided design tools not available in the company before is required for funding. Introduction and first-time use must constitute a significant financial and man-power effort for the company.
The design of microsystems components and microsystems makes great demands on developers and the design tools used. Design aid from beginning to end, which is widely practised in microelectronics for example, will not be available for microsystems in the foreseeable future. But there is a series of tools on the market that can be fully used for particular development phases. If used, they can reduce the time and cost of development by a considerable margin.
Many of the applicable tools typically were first developed for other applications, where they are still predominantly in use. Meanwhile, additional targeted developments and model libraries make them very well applicable to the development of microsystems.
The BMBF has been funding the advancement of such tools and the improvement of development processes in SMEs for quite a while. Under the previous MST programmes SMEs were also supported when new development tools were employed. The cooperative project EKOSAS for example, which ended two years ago, is aimed at eliminating the existing deficits in the present CAD environment for the design of new Sensor-Actor Systems. Three typical microsystems were used to show how to achieve a better design aid by using advanced CAD software. One SME for example developed a positioning sensor for dental diagnostics as part of a project. The company, supported by other partners of this project, was able to use FEM calculations, system modelling and simulation to clearly accelerate the design and optimization of the sensor and to achieve the best possible development result.

For more information about the main topic "first use of computer-aided tools for design and simulation in microsystem-technology", visit: www.vdivde-it.de/foerderung/skizzen/aktuell or the organization executing the project.
VDI/VDE Innovation + Technik GmbH
Rheinstraße 10 B
D-14513 Teltow
Phone: +49 33 28 4 35 1 01

Prolonging the Life of Microsystems

In many microsystems so-called "micro materials", which are powerful new materials, are applied. This allows cost-efficient manufacturing in high numbers. So far, it has been extremely difficult to estimate the long-term behaviour of such materials. No sufficiently exact constitutive equations and parameters that can be used in tools for design, simulations and tests are known. Therefore, useful estimations concerning the reliability of microsystems with very long system life spans (over several years) are not possible. This "safety loophole" has to be closed, because microsystems technology is increasingly being used in technology areas with high safety sensitivity.
Under the collaborative project LONGLIFE optical measuring systems and evaluation methods for the mechanic evaluation of material and network characteristics have been developed. The project, started in November 2001, was funded by the Federal Ministry of Education and Research with 1.35 million Euros within the framework of microsystems technology funding.
The six project partners will present their results to the public on April 21. The presentation is taking place at the fair SMT/HYBRID/PACKAGING 2005 in Nuremberg.

Further information at:
kuenzel@vdivde-it.de.

Workshop Helps German Companies to Enter Chinese Market

China is offering German microsystems technology (MST) companies great market opportunities. In the Far East there is a great interest mainly in advanced energy and home technology made in Germany. For the second time VDI/VDE Innovation und Technik GmbH is hosting a German-Chinese workshop on "Smart and Green Building" to facilitate market entry in China for small- and medium-sized companies from Germany. The main focus of the workshop, to be held in Quingdao on 18 and 19 April, will be on "Energy Efficiency". This event will be held under the auspices of the Federal Ministry of Education and Research (BMBF) and the Bavarian Ministry of Economy, Infrastructure, Transport and Technology. For some time now the BMBF and other ministries of the German federal states have maintained close contacts with administrative bodies (Ministry of Science and Technology, National Development and Reform Commission) and different provincial and municipal authorities in China. In talks, the Chinese partners showed great interest in modern energy and home technology from Germany.
One workshop on "Smart and Green Building" was held in the autumn of 2003 in Beijing, in which over 30 German companies from the fields of home and building technology and energy technology as well as over 100 decision-makers from the Federal Chinese organisations participated.
Given the positive response from the German companies as well as the Chinese side, contacts should be developed and the cooperation be continued. China is especially interested in modern technologies for power supply and energy conservation in residential and functional buildings. The workshop "Smart and Green Building - Energy Efficiency", to be held on 18 and 19 April, will offer German companies a platform to present innovative technologies in the areas of power supply and power management.

Further information at:
www.vdivde-it.de/smarthome.

Contact

GERMAN MST PROGRAMME News is provided to mstnews readers by the German Programme Microsystems (MST), managed by VDI/VDE-IT on behalf of the German Federal Ministry of Education and Research (BMBF).

Support Programme
Dr. Lars Heinze
VDI/VDE-IT
E-Mail: heinze@vdivde-it.de

Accompanying Measures
Alfons Botthof
VDI/VDE-IT
E-Mail: botthof@vdivde-it.de

German MST Programme News is compiled by:
Wiebke Ehret
VDI/VDE-IT
E-Mail: ehret@vdivde-it.de
Fax: +49 3328 435 281

First Networks Starting Now

Federal Minister Edelgard Bulmahn started the new "Microsystems" framework programme one year ago. Funding concentrates on important areas that may strengthen the innovative power of German industry.
The Federal Ministry of Education and Research (BMBF), in dialogue with the industrial and economic community, has identified six of those priorities. Over 70 million Euros will be allocated to them in the years ahead. More priorities will soon be identified.
The first six announcements of the BMBF have met with a positive response from companies and institutes. The first networks are starting their research and development work these days. 12 collaborative projects will be launched in the field of "measuring and testing technology". Three collaborative projects have been granted in the area of "micro process engineering"; more networks in micro process engineering are forthcoming.
Further information on previous and current announcements can be found at: www.mstonline.de/foerderung.

Events

MicroTechnology
Leading fair of applied microsystems and nano technologies at the Hanover Fair
11-15 April 2005
Hanover

SMT/Hybrid/Packaging
Specialized fair for system integration in microelectronics
19-21 April 2005
Nuremberg

New Definition of Micro, Small and Medium Sized Enterprises within the European Union
The European Commission has redefined the definition of SMEs. The new definition will apply from the 1st of January 2005 and shall ensure that the benefit for national and European support mechanisms will be provided exclusively for those enterprises "which have the characteristics of real SMEs".

Micro-enterprises are classified as enterprises with fewer than 10 employees and a threshold of 2 million for the turnover and the balance-sheet total.
Small enterprises have between 10 and 49 employees and a turnover threshold and balance-sheet total of max. 10 million .
Medium-sized enterprises have between 50 and 249 employees. The turnover threshold is 50 million and the threshold for the balance-sheet total 43 million .

The method of calculating the threshold is dependent on the type of enterprise. A definition of the three types (autonomous enterprise, enterprise with partners and enterprise linked to another enterprise) can be gathered from the following page:
http://europa.eu.int/scadplus/leg/en/lvb/n26026.htm

Competitive Call for an Additional Project Partner
The project "SHIFT", Smart High-Integration Flex Technologies currently active in the FP6 requires the participation of a new project partner to carry out LAP Large area panel processing tasks:
HiCOFlex (http://www.hightec.ch/index1.html) processes shall be transferred to existing 12" x 12" or 24" x 24" facilities. Expansion of LAP processes to the processing of polyimide, sputtering and photolithographic processing of conductors shall be developed. A defined set of process steps shall be carried out. Proposers should possess the infrastructure necessary.

Expected duration of participation in project: June 2005 to December 2007
Total Commission funding available is 170.000 for Research activities (estimated 320.000, to be supported by Commission funding up to 50%) and small additional Training and Consortium Management activities (to be supported by Commission funding up to 100%).
Date of close of call : March 16, 2005.

For further information please contact the project co-ordinator
IMEC/INTEC/TFCG
Jan Vanfleteren
e-mail :
Jan.Vanfleteren@elis.ugent.be

Technology Offers and Requests from the Network of Innovation Relay Centres
An Innovative Device for Determination of Soil Moisture
A small Israeli company has developed a new sensor and measuring device suitable for determination of soil moisture. The device is demanded in the agricultural field, particularly for determination of watering time. The company is looking for industrial partners interested in further development, commercialising the product and bringing it to the market.

Lightweight, Compact, Low-cost Position & Motion Sensors to Replace Resolvers, Synchros, etc.
A UK company has developed an accurate sensor technology to replace traditional position and motion measurement systems with applications in aerospace, machine tools, medical equipment, robotics, etc. Using simple printed circuit boards rather than the traditional wire windings - the resulting systems are light, compact and low-cost. Advantages include non-contact, long life, scalability, & flexibility (shape & size). The company is seeking industrial partners with volume applications.

Info at: kreibich@vdivde-it.de

IRC Future Match at CeBIT 2005
On the occasion of CeBIT 2005, the world's leading fair for information and communication technologies, the Information Technologies Thematic Group of the Innovation Relay Centre Network will organise the brokerage event IRC Future Match. It aims at helping exhibitors and visitors to the fair to find partners in Europe for technology-oriented partnerships. Companies, universities and research institutes in the ICT sector are invited to use this unique opportunity to establish new cross-border contacts for future collaboration.

Participation in the event is free of charge. Participants will only have to pay entrance to the fair. IRC Future Match 2005 takes place in hall 9, stand C21 within the future parc.

For further information, please contact:
Marion Laue, University of Hanover,
E-Mail: ml@tt.uni-hannover.de

Demo Day at the International Conference "Advanced Microsystems for Automotive Application 2005" in Berlin
The Innovation Relay Centre Northern Germany, represented by VDI/VDE-IT, invites all interested parties to attend their demonstration day of advanced Microsystems in automobiles. On the 16th of March, the day before the start of the 9th AMAA in Berlin, you will have the chance to test different pre-crash systems, pedestrian protection systems based on laser and radar, lane keeping and lane recognition warning systems. 10 cars from providers like IBEO, Conti, A.D.C., Aglaia, University of Ulm, Bosch, Daimler-Chrysler, Audi and Toyota will be at your disposal for testing.

The demonstration day starts at 10 a.m. and lasts until 6 p.m. Participation for attendees of the conference and for the press is free of charge.

Info at:
Jürgen Valldorf:
E-Mail: valldorf@vdivde-it.de or www.amaa.de
For press accommodation, please contact: Miriam Kreibich
E-Mail: kreibich@vdivde-it.de

A Fundamental Expansion of the MNT ERA-NET

After six month of searching and preparing we used the ERA-Net call in October to expand our MNT ERA-Net and add additional countries to the existing consortium.
The Added Value of the Extension to the original MNT ERA-NET project will be:
(i) doubling the geographical coverage, (ii) introducing new complementary MNT subjects, (iii) embracing new EU Member States and (iv) in all of these ways significantly expanding the scope for transitional cooperation between programmes and programme beneficiaries, i.e. the supported firms and research organisations.
The **geographical scope** of MNT ERA-NET will approximately double. The initial 8 participating countries will become 16. The number of participating programmes will increase from 8 to 21. A further 2 countries and 1 region will participate as "Associate Partners". This expanded geographical coverage will significantly increase the scope for transnational cooperation at both the programme and project (beneficiary) level.

The extension will also introduce **new MNT subjects** that strategically complement the thematic coverage of the original project. Particularly important in this regard are programmes with a strong focus on specifying and developing the process and product technologies that will be needed to support the widespread future application of MNT.
Half of the new partner countries are **new EU Member States**. Their participation will add multiple values to the project:

- Learning in programme design and management at a time when most of the new Member States are rethinking their R&D and technology policies
- Integration into a European programme cooperation framework, and consequently
- Accelerated development in the area of MNT as a result of enhanced learning and cooperation opportunities.

A first meeting with all partners took place in Vienna in mid-January. Results of this meeting will be published at www.mnt-era.net.
For more information:
reinhard.zeilinger@ffg.at.

MNT ERANET Faces Joint Activities among European National Programmes

The success of a European mobilisation reached through the extension requires the collaboration of the research and industrial community from an early stage. For this reason, the conclusions of the strategic activities among agencies (workpackage 2 of the project) have been to let the Research Community be the protagonist of the Joint Activities (WP3).
How can we integrate this bottom-up approach into the Eranet scheme? MNT-Eranet proposes a well-known mechanism: these are the Expressions of Interest (EoI).
The EoIs will provide the initial glue to link national and regional MNT programmes with research actors, safely and fast:

- Sizing of the clustering exercise is a powerful management tool for governments, providing key scenarios and parameters for long-term national commitments.
- Collaboration will be based on real projects, real sharing of efforts and rights between participants.
- Projects will be brought to their attention from year 2, but funding decisions may be taken a step later in order to invest on solid bases.
- Barriers will be faced and overcome against a practical context and timings.

However, a European joint initiative for EoI in 2005 in the field of micro and nano technologies requires a certain coaching from the respective agencies in order to tune expectations and work commitment from the research actors.

The challenge is twofold.
On one hand, preserving the proximity of companies and other research actors to the national or regional agency.

On the other, providing a progressive path that will act as a "stair of Europeanization" for them that will add new partners, contacts, opportunities, and will also require some new procedures.

To achieve this target, MNT-Eranet plans the WP3 of EoI in two stages:

- PHASE 1: LOCAL Workshops. To be held the first half of the year, announcing the Eranet plans to research actors and demanding short-term action of local EoIs to collect the best ideas and needs. They will be performed by each agency, with a crossed participation of at least 2 extra agencies, and with an open character for European partners. The result of the action will be the collection of these EoIs per agency.
- PHASE 2: EUROPEAN action. The target will be to coach a concentration process, enlarging the European cross participation of the best EoIs:
  - The MNT-ERANET web will be available for consultation and interaction of these EoIs, existing and new participants.
  - Each agency will present the rsum of opportunities and projects demanded by its country or region.
  - An internal workshop will assign responsibilities by topics or areas to agencies, and will provide a first management look at the basics of the collaboration.

  These events are planned for the second half of the year.

And the results of this WP3 will be:

- The launching of the first joint call of MNT projects in 2006.
- Crossed participation of international partners in local national calls in 2005.

Contact:
Peter Hahn, hahn@vdivde-it.de

The FP6 Marie Curie Research Training Network "Advanced Methods and Tools for Handling and Assembly in Microtechnology - ASSEMIC"

Introduction
Microhandling and microassembly are innovative research areas which impose challenging requirements. In order to prepare the new generation of researchers working in this field, special training schemes are needed, adapted to its multidisciplinary and intersectoral character.
The European Research and Training Network "Advanced Methods and Tools for Handling and Assembly in Microtechnology ASSEMIC" will address this need at the European scale, by providing advanced training for early-stage and experienced researchers in a 4-year collaborative research project with 14 participants from 10 different countries.
Micromanipulation techniques can include not only handling of microcomponents for assembly of MEMS, but also application fields and challenging tasks. Some examples are microsurgery, manipulation of biological material and microrobotics. One of the aims of this project is to explore and develop new methods, tools and applications for micromanipulation beyond the limits of traditional assembly techniques for microcomponents.

Learning by doing: ASSEMIC'S Research Dimension
The project is structured in several work-packages, defined to address the following main research objectives: ultra-precision positioning, innovative tools for handling and assembly, advanced control methods, application requisites and industrial production. A brief description of the workpackages' content is given below:
WP 1. Micropositioning: Positioning stages and elements with integrated sensors and feedback control, autonomous and mobile systems, microrobotics.
WP 2. Microhandling: Development and test of tools and methods for handling in different environments (normal room conditions, clean room, vacuum, fluids) and applications
WP 3. Microassembly: Innovative tools, special strategies and alternative approaches for efficient high precision and microassembly
WP 4. Automation for industrial production: Including production chains, quality assurance, test and characterization issues, etc.
WP 5. Know-how management: Technology transfer and dissemination

Table 1 PROJECT PARTNERS

1.	Institute of Sensor and Actuator Systems, Vienna University of Technology; Coordinator	ISAS	Austria
2.	Fondation Suisse pour la Recherche en Microtechnique	FSRM	Switzerland
3.	ARC Seibersdorf research GmbH	Seibersdorf research	Austria
4.	National Institute for Research and Development in Microtechnologies	IMT	Romania
5.	Politechnika Warszawska (Warsaw University of Technology)	PW (WUT)	Poland
6.	Instituto de Desenvolvimento de Novas Tecnologias	UNINOVA	Portugal
7.	University of Oldenburg	Uni-OL	Germany
8.	Fundacion Robotiker	Robotiker	Spain
9.	Foundation for Research and Technology – Hellas	FORTH	Greece
10.	Progenika Biopharma S.A.	Progenika	Spain
11.	Council for the Central Laboratory of the Research Councils - Rutherford Appleton Laboratory	CCLRC-RAL	United Kingdom
12.	Fraunhofer Gesellschaft zur Förderung der angewandten Forschung e.V.	FhG/ILT	Germany
13.	Scuola Superiore Sant'Anna	SSSA	Italy
14.	Nanoscale Technologies GmbH	Nascatec	Germany

Training Opportunities
Early-stage fellows participating in the ASSEMIC network will have the opportunity to receive training in a number of disciplines (artificial intelligence, material science, process control, vision systems, etc.) which are relevant to both MST and other areas such as information technologies and production engineering. In this way, the range of possible choices for their professional career will be broadened thanks to the opportunity of selecting from a wider variety of potential working areas and thus increasing their professional success expectancies.

ASSEMIC will provide a cohesive but flexible framework for the training and professional development of the fellows, especially in the early stages of their career. The network as a whole will provide a minimum of 574 person-months of Early Stage and Experienced Researchers, whose appointment will be financed by the contract. Measures intended to address training and transfer of knowledge will be divided into individual and network-based measures.

1) Individual measures will be:
- Basic training at the host institution: Training in available technologies and with specialized instruments, performance of experiments, basic skills such as preparation of presentations and redaction of technical reports and publications
- Secondments and visits to other network partners.
- Other individual training activities: Courses, tutorials, contact with and visits to industrial operations and SMEs, participation in external conferences, etc.

2) Network-based measures are as follows:
- Summer schools: Organized every year by FSRM exclusively for the network, the fellows will be trained by internal and external international experts with regard to microhandling and microassembly topics
- Training workshops
- Open seminars: Organized by the academic partners for students and interested early-stage researchers on topics related to microhandling and microassembly

Significant synergy effects are also expected with industry. The network ASSEMIC has an important industrial component. Links with industrial companies have already been established and are expected to be expanded through a series of dissemination and technology transfer activities.

Acknowledgement
This Project has been funded by the Commission of the European Community, Contract no MRTN-CT-2003-504826

Contact:
Werner.Brenner@TUWien.ac.at
Project Coordinator
www.assemic.net

MINAEAST-NET

Specific Support Action from FP 6 (2004-2006): MIcro- and NAnotechnologies going to EASTern Europe through NETworking" (MINAEAST-NET)

Coordinator: National Institute for Research and Development in Microtechnologies, Romania

On the MINAEAST-NET project web page (www.minaeast.net), a **Database for partner matching and expressions of interest for Call IST - 4 in FP 6** may be accessed. Also **Databases for Research centres** (either independent or autonomous from the scientific point of view, i.e. labs from universities and even institutes), **International projects** and **Specialists** are available at the same address. One may access databases related to thematic research fields, as defined in the on-going call in PC 6.

We are continuing the presentation of MINAEAST-NET partners.

Institute of Physical Electronics of Kaunas University of Technology (Lithuania) - IPE (http://www.fei.lt)
The Institute of Physical Electronics of the Kaunas University of Technology was founded in 1994 and in 2003 was reorganized into the Independent Institute, having the status of a University Institute. IPE takes part in the Eureka project, the science programme Gillibert, the Nordic Energy Research Program, and the NATO Science Programme - Cooperative Science and Technology.
IPE is one of the main organizers of the International Conference - School "Advanced materials and technologies", which takes place in Palanga, Lithuania, every year.
The main research activities of IPE include nanotechnology (thin films, surface engineering, nanostructures and nanomaterials) and optical document security.

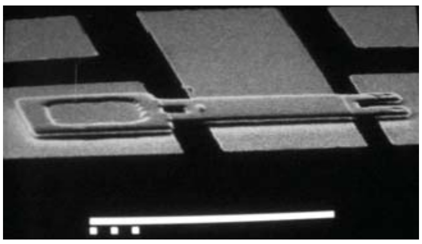

Figure 1: Microelectromechanical switch made at IPE

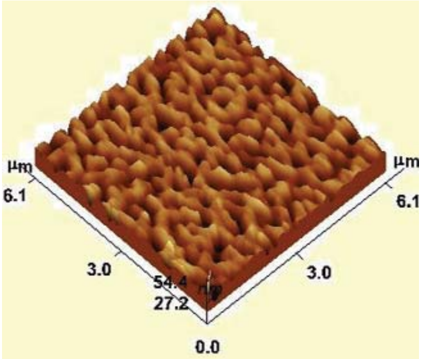

Figure 2: 25% PS - 75% PMMA nanostructured polymer bend on crystalline silicon (100) substrate -IPE project

Currently, IPE is employed in the development of polymeric nanocomposites, nano-imprint lithography, ion beam synthesis of carbon nanostructures, investigations of high-power micro-electromechanical switches.

Prof. Sigitas TAMULEVICIUS is the Director of the Institute of Physical Electronics of the Kaunas University of Technology, Lithuania. Prof. Tamulevicius has experience in international projects, he is an expert member of the Lithuanian Academy of Sciences, winner of the National Award of Science for 2001, member of the European Materials Research Society and FP5 and FP6 expert.

Sabanci University (Turkey) - Microelectronics Program (http://micro.sabanciuniv.edu)
The main principles of action for the Microelectronics Group at Sabanci University are the following: Assuming a leadership role in certain areas/technologies; Establishing and maintaining strong ties with industry; Maintaining strong collaboration with international partners; Disseminating expertise/educating industrial partners; Encouraging the development of commercial products/applications.

Research areas of the Microelectronics Group are:

" Microelectromechanical Systems: design, modelling, simulation and fabrication of silicon-based MEMS for different applications; acceleration sensors, pressure sensors, chemical sensors, ultrasonic transducers, infrared sensors, RF-MEMS.

" Very Large-Scale Integrated Circuits/Systems (VLSI) Design and Technology: Analyzing, designing, simulation and testing of semiconductor devices and VLSI for different applications; Analog, Digital, and Mixed Signal VLSI Circuits, Modelling and Simulation of Semiconductor Devices.

Associate Prof. Yasar GURBUZ (yasar@sabanciuniv.edu) is the coordinator of the Microelectronics Program at Sabanci University, Faculty of Engineering & Natural Sciences. He obtained his BSc. in Electrical Engineering at Erciyes University, Turkey, MSc. and PhD in Electrical Engineering at Vanderbilt University, TN, USA. Areas of Interest: Sensors and actuators, analogue ICs, MEMS, modelling and simulation of semiconductor devices, wide bandgap semiconductors.

MINAEAST-NET project

MIcro and NAnotechnologies going to EASTern Europe through NETworking
EU Contract no.: 510470 (SSA in FP 6)
Project coordinator:
National Institute for R&D in Microtechnologies (IMT-Bucharest)
Contact persons:
Project coordinator
Prof. Dan Dascalu (dascalu@imt.ro)
Project Vice-Coordinator
Dr. Carmen Moldovan (cmoldovan@imt.ro)
E-mail contact: net@imt.ro
Phone: +40 21 490 82 12 or +40 21 490 84 12
Fax: +40 21 490 82 38 or +40 21 490 85 82
Web page: www.minaeast.net
Special presentation of this project in MST News and MNT Bulletin (www.imt.ro/MNT)

Continuation from page 17

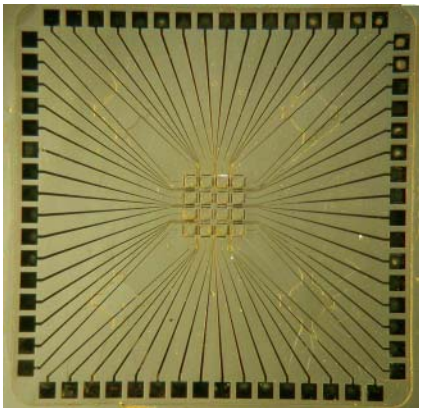

Figure 1: Microholder for single fibre produced in collaboration with IMM-Mainz

process. Each of the 4 electrodes surrounding one micro hole is connected to a high-voltage source and can be controlled individually to generate an attractive electrostatic force between the electrode and the grounded fibre. This will move the fibre towards the electrode.
A fibre tracking system is used to determine the actual fibre position in respect of its desired final position. By including this tracking system and the voltage generators into a closed loop alignment system, the fibre can be moved to its ideal position inside the hole. This ideal position can either be determined by the maximum measured output from a light source to which the fibre is to be aligned or the absolute distance from the other fibres in the fibre array. Once the fibres are in their respective desired position, UV light can be applied to selectively cure the glue in one micro hole. By applying the closed loop alignment throughout the hardening process, a movement of the fibre due to tensions induced by the glue can be minimised. This method reduces equipment and human labour requirements, and still remains the capability of moving fibres to their optimum position.

Conclusion
We have shown that the proposed method of electrostatically induced fibre actuation allows precise positioning of single mode optical fibres and the fabrication of two-dimensional fibre arrays.
An array for 4x4 fibres was produced and its functionality tested. Plans to increase the array size are currently under investigation.
A patent application for this technology is currently on its way [1] and inquiries by parties possibly interested in a potential collaboration are welcome to contact the main authors.

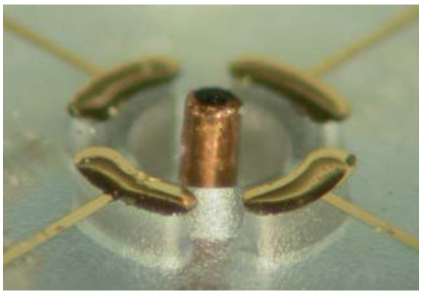

Figure 2: Microholder array for 4x4 fibres, 16 micro holes in the centre surrounded by 64 connection pads to contact each electrode individually.

Acknowledgements
The authors would like to acknowledge the financial support of the British Engineering and Physical Sciences Research Council (E.P.S.R.C.) through the Basic Technology Programme "A thousand micro emitters per square millimetre". Grant number: HWU 0240 R21 100006.

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Contact:
Dominik Weiland, Marc Desmulliez
MISEC, Heriot-Watt University, Edinburgh, EH14 4AS, United Kingdom
Phone: +44 131 451 3783
E-Mail: dw16@hw.ac.uk
M.Desmulliez@hw.ac.uk

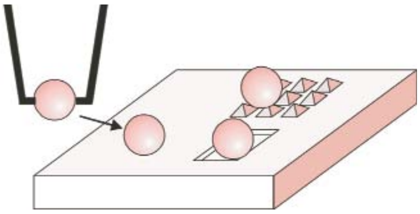
Adhesive Joints for MEMS Using Hotmelts

Stefan Böhm, Klaus Dilger, Elisabeth Stammen, Jürgen Hesselbach and Jan Wrege

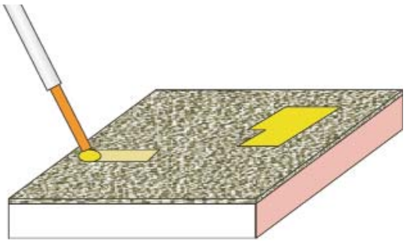
This paper presents an alternative adhesive system holding out the promise of joining very small parts as well as joining relatively big parts with high accuracy requirements. The main advantages are the possibility to apply small volumes, to pre-apply the adhesive with a temporally delayed joining procedure and extremely short set cycles. Therefore, using hotmelts can be a technologically and economically interesting alternative for the assembly and packaging of MEMS.

Introduction
The development of connection/joining techniques meeting requirements at the microscopic scale, in particular small joining geometry with high precision, is still a challenge. Beside technical requirements, economic aspects call for new techniques which are suitable for highly reliable automated processes.
In general adhesive bonding offers various advantages compared with other joining processes. Machine expenditure is quite small. The components that can be added are not exposed to a considerable thermal load during the joining process if the system is not warm-cured. In the cured condition the joint offers a high structural strength. Depending upon requirements, further functions can be integrated into the joint. Here mainly the possible electrical and thermal conductivity or isolation is required.

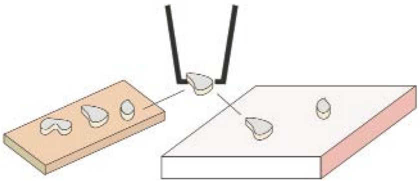
Adhesive Application
A central problem in MST production is applying the necessary very small adhesive quantities. An adhesive drop of 1 nl takes a diameter of 356 µm between two joining parts with a layer thickness of 10 µm [1]. That means that dosing equipment suited for micro bonding must be able to dose within a range from several hundred pico-litres to nano-litres, so that the geometrical dimensions of the joint do not become larger than the micro part. If the joint is to be in the dimension of e.g. only 10 µm (layer thickness adhesive likewise of 10 µm), the volume that can be dosed amounts to only 1 pl. By using viscous systems, currently a range from several picolitres is, however, the border of what is technically feasible related to the volume that can be dosed. I.e. by the default of the dosage system the min-



Discrete application of adhesive balls



Application of adhesive in powder form and punctual melting by the use of lasers



Application of adhesives in foil form

Figure 1: different methods of preapplying hotmelts

imum volume and minimum joining geometry are limited. In the literature the size is described within the range of a minimum of 100 µm and volumes in the range from 100 pl [2, 3, 4].

Alternative Adhesive Systems

Adhesives based on hotmelts have proved to be a promising alternative to viscous systems. An important advantage of hotmelts in relation to viscous adhesive systems is - particularly in microsystems engineering - the possibility of being able to pre-apply hotmelt systems. The joining procedure does not have to take place directly after applying the adhesive to the substrate; this can happen at any time later on. This is an important basis for the use of adhesive bonding in a batch process. The possibility to prepare multiple parts in advance and joining the parts simultaneously in a batch process is economically very interesting. The adhesive is only melted during the bonding process by a thermal impulse and moistens the surface of the other substrate. During suitable heat guidance hotmelts set very fast, i.e. a handling strength (usually the ultimate strength) is clearly achievable in less than one second as attempts have shown.
Hotmelts can be applied as adhesive ball, laminar in powder form or as foil, figure 1.

Production of suitable adhesive geometries

Commercially available hotmelt powder on a PA basis was particularised through filters or by sighting in graduated grain fractions between 2 µm and 63 µm. In bonding experiments these grain fractions were applied to the substrates as powder directly or processed before into adhesive balls or foils. Manufacturing balls took place on teflon in hot-air furnaces. For this, particles were applied isolated to teflon and warmed up in the furnace to fusing temperature. As a result of the surface tension of the adhesive and the small surface energy of teflon, a contact angle of approximate 180° between the adhesive and the teflon surface arose and the hotmelt particle became a ball, figure 2.

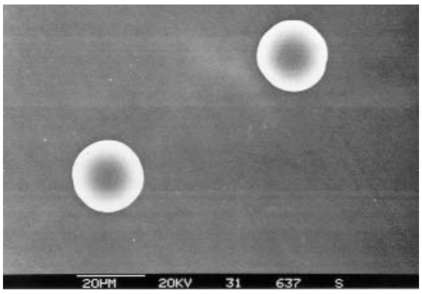


Figure 2: Hotmelt balls, diameters approx. 20 m

Manufacturing sequence in batch process

Bonding experiments were carried out in a clean room with the help of a commercial robot for micro assembly. After gripping from a magazine the adhesive (ball, foil) was positioned on a substrate and warmed to the melting temperature of the adhesive, figure 3.

Afterwards the robot placed the adherent on the pre-coated hot melt adhesive. The adhesively bonded adherents were removed from the plate and due to the decreasing temperature the hotmelts sets.

Conclusions

Since July 2004 our work has been partly supported by the German science foundation in the context of the Collaborative Research Center 516 "Design and Manufacturing of Active Micro Systems". Furthermore the transfer of initial research results started in co-operation with industrial partners. The results of the work were so convincing that a patent was applied for the procedure of micro bonding described above.

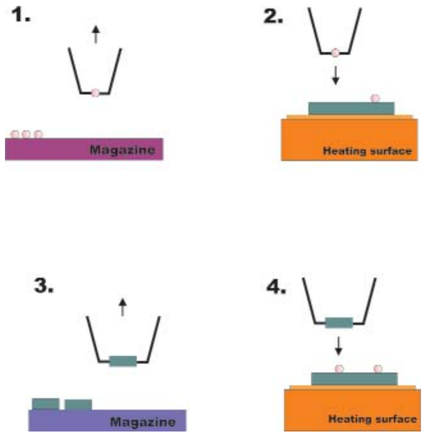


Figure 3: Manufacturing sequence of adhesive bonding in batch process

Acknowledgements

This work is partly supported by the German science foundation (Collaborative Research Center 516 "Design and Manufacturing of Active Micro Systems"). The authors would like to express their thanks.

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Contact

Stefan Böhm, Klaus Dilger,
Elisabeth Stammen
IFS - Institute of Joining and Welding
Technical University of Braunschweig
E-Mail: s.boehm@tu-bs.de

Jürgen Hesselbach, Jan Wrege
IWF - Institute of Machine Tools and Production Technology
Technical University of Braunschweig
E-Mail: j.wrege@tu-bs.de

High-Vacuum Wafer Bonding Technology

AuSi eutectic wafer bonding with integrated getter thin film for long-term stable high vacuum

Wolfgang Reinert

MEMS operation requirements

Microsensor packaging is one of the most important and challenging technology areas. In particular, hermetic packaging on wafer level is a key technology of many microelectromechanical systems (MEMS). The hermetic sealing protects them from harmful environmental influences, significantly increasing their reliability and lifetime. In addition some MEMS need a specific gas or pressure environment within the package to function as specified, see table 1. This article intends to give an overview on the relevant technological topics to produce hermetically sealed, micromachined devices on wafer level with controlled cavity pressures ranging from 10-4 mbar to 1000 mbar.

sensor/device type	vacuum level
accelerometer, switch	300 – 700 mbar
absolute pressure sensor	1-10 mbar
resonator (angular rate)	10^{-1} – 10^{-4} mbar
bolometer	< 10^{-4} mbar

Table 1: Required vacuum level for different MEMS.

Wafer-level processes are particularly interesting for MEMS packaging since they can reduce fabrication costs and open up possibilities for batch processing. Various wafer level sealing technologies may be used, including wafer bonding, cavity sealing by thin-film deposition, and reactive sealing. The present article focuses on eutectic AuSi wafer bonding to produce low-cost and long-term reliable hermetic MEMS packages.

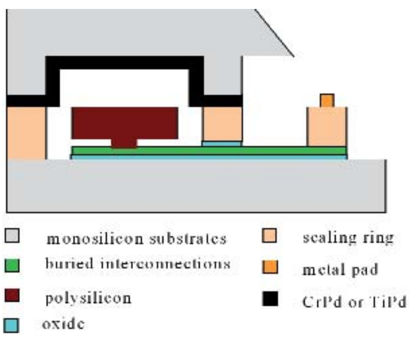

Figure 1: MEMS construction with getter.

Figure 1 shows the main functional elements of a surface micromachined MEMS device with integrated getter film in the cap.

Beside maintaining vacuum, encapsulation on wafer level solves the problem of device protection during wafer dicing operation. The improved robustness of capped devices allows MEMS devices to be handled in existing standard semiconductor backend processes.

AuSi eutectic bonding

AuSi eutectic bonding is a technology using eutectic formation at 363°C between a silicon wafer and gold deposited on another silicon substrate. The bond temperature used is in the range of 380-400°C. This is compatible with Al device metallisations. Due to the liquid melt formed, this technology tolerates wafer topography coming from previous processing operations. The technology is also compatible with extended outgassing cycles and the activation requirements in case a deposited getter layer is present in the device cavity. Compared to glass frit bonding, AuSi eutectic bonding does not outgas during the wafer bonding cycle, and requires only very small bond frame widths, typically in the range of 60 - 100 µm. This increases throughput, which is a major parameter for low-cost production.

Getter technology

The use of Non Evaporable Getter (NEG) material (Zr based alloy) is required to ensure suitable vacuum (total pressure under 1x10-3 mbar) and long-term stability in MEMS devices. NEG can chemically sorb all active gases, including H_2O, CO, CO_2, O_2, N_2 and H_2. The main constraints imposed by device design and process are the compatibility of the getter with the fabrication process, the thickness of the getter film and an activation temperature compatible with the bonding process. Besides this, SAES Getters laboratories offers a patterned deposition of the getter material on the cap wafer by a proprietary technology: PaGeWafer .

The thick getter film can be selectively placed into the cavities without affecting the lateral regions of the wafer where the hermetic sealing is to be performed. The typical pattern lateral dimensions are in the millimetre range, while the getter film can be placed in the cavities with any depths, ranging from a few microns to hundreds of microns. Figure 2 shows the precise deposition of the getter material inside the cavities.

The getter film consists of a special Zr alloy, whose composition is optimized to maximize sorption performance or to maximize performance in specific sealing or bonding processes.

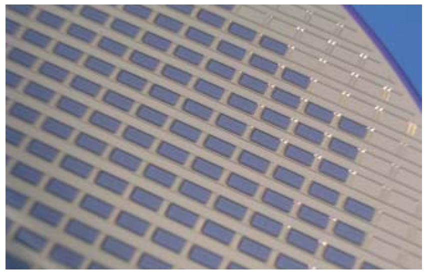

Figure 2: PaGeWafer , cap wafer with deposited getter layers.

Cap wafer cleaning

Wafer cleaning of the cap wafer is usually required before bonding to remove organics from the gold bond frames. The getter layer must tolerate the cleaning chemistries. It has been discovered that a caustic chemical treatment of the getter film both cleans the film and enhances its performance without measurable degradation of its structural integrity. For example, caustic chemical treatment SC1 with NH40H/H202/H20 and SC2 with HCl/H202/H20 did not affect the morphology and the sorption capacities of the getter film and significantly increased the sorption capacity, measured under ASTM standard F 798-82.

The getter film at wafer level can also withstand treatment with a highly aggressive HNO3 process up to 65% @120°C. The full compatibility of the getter film towards both temperature and chemical treatment with regard to the activation and capacity of the getter film is demonstrated. Typical absorption speed and absorption capacity of the patterned getter film per unit area at room temperature for hydrogen and carbon monoxide are reported in Figure 3.

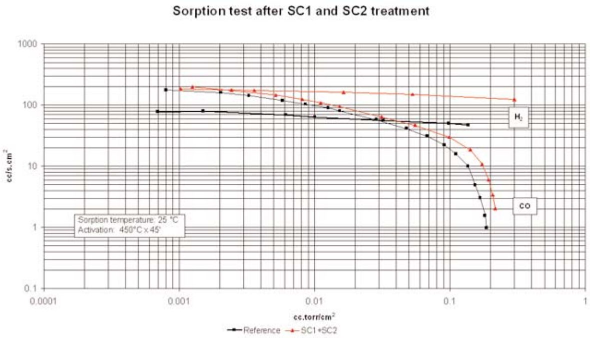

Figure 3: Sorption characteristics for H_2 and CO per cm^2 of getter film after SC-1 and SC-2 treatment

Getter activation

The getter film is supplied in a stable, passivated form to protect the getter and to ensure that it performs as specified. The PaGeWafer can be safely handled in clean room air. Once the getter film is in a vacuum or noble gas environment, it needs to be activated. Activation is achieved by applying thermal energy to the getter to diffuse the passivation layer into the bulk, rendering the surface of the grains chemically active and ready to pump contaminants out of the MEMS package.

Getter film activation can be achieved through three main scenarios:

1. The classic scenario is activation of the getter as part of the wafer bonding process. The temperatures under vacuum reached in the bonding process will simultaneous activate the getter as well as bond the device and cap wafers. In this case, the getter film will also improve process conditions by achieving a higher vacuum between the two wafers in the cavity.
2. The second scenario is to apply heat to the cap wafer after bonding
3. The third scenario is first to heat the cap wafer under vacuum and then align the wafers and bond them.

Backfilling

To realize a defined gas damping for resonating sensors, a gas-filling procedure has to be established. Only inert gases or gases that do not consume the getter or alter the getter sorption performance may be backfilled in the device cavities. Most often Argon is selected because of good damping characteristics and low out diffusion. The backfill operation is typically one step in the wafer bond cycle. Figure 4 shows the dependency of the device Q-factor on cavity pressure for a typical BOSCH type yaw rate sensor. The cavity pressure can be tuned to any value between 10-4 mbar and 1000 mbar; even overpressure is possible depending on the wafer bonder infrastructure.

Hermeticity testing

The pressure inside of the vacuum encapsulated devices depends on the outgassing of the inner surfaces, the leakage rate through fine leaks and permeation through the walls, see figure 5. The outgassing depends mainly on the fabrication process of cap and device wafer, which has to be optimized.

Fine leaks arise from imperfect bonding or crack initiation. The pressure change per unit time in a device can be expressed as

$$dP/dt \quad L / V$$

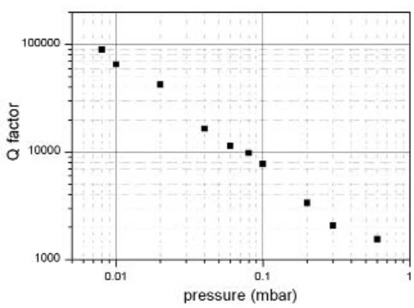

Figure 4: Dependency of the Q-factor vs cavity pressure [N2] for a typical surface micromachined renonator.

where L is the leak rate and V the cavity volume of the device. Typical cavity volumes range from 0.1 mm^3 to around 5 mm^3.

Since fine leaks may always be present a leak test is necessary to guarantee a leakage rate that is small enough to be compensated by the getter. This leak rate may be called the critical leak rate, as it defines the devices within the statistical cavity pressure distribution that fail the first after the guaranteed lifetime is fulfilled. As an example: for a device with a life time requirement of 15 years and internal vacuum requirement better than 0.1 mbar and a getter capacity of approximately 1.7x10-5 mbar l per cavity the maximum tolerable leakage rate for a cavity volume of 0.26 mm^3 is 3.6x10 14 mbar l/s. Due to high Helium permeation in Si and silica, a long-term stable, high vacuum better than 10-4 mbar is very difficult to achieve.

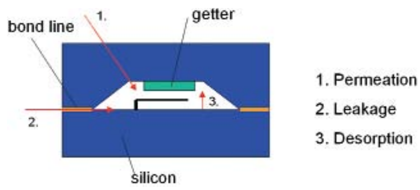

Figure 5: Effects degrading cavity pressure.

Fraunhofer ISIT has developed an in-line, ultra-fine leak test on wafer level to determine the leak rate of every single resonating device before shipping out. This ultra-fine leak test overcomes the limitations of He and Kr85 fine leak test and is compatible with integrated getter and unaffected by the typically very small cavity volumes. Critical leak rates down to 10-16 mbar l/s can be determined without interference between neighbouring devices.

Conclusions

In respect of process yield, a eutectic wafer bonding technology with a liquid phase of > 1 µm thickness will considerably improve the tolerance of the bonding process in terms of surface topography and bond frame imperfections (scratches, particles). A cap wafer cleaning procedure with SC1 and SC2 was found to be very effective to achieve good bond homogeneity, and at the same time even improves the getter sorption capacity. It is not recommended to apply Ar ion milling or backsputtering to any of the used wafers. PaGeWafer can assure high performance MEMS sensors, thus considerably increasing the device lifetime by maintaining the Q-factor of the device while relaxing the stringent requirements for minimum leak rates.

Acknowledgements

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Please visit also: www.vabond.com

AP Plasma Activation for MEMS Wafer Direct Bonding

Markus Gabriel

Within the five basic processes of wafer bonding (anodic, thermo-compression, direct, eutectic and adhesive) many variations are applied in MEMS, micro-opto-electro-mechanical systems (MOEMS) and advanced wafer-level packaging. The choice of a bonding method depends on the initial substrates and the final application. New developments enable direct wafer bonding with subsequent annealing at moderate temperatures extending the potential for new applications, not compatible with other bonding processes.

Why LT wafer direct bonding?
Direct wafer bonding is an established technology for many applications in MEMS and substrate engineering. It is also the only one front-end compatible wafer bonding process with high volume capabilities. The standard process consists of a) cleaning, b) room temperature bonding and c) high temperature annealing. For cleaning DI, water and megasonic power are utilized just before the bonding process. Both process steps can be performed in one tool without additional handling within about 2-3 min. The annealing step, typically a batch process, is required to increase the bond strength withstanding the following processes like thinning (mechanical, chemical) and dicing. The very high annealing temperatures (~1100°C) in the annealing processes of directly bonded wafers however created some technological problems and therefore restrictions in applications in the past. To overcome the problem a surface activation before bonding is required. SUSS MicroTec`s nanoPREP technology is the new approach for effective surface activation of materials used in MEMS and the Semi Industry.

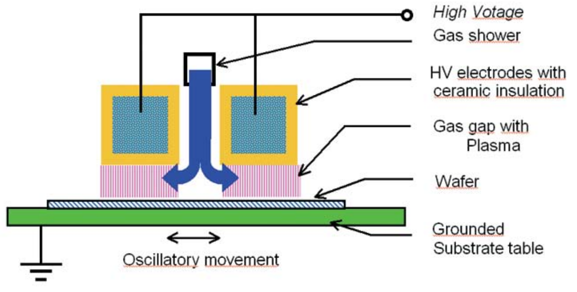

Figure 1: A principle of an ambient pressure plasma system

Features of ambient pressure plasma
nanoPREP is an ambient pressure plasma process, developed in cooperation with FhG and MPI in Germany. The technology is based on the dielectric barrier discharge (DBD) principle, widely used in other industries and optimised for the treatment of semiconductor wafers. The active plasma is limited to a long but narrow area (Fig.1). A uniform treatment is achieved by scanning of the substrate. Control of the process gas, generator power and some other parameters guarantee a stable process. The generator delivers an AC voltage in the range of 20kHz.

The nanoPREP technology was realised in a commercially available tool: the NP200. The NP200 is a stand-alone system with manual loading. Integrated modules in a fully automated bond cluster were recently installed in field. All wafer sizes up to 300mm as well small chips can be processed.

With respect to the CoO, the nanoPREP technology has some benefits compared with low-pressure plasma systems. Very short time of down to 10 seconds for one scanning path process characterises the process. The complexity of the technology is minor, the process window wider. The investment costs are minor due to the lack of vacuum technology.

Effects of Activation
The surface properties are modified by the process in the range of a few Angstrom. Typical process gasses are N_2 or O_2 mixtures resulting a very hydrophilic surface (Fig.2). AFM measurements showed reduced RMS roughness after the treatment. No additional particle contamination was measured at appropriate parameter settings. Results of a metallic trace analysis match the SEMI specifications.

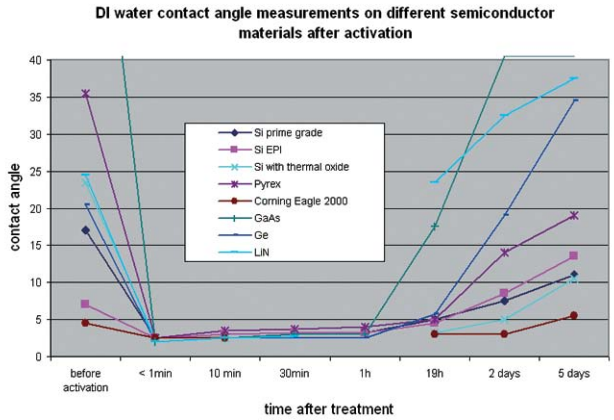

Figure 2: Contact angle measurements of plasma treated wafers

The bond energy and yield are the most important criteria of wafer bonding evaluation.
A yield up to 100% of samples with test structures (50-500µ) was analysed by Fraunhofer. Bond energies up to the bulk material fracture limit can be achieved.

Challenges
The versatility of material requires the development and optimisation of the process to the applications. An interesting field of investigation is the SiO_2 deposition with nanoPREP. Direct bonding of Pyrex with Si was demonstrated as a real alternative for Anodic Bonding and needs to be proven in terms of yield and hermetic seal properties.

Contact
Markus Gabriel
m.gabriel@suss.de
www.suss.de

Advances in Aligned Wafer Bonding for 3D Interconnect

Thorsten Matthias and Paul Lindner

The International Technology Roadmap for Semiconductors predicts continuing development towards smaller geometries, higher frequencies and larger chip sizes. However it is pointed out that the traditional path of downscaling together with material innovation is no long-term solution for the performance requirements due to interconnect problems [1].
3D Interconnects enabling chip stacking offers an approach to vertically connect two integrated circuits for the purpose of shortening the wiring distance between them. This technology enables increasing levels of integration, which enhances performance and functionality, reduces signal time delay and extends bandwidth while reducing cost, size, weight and power consumption [2].
Aligned wafer bonding is a wafer-to-wafer 3D interconnect technology. Two fully processed wafers are aligned and bonded face-to-face. The top wafer gets thinned down to a thickness of a few microns or below, and high aspect ratio vias are etched through the backside of the thinned wafer to provide vertical electrical connections between the two wafers. The electrical connections have a length of only a few microns, which enhances the performance of the devices dramatically. This process sequence can be repeated several times (Fig.1).
Heterogeneous subsystems like CMOS and memory, mixed signal or bipolar (RF) devices sometimes require highly different, worst-case non-compatible, processing steps. Aligned wafer bonding allows processing of the different functional subsystems on separate wafers, thereby reducing the complexity and number of process steps greatly.
3D interconnect applications require wafer-to-wafer alignment accuracy in the low-micron or sub-micron range. The established alignment methods developed for MEMS production have very limited usability for 3D integration. High concentrations of dopants and metal layers limit the usability of IR alignment. Backside alignment keys cannot be used for CMOS applications, as the wafers are generally single-side processed.

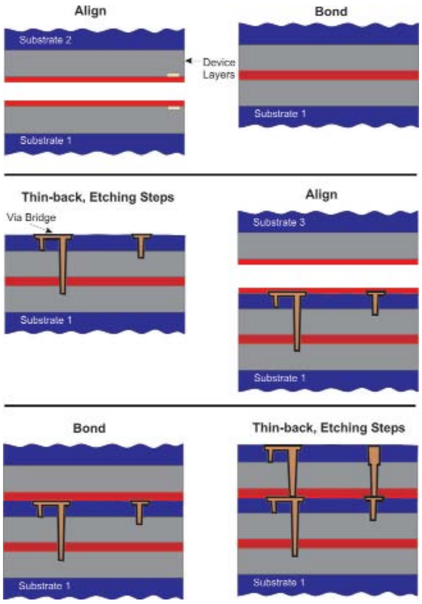

Figure 1: 3D Interconnects through aligned wafer bonding

A new method, the SmartView® face-to-face alignment, allows alignment keys of both wafers within the bond interface. The SmartView® system employs two dual microscopes with identical optical axes. One microscope is placed above and the other below the wafer stack. First the microscopes are centered on the keys of the bottom wafer, then the top wafer is positioned according to the microscope position (Fig.2).

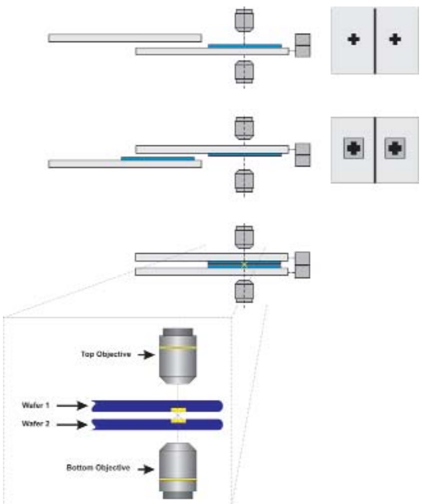

Figure 2: SmartView® alignment principle

Wafer alignment is accomplished using encoded stage motors allowing X and Y movements in increments of 0.1 µm steps.
Wafer bonding for 3D integration is compatible with conventional back-end-of-line processes allowing subsequent back thinning, inter-wafer interconnections etching, dicing and packaging. The best-investigated wafer bonding techniques for 3D interconnect applications are Cu-Cu thermocompression bonding and adhesive bonding. The advantage of the Cu bonding technique is that the bond pads directly connect the two devices electrically and thermally. Thereby the process steps for via etching and connecting of the two device layers are avoided. The advantage of adhesive bonding is that the required specifications for wafer surface properties and cleanliness are relaxed as any particulates are embedded in the adhesive layer.
Modern integrated wafer alignment and bonding systems allow automatic cassette-to-cassette operation fulfilling the requirements for high volume manufacturing (Fig.3).

Figure 3: GEMINI® fully automated production bond system with SmartView® alignment and multiple bond chambers

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Contact:

Thorsten Matthias, Paul Lindner
EV Group, DI Erich Thallner Strasse 1, A-4780 Schärding
E-Mail: T.Matthias@EVGroup.com
www.EVGroup.com

Back-End and Assembly Production of Cost Sensitive Microsystems

Christian Ossmann

Today the "classical" electronic and sensor-related manufacturing process steps are moving closer together. New technologies such as "System in Package - SiP" or "Molded Interconnect Devices - MID" combine a variation of different technologies like screen printing, die bonding and / or surface mount technologies. The demands for cost reduction and the increase in the fill factor and functionality of the packages drive this movement.
It is well-known that the package of a MEMS device creates about 70 to 80% of total production cost today. The technologies mentioned earlier for the first time allow a significant reduction in the costs of MEMS packaging and thus create the possibility for a real step into cost-optimized mass production of Microsystems. The latest example is the mass production of the micro cameras for mobile telecommunication applications. Today the total costs of such cameras amount to approximately two Euros. New technologies have the potential to reduce cost by factors. To understand this statement, the process flow of typical cell phone cameras in production today is described (Figure 1). One can realize that there are a variety of technologies to be adjusted to each other to ensure an optimized production.
In a first step the CMOS sensor and Asics will be assembled. Therefore one or more chips are bonded into a cavity (substrate). Next, using a wire bonder, the electrical connections are created. Finally an IR absorbing glass has to be attached onto the cavity for contrast enhancement and contamination protection. This package is called a cavity CMOS sensor.

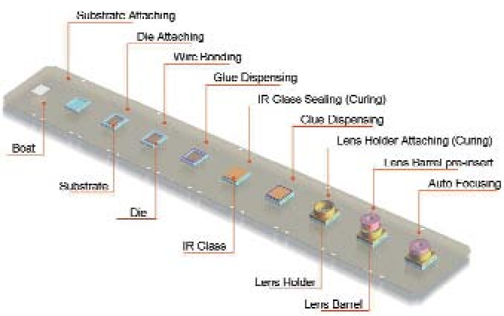

Figure 1: Process flow towards an assembled micro camera

Up to this step the whole process is extremely sensitive to contamination by particles. One can easily imagine that even smallest particles inside the package will cause malfunctioning of the whole sensor module.
To address the contamination problem, equipment manufacturers create a clean environment in the process area. Since this approach covers only part of the problem, the contamination of the chip prior to chip handling and the chip handling itself are extremely critical. Thus, these types of machines need an actively controlled air flow through the whole machine. Alphasem, the market and technology leader for CMOS sensor bonding, additionally offers the unique approach of vertical handling of wafers instead of typical horizontal handling, which is used today. Thus, even the few present particles have almost no chance to hit on the sensor surface.
In terms of cost-optimized production, one can imagine that the combination of the CMOS chip bonding and IR glass attachment on one hand and wire bonding, as a complete different technology, on the other hand are extremely critical. Successful fab designs in the Asian Pacific area in most cases follow a strategy of creating technology islands. Thereby process steps are clustered and optimized. Alternative solutions, such as inline production, where all machines are arranged in one line, assembling the complete product fully automatically, in most cases exhibit significant problems in yield and availability. This is mainly due to the complexity of linking totally different equipment together. Not mentioning the difficulties of the clean room layout, since the cavity assembly typically is in class 100 condition, while the following process steps will take place in class 1,000 to 10,000. The following assembly steps are significantly different from CMOS sensor assembly. Here a combination of surface mount and fine mechanical assembly technology is required (Figure 3).
Typically this part of assembly

Figure 2: Alphasem "Swissline"

starts with an attachment of the lens holder onto the CMOS sensor. If not already assembled in a next step, the lens barrel will be screwed into the lens holder. Finally the optics has to be adjusted and fixed. Since the production of the low-cost modules is almost completely located in the Asian Pacific area, the automated equipment has to offer a significant cost and performance advantage over manual assembly.
Thus, today in most cases dedicated assembly equipment such as Alphasem's Flexline (Figure 4) is installed. Common to these platforms are high flexibility and moderate investment costs. The flexibility is defined by two parameters. On the one hand, by the possibility of the integration of third-party tooling and, on the other hand, by the possibility of being re configurable during a given product change. Thus it is important for this type of equipment to offer standardized interfaces for an easy and fast integration of third-party tooling. An example of such a customized tool, a gripper for pre-assembled lens holder handling is shown in Figure 5. Having such cells in operations it is easy to adapt a variety of process steps to meet the needed throughput of the assembly line. It is therefore possible to start with one cell for R&D and split the process steps over a num-

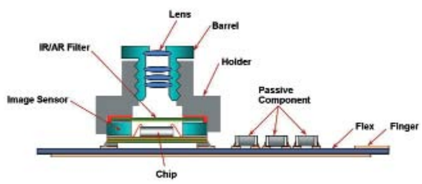

Figure 3: Cross Section of Micro Camera on Flex

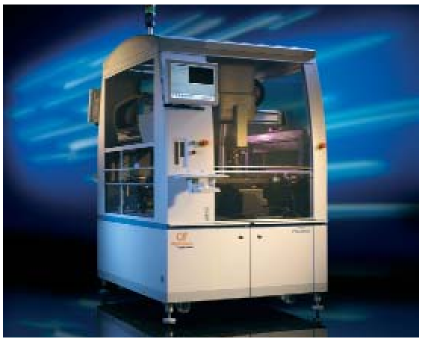

Figure 4: Assembly Cell "Flexline"

ber of cells as soon as the volume increases.

Today the final steps of tuning the camera by calibrating the position of the lens barrel and fixing it at the best position are mostly manual or semi-automated operations. The drawback to fully automated solutions in the cell phone camera assembly is the level of salaries in Asia, mainly China.

Figure 5: Lens gripper (Schunk)

Since the manual workspace for such an operation is available at low cost, highly flexible for new products and the throughput created by the operators in the range of 100 to 150 pieces per hour, dedicated equipment can hardly compete. While increasing the quality of the optics and increasing demands on adjustment and testing, automated equipment will play a significant role in the future. Thus, the needed tools are under development and will be released into the market soon.

The process steps to assemble a micro camera described so far are close to the "classical" assembly of cameras. This technology is limited in terms of the achievement of cost improvement and fill factor. As a result, a number of groups worldwide are working on concepts for new assembly methods, closer to MEMS technologies. One approach is the MID technology - Molded Interconnect Devices (Figure 6).

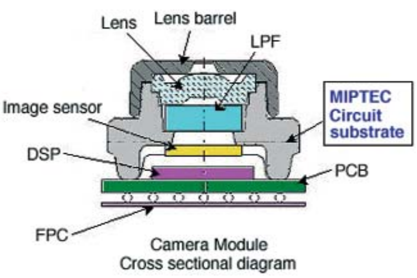

Figure 6: MID Camera Module (Image is courtesy of Matsushita)

The goal is to provide a pre-manufactured package including all optical, electrical and mechanical features. This can be achieved by a combination of molding and deposition techniques. Using a standard die bonder, the CMOS sensor chip will be bonded on top of the electrical interconnects by flip chip technology. As a result, an easy-to-handle SMD type device has been created. Especially if one considers the tolerance budget, this approach is very promising for low-cost production.

Contact:
Christian Ossmann
Business Unit Manager Microsystems
Alphasem AG
Phone: +41 71 637 6373
E-Mail: Ossmann.C@Alphasem.com

Micro- and Nanotechnologies for Advanced Packaging

Karl-F. Becker

Microelectronics miniaturization has evolved according to Moore's law since the mid-sixties and over the years it has always been possible to follow its prediction without meeting fundamental technological limits. This might be in question for future applications, where the SIA roadmap indicates a red brick wall for the further development of microelectronics without fundamentally new approaches.

These new approaches towards microelectronics as single atom and CNT based transistors all benefit from nano-science and technology to target a maximum integration on chip level, leading to increased interconnect density and thus to a miniaturization of the individual contact. Parallel to this miniaturization of interconnects, the development of an adapted packaging technology is necessary to provide reliable interconnects from the nano- and microscale to the meso-world, where microsystems are used.

Roadmap Predictions for Packaging Technologies

The demands towards the packaging of advanced micro- and nano-systems are described in the 2004 update of ITRS for Assembly and Packaging, where experts identify the demands for system packaging for the next 14 years. [1] The recent update focuses packaging needs on three main topics:

Difficult challenges - Closing the gap between continuously decreasing chip pitch and stagnating package pitch, Packaging of MEMS, of nanostructured systems and of emerging technology devices.

Material challenges - Development of materials stable at high temperature and matching lead-free requirements. Development of dielectrics for embedded passive and active components

Packaging cost challenges - Development of cost effective packaging technologies that cope with increasing material cost and matured packages.

Advanced Packages, possibly better described as System In Package (SiP), integrate more than one die and optionally sensor functionality, bus or RF interfaces, passive components and geometrical features as media ducts and alignment structures for additional component attach. This allows sharing packaging cost with a larger amount of functionality compared to single chip devices. As outer package geometry often Area Array configuration is selected, leading to BGA, CSP or QFN package types.

According to ITRS, the following specifications will be true for the next generations of System in Package. SiPs will contain both embedded passives & embedded actives; there will be up to 5 dies in a stack and up to 6 dies in a package. From 2010 the I/O count for digital signals is estimated to be 2000, for RF 200. Small BGAs / CSPs in their various geometries will be the dominating package type, with pitches from 200 µm in 2006 down to 150 µm in 2012 and 100 µm in 2016. Moisture sensitivity level (MSL) for these packages will decrease from today's MSL of 3 to MSL 1 from 2010.

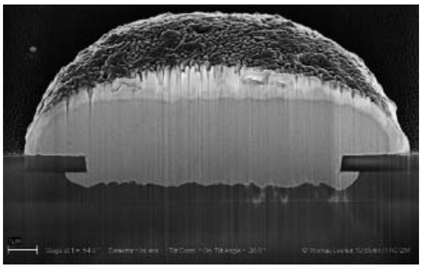

Figure 1: Interconnects for Nano Systems - Bump with 10 µm width for low profile, fine pitch interconnects

For short-term applications in system packaging, the specific task is to close the gap between chip and substrate, implicating research on:

- Low-cost embedded passives: R L C
- Material and process solutions for operation temperatures up to 200°C
- Interconnect density scaled to silicon (silicon I/O density is increasing faster than the package substrate technology)
- Production techniques adapted to silicon like production and process technologies after 2005

As possibilities are limited to reach the ambitious technological and economic goals of the packaging roadmaps with existing technologies, it is assumed that future progress will be driven by further developments in micro- and nanotechnology.

Technological approaches towards Micro/Nano Integration

System integration at the micro- and nanoscale includes various technological options that need to be addressed in the future, sometimes introducing radically new process flows.

System Assembly

Maximum system optimization can be achieved by merging the technological areas of components and infrastructure, i.e. housing, leads, alignment structures, as function integration is the key for maximum miniaturization. Micro and nano systems of the future will contain subsystems and components that com-prise functional structures at the nano-scale with a need to interconnect these to a micro scale. An example for a state-of-the-art contact element in the lower µscale is depicted in figure 1. As an example, this 10 µm wide bump can be used for ultrathin interconnects for miniaturized micro systems. Future systems will drive miniaturization further, introducing 3D integration at the submicron scale, yielding e-grain like structures [2].

Building Blocks - Components

Conventional system assembly is using

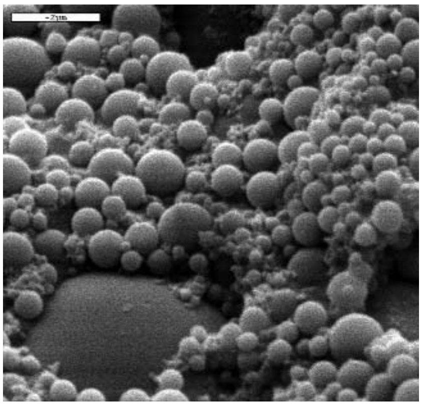

Figure 2: Nano-enhanced encapsulant - Nanoscale filler particles help to tailor materials CTE

discrete components that are combined by pick and place, yielding a functional system. Targeting miniaturized nano systems it is necessary to maximize system size reduction by function integration. For this approach, a precise definition of components and interfaces is crucial, typical components are:

- µProcessors
- Power Supply
- Actuators
- Passive Devices
- Sensors
- Displays

Depending on future developments, it is possible to integrate the realization of the above-mentioned components away from dedicated fabrication sites into the back-end area, e.g. by simultaneously generating printed leads and integrated resistors. Near-term realization of this integration will be possible especially for passive devices, sensors and displays taking benefit of progress in polymer electronics with the functionality defined at the nano scale [3].

Building Blocks - Infrastructure

For system integration using nano scale functionality, it is necessary to provide interconnection and protection for the components used. These infrastructural components include electrical, optical and RF interconnects on the one hand; on the other hand the realization of substrates and conductive structures, of external interfaces (alignment structures, media ducts, optical interfaces) and of protection/encapsulation for the system generated. Today's state of the art includes the use of materials with integrated nano functionality (see Fig. 2) [4] and for chip interconnects the use of carbon nano tubes [5] or nano structured interfaces, as the Au based nano-lawn for low-temperature interconnects for example [6].

Integration Technology - Manufacturing

With components and subsystems available, the challenge of micro and nano system manufacturing is to establish the most efficient process chain of placement, joining, coating, structuring and interconnection. Possible manufacturing technologies for miniaturized systems are largely dependent on the geometry of the components/subsystems. As a near-term strategy to integrate discrete components in the µm scale, the following means might be applicable:

- Parallel Pick and Place, using e.g. advanced AFM tools as IBM's Millipede concept
- Self-Assembly using liquid, magnetic, electrostatic, geometric means or a combination thereof

For the realization of infrastructural elements, most likely the following means might be adapted to the needs of nano system assembly:

- CVD/PVD
- Liquid Coating as dipping, spray coating, spin coating and jetting
- Lithography
- Galvanic Material Deposition
- Field assisted structuring especially utilizing non-linear behavior under overlayed electrical, optical or acoustical fields

For the long-term estimation of the integration of nano scale functional building blocks into system assembly process flow, it is of vital importance to know the nano technological manufacturing technology. One option are scenarios comparable to today's front-end manufacturing with maximum demands towards the environment. Processing is conducted in a dry atmosphere, typically using PVD and CVD processes. Another option, at least for selected process steps, is processing in liquids; this has been demonstrated e.g. by Whitesides [6]. Using such carrier liquids is reliably preventing electrostatic charging of nano particles and also prevents inhalation of potentially hazardous particles. Potential carriers are aqueous solutions or organic solvents; system integration might take place in micro reactors, where components form systems by self-assembly processes.

Analytics and Modeling

With further miniaturization the analysis of systems at the nanoscale will gain more and more importance, especially cost-effective analytical solutions for manufacturing process control. Know-how on interface analytics is needed for the successful realization of reliable nano systems. For modeling, interfacial behavior as well as a detailed knowledge of the behavior of nano-enhanced materials are crucial for an optimized descrip-tion of micro/nano systems.

Design of Micro/Nano-Systems

Design tools available for system generation are adapted to the meso- and microscale, taking into account manufacturability with state-of-the-art equipment. For nanoscale systems, these approaches have not yet been adapted. The fundamentally new working principles of nano technology do not allow simple scaling of existing technologies; research will be needed to integrate e.g. quantum effects into system design.

Conclusion

A large contribution of micro and nano technology is seen for the further evolution of packaging technology; actually, most of the obstacles predicted by state-of-the-art roadmaps for packaging technology can only be solved using nano technological means. Amongst all semiconductor-based research, the important contribution of packaging to a successful system in package realization should not be underestimated.

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[4] M. Werner, B. Michel, H.-J. Fecht and N. Meyendorf, Applications and Challenges of Nano- and Micromaterials for Microsystems, mst-news 04/04, pp. 5-9

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[6] S. Fiedler, Nano-Bio-Packaging - Ansätze, Chancen und Trends Teil I . P.L.U.S. (Produktion von Leiterplatten und Systemen) 2004 / 8 1169-1178; Teil II Ibid. 1362-1368

Contact:

Karl-F. Becker
Fraunhofer IZM Berlin
Phone: +49 30 464 03 242
Fax: +49 30 464 03 254
E-Mail: becker@izm.fhg.de

MicroTechnology at 2005 Hanover Fair

MicroTechnology will open its gates in Hanover on April 11-15 (09:00-18:00) this year (hall 14/15), in conjunction with 10 other trade fairs, covering sectors like factory and industrial automation, research and technology, industrial subcontracting and services, energy, and many more.
MicroTechnology is the No. 1 trade fair for all aspects of microsystems technology, micro-assembly and micro-optics, as well as the fast-growing discipline of nanotechnology in Europe. Underlining the message "small is beautiful", approx. 250 exhibitors will present innovations with multiple applications and solutions ready for production.

SchauPlatz Nano

After having been presented for the first time during the trade fair MATERIALICA 2004 in Munich, the showcase Nano will be a new attraction of MicroTechnology. Additionally the "nanoTruck" of the German Federal Ministry of Education and Research (BMBF) will be situated directly outside the hall. Visitors of the fair have the opportunity to learn more about applications and solutions in the area of nanotechnology, presented by a number of exhibitors from industry and research within one focused area. Contacts can be made and intensified in the integrated showcase-lounge. More information on the showcase Nano can be found at www.schauplatz.de/nanoworld.

IVAM pavilion

The largest booth of MicroTechnology in hall 15 is again being organised by IVAM, comprising more than 30 exhibitors, mostly SMEs. A visit to this pavilion covering an area of over 500 square metres will give an excellent overview of industrial and research activities in the area of microtechnology in Germany.

VDI/VDE-IT presents MST Germany

The manifoldness of industrial and research structures in conjunction with microsystems technology in Germany will be the main feature to be presented at the booth of VDI/VDE-IT (hall 15 / D 52). Germany offers unique opportunities to carry out research, to transfer research results into industrial products and services, and to interact with players of all relevant disciplines in a very easy way. The challenge however, especially for foreigners, is a suitable navigation within this complex community. This is an important service VDI/VDE-IT can provide, giving assistance in finding the right partners for microsystems technology research, exploitation and application.

Due to its broad integration into the European Research Area and specific projects in FP6, VDI/VDE-IT additionally can provide services for German actors looking for partners in foreign countries.

Educational issues of microsystems technology have become a key issue for further successful implementation and growth of the industrial sector of microtechnology. VDI/VDE-IT, being involved in a number of dedicated initiatives and activities, can give assistance to young people planning their future as well as to organisations beginning to set up, or already carrying out, education programmes.

Additionally, the status and new topics for specific calls of the BMBF-Microsystems Technology Framework Programme, providing national funding for RTD projects, will be presented.

And last but not least, MicroTechnology offers the chance to personally meet the staff of mstnews.

Micro production live

Organised by VDMA, the German Engineering Federation, problems and solutions of micro production can be experienced within a live demonstration, showing an automated production of stents, based on an existing industrial application (hall 15 / booth D 35). Specific times will be scheduled, where experts will in detail explain and present the various process steps and their integration into an automated production line.

Ultra-precision manufacturing

NC Gesellschaft e. V. is presenting their pavilion on ultra-precision manufacturing (hall 15 / D 50) for the fifth time. Tool and mould manufacturers will show practical examples concerning the utilisation of ultra-precision technology for the production of highly miniaturised products. Technologies like micro milling/turning, ultrasonic milling, micro injection moulding, and others will be in the focus.

MicroTechnology FORUM

Under the motto "Innovations for Industry" Deutsche Messe AG and IVAM in 2005 will again be staging a special forum. In 2004 more than 60 presentations by microtechnology users and suppliers of microsystems from industry showcased the latest products and provided a glimpse of the future at the MicroTechnology trade fair.

This year topics will range from positioning tasks in the micro range to intelligent RFID systems or nanoporous coatings: informative topics for suppliers from all branches. Micropumps for the mass markets, masks for wafer level packaging or multi sensor systems: MicroTechnology is the one and only fair that covers all these disciplines and challenges in miniaturisation within a one-stop shop.

For exhibitors of MicroTechnology, participation with a presentation will be free of charge. Registrations will be dealt with according to the "first come, first served" principle. Please contact Verena Hingst at IVAM immediately to find out about presentation times still open for booking (verena.hingst@ivam.de, phone +49 231 9742169).

Funding opportunities for R&D projects

On Friday, April 15, VDI/VDE-IT will be organising an information day on German national and European premises for funding of R&D projects that will take place at the MicroTechnology FORUM. The German Microsystems Technology Framework Programme, the EUREKA Initiatives, and the 6th Framework Programme of the EU will be covered.

In the morning, several lectures will spotlight the different programmes, their status and the future outlook, and experience gained during the preparation and execution of specific projects.

In the afternoon, the FORUM will turn into a consultancy centre. Experts from the EU, the German National Contact Point for microsystems technology, the EUREKA/COST office of the BMBF, of the Innovation Relay Centre (IRC) North Germany, and finally experts for the German national Microsystems Technology Framework Programme will be offering individual consultation meetings (20 min.) free of charge. For participation, advance reservation is required, all information can be ordered and reservations made by contacting Thomas Köhler (Koehler@vdivde-it.de, phone +49 3328 435149).

Helmut Kergel
kergel@vdivde-it.de

Prof. Dr.-Ing. Dr. E.h. Herbert Reichl Celebrates his 60th Anniversary

mstnews and VDI/VDE Innovation + Technik GmbH congratulate Prof. Reichl on his 60th birthday, wishing him happiness in his personal life and good health so that he may continue with his dynamic and creative way.

Prof. Reichl is an expert of worldwide repute on Microsystems Technology. Since 1987, when assuming a chair at Berlin's Technical University, he has been head of the research group on "Technologies of Microperipherics". Starting in 1993 he was instrumental in setting up the internationally renowned Fraunhofer Institute for Reliability and Microintegration (IZM).

From his early days in Berlin Prof. Reichl, together with his team, has been closely involved with the Federal Republic of Germany's projects and objectives related to Microsystems Technology, whether in his capacity as a highly welcome partner to cooperative projects run by industry or as an appointed member of the national panel on Microsystems Technology.

His record of scientific achievements has been recognized worldwide, winning him awards and docu-mented by numerous patents and publications.

His creativity, his expertise as a scientist and his foresighted approach, which equally reflects techno-logical development, economic requirements and social needs, have made him a stimulating interlocu-tor for VDI/VDE-IT, which has been asked by the Federal Ministry of Education and Research to flesh out innovation policy.

We are grateful for having Prof. Reichl as a partner and are looking forward to conducting with him an interesting exchange of ideas in future too.

Nano is coming - patternable materials for the future

Nanoimprint Lithography

Nanoimprint lithography (NIL) is a low-cost, high throughput alternative lithographic technology that defines patterns by mechanical deformation of a polymer on the sub-100 nanometre scale. It is characterized by parallel patterning across the whole wafer and well suited for mass production of nano-structures. In December 2003, NIL was included in the International Technology Roadmap for Semiconductors (ITRS) as a next generation lithography alternative to be employed at the 32 nm node.

First Market Leadership

Thermoplastic and thermoset polymers for NIL with good thermal and high dry etch stability were developed. They allow applying films with lower thickness and, hence, enable smaller feature sizes for pattern transfer.

Currently ***micro resist technology* GmbH** is the only company in the world who produces these materials for NIL. Standard polymers as well as customized polymers are commercially available.

Applications

Filtered, ready-to-use polymer solutions are available for many purposes. They can be easily applied by spin coating. Film thicknesses from about 80 – 500 nm can be achieved.

Numerous applications have been proposed for NIL: electronics, high density storage, nanomagnetic devices, and beside typical lithographic applications, such as optics, nano-fluidics, nano-electromechanical elements, bio-devices, and transducers.

Materials for Microoptics

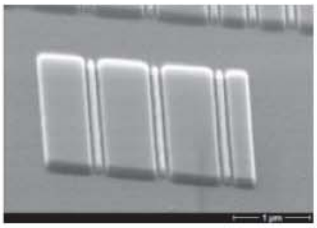
Another new class of advanced materials are ORMOCER®s (inorganic-organic hybrid polymers). Due to the increasing importance of microoptics in nearly all fields of technology (e.g. optical data switches, micro lenses in mobile phone cameras, VCSEL-laser for analytics) there is a strong demand on materials that combine high optical transparency, high stability and easy processing.

ORMOCER® materials combine advantageous properties of ceramics, glasses, and polymers enabling a broad range of applications.

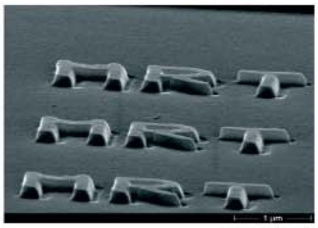
Micro optical elements as mentioned above can be fabricated by replication, UV lithography, or a combination of both.

Beginning with two kind of materials, which were mainly designed as core and cladding materials for optical waveguiding, ***micro resist technology* GmbH** completed its range of products with ORMOCOMP. This material suites very well to the users needs for UVmolding/ soft embossing.

Contact: see advertisement below.



70 nm lines and 50 nm trenches in 300 nm thick mr-I 9000



Ormocomp structure replicated by UV embossing