This paper introduces one of the first reported transmit signal chains in a 45nm CMOS process operating from a 1.1V supply with performance comparable to long-range, wide-bandwidth, high-data rate standards. A new scheme is presented to reduce the number of components in the signal path and enhance the TX chain linearity for use in 4GFOM based systems. A traditional direct-conversion signal path contains a filter, VGA and mixer stage as shown in Fig. 24.6.1. The proposed transmitter combines the functions of the three aforementioned blocks into a single component, as described in the first section of this paper (note: only one filter pole is combined, additional poles must be added as needed). The overall transmitter is then described, followed by measured data to demonstrate performance comparable with operation as a general purpose device, in a co-existence environment.

A key aspect of this transmitter is the use of a single opamp to realize the functional blocks of three TX components; a filter pole, a VGA, and a highly linear active mixer transconductance stage. The approach is based on a traditional single-pole filter stage, where a conceptual single-ended version is shown in Fig 24.6.2. Instead of using the filter output voltage and applying this to the input of a mixer, the current in the opamp output stage, I(s), is mirrored, I(s), and used as the input to an active current-commutating mixer. A resistor, R_c, which dominates the opamp output loading is added. Under the condition that R_c << R_f, R_n (the opamp output impedance) the one-pole filter frequency response will appear in the opamp output current, Fig. 24.6.2. Both the current and the filter frequency response can then be mirrored into the mixer. The passband mixer G_m is approximately 1/R_c. Therefore, variable gain is attained in the mixer transconductance stage by modulating the value of R_c, Fig. 24.6.2.

Reducing the number of active components in the signal path, while combining functionality, improves linearity and lowers the power consumption as compared to more traditional solutions. An active mixer topology, where feedback may be applied to improve linearity, was selected over a passive mixer. The active mixer obviates the need for more high-frequency open-loop gain stages after the mixer, as would be required in the passive mixer approach.

Although the concept of reflecting the filter frequency response in the form of a current may be somewhat obvious, a less salient aspect of this topology is the feedback used to enhance the linearity of the mixer transconductance stage. This approach provides feedback with a single-pole frequency response. The loop gain around M3 and M4 helps to significantly improve the linearity of the mixer transconductance, Fig. 24.6.3. Although similar use of feedback in active mixers has been suggested [5,6], this is the first use of a combined block with both a single pole added and variable gain. While R_1 and C_1 serve as a pole in the forward signal path, they act as a zero from the perspective of M3 and M4, thereby extending the loop bandwidth and further improving the mixer linearity. The differential version of this combined block is shown in Fig. 24.6.3. The mixer transconductance is varied with an array of bridge resistors at the filter output. Any mismatch in R will appear as a common-mode offset, thus providing an additional benefit over approaches that vary the gain using two differential resistors [6].

All components in this transmitter signal path have been designed to run from a 1.1V supply. To compensate for the low g_m (less than 10) in this 45nm process, the mixer opamp uses a folded-cascode topology to improve the open-loop gain, Fig. 24.6.3. Body biasing was used wherever possible, with a resistor to the source [7], Fig. 24.6.3. To maximize the opamp output-signal swing, the output-common mode was set at mid supply. A resistor, R_f, between the opamp inputs and ground creates an input common-mode offset to a PMOS differential pair, required by a low supply voltage [8]. An active-mixer approach is used, thus allowing for smaller switching-device sizes, and removing the need for a buffer which follows the divide-by-2 circuitry. A two-stage matching network between the mixer and pre-PA driver was selected to provide a wide bandwidth. To decrease the die area, a single differential inducer, L_COM in Figs. 24.6.3 and 24.6.4, was used for LC tuning of both the I and Q mixer output, and in the 2-stage matching network. This matching network provides optimal load-line impedances to the mixer output (∼250Ω) and the input of the pre-PA driver (∼7Ω). The simulated Q of the matching network was approximately 4 with a passband loss of ∼2dB.

A single-stage, common-source pre-PA amplifier follows the two-stage matching network, Fig. 24.6.4. This pre-PA driver was biased for Class-AB operation. Discrete variable gain is realized with a 3b binary-weighted array, PO-P2, controlled by switching the cascode devices on or off. An integrated L-section matches the pre-PA driver output to a differential 100Ω off chip.

On wafer-probing was used for measurements. Both the simulated and measured gain versus frequency are shown in Fig. 24.6.5, with a plot of WIMAX EVM versus backoff from P1dB, an example two-tone test TX-output spectrum, and extrapolated OIP3. Measured wideband noise levels of -143dBm/Hz and -146dBm/Hz at 100MHz and 300MHz offset from the carrier were recorded, respectively. This noise performance shows promise for this TX, to be collocated (co-exist) with receivers on the same platform or die, with a modest amount of additional TX-to-RX isolation.

The prototype was implemented in a 6-layer metal 45nm CMOS process. Measured results are tabulated in Fig. 24.6.6. The TX signal path consumes 108mA from a 1.1V supply while occupying an area of 1.0×1.5mm², Fig. 24.6.7. A P_1dB of +12.2dBm and P_{out} of +14.9dBm at 5.5GHz are measured at the TX output with max. gain. This TX reports the highest extrapolated OIP3 (+23.5dBm) found in the literature, at 1.1V.

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References:
Figure 24.6.1: Traditional and reduced-component TX.

Figure 24.6.2: Concept of filter, $G_m$, VGA combination stage.

Figure 24.6.3: Simplified circuit of pole, VGA, & mixer $G_m$ stage.

Figure 24.6.4: Chip block diagram of reduced-component TX.

Figure 24.6.5: Channel response, WiMAX EVM, two-tone spectrum and OIP3.

Figure 24.6.6: Summary of measured results.
Figure 24.6.7: Die micrograph.