A Mm-Wave Gm-Assisted Transformer-Based Matching Network 2x2 Phased-Array Receiver for 5G Communication and Radar Systems

Kun-Da Chu
Electrical and Computer Engineering
University of Washington
Seattle, USA
kdchu@uw.edu

Jacques C. Rudell
Electrical and Computer Engineering
University of Washington
Seattle, USA
jcrudell@uw.edu

***Abstract*—This paper describes a 50-58GHz 2x2 phased-array receiver (RX) for 5G communication and radar systems. The RX utilizes a G_m-assisted matching network (MN) to reduce the noise figure (NF) of a conventional passive mixer-first RX by placing an extra gain of ~5dB prior to the down-conversion mixers with minimal additional components. This prototype phased-array RX integrates a proposed G_m-assisted MN, mixer-first RX with translational feedback, Cartesian phase shifters as a baseband beamformer, poly-phase filters, and LO generation in TSMC 28nm CMOS, occupying a total area of 0.53mm². This RX achieves a NF of 7dB, gain of 26dB, input $P_{1\text{-dB}}$ of -20dBm with an 8-GHz 3-dB BW and a S_{11} lower than -10dB over 22-GHz BW.**

Keywords—5G mobile communication, CMOS receivers, millimeter-wave, phased-arrays, radar systems

I. Introduction

The pervasive nature of future 5th Generation (5G) wireless systems has motivated research to explore low-cost, ultra-broad bandwidth (BW), and low power wireless systems which exploit millimeter-wave (mm-Wave) frequencies. Although CMOS mm-Wave phased-array solutions hold potential to address concerns of cost and silicon size, a key challenge associated with mm-Wave receiver (RX) front-end modules (FEM) relates to the power inefficiency of producing gain at high carrier frequencies. Assuming the RX FEM gain is scaled to exploit the ADC's full range, several points along the RX chain can potentially provide signal amplification, see Fig. 1.

An LNA is traditionally used for signal amplification prior to the down-conversion mixers to improve the RX noise performance [1], [2] (Fig. 1). However, in the mm-Wave bands (above ~30GHz), the gain at the carrier frequency, prior to the down-conversion mixers, becomes extremely power-inefficient due to the inherent gain roll-off. As shown in Fig. 1, the G_{max} of a 10-um-wide NMOS transistor in 28nm technology with a current density of 125μA/μm, is only 10.5dB at 60GHz. By comparison, the same transistor with an identical bias current achieves >30dB of gain for the frequencies below 1GHz. As a result, implementing gain at mm-Wave frequencies is a relatively unattractive choice with respect to power efficiency.

In contrast, mixer-first RX FEMs were introduced to achieve a more power-efficient solution by offloading the burden of RX gain exclusively to the analog baseband (BB) prior to the ADC [4][5]. Moreover, passive mixer-first RXs have shown promise particularly for the applications that demand high linearity, such as 5G and radar systems. For example, BB Cartesian phase shifters and digital beamforming architectures enable opportunities for compact-size phased-arrays in 5G radios [1], but require highly linear FEMs due to the absence of spatial selectivity before the mixers. Although recent passive mixer-first RXs have been demonstrated which achieve high linearity, wide BW, and compact silicon area, this class of FEM topology suffers from relatively poor noise figure (NF) performance due to the lack of gain at the RX input [4][5]. This paper describes a 2x2 phased-array RX which exploits the already existing MN to provide a modest amount of gain prior to the down-conversion mixer, to improve the NF for mm-Wave mixer-first RX.

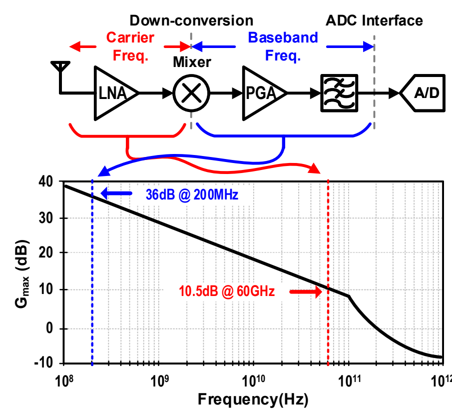


Fig. 1. Amplification-and-down-conversion in a conventional RX (top). G_{max} simulation for a 10-um NMOS transistor with a current density of 125μA/μm.

II. Gm-Assisted Matching Network

Matching networks (MN) can serve a multi-purpose role which includes converting a single-ended signal to differential and impedance matching. Thus, MNs are necessary, independent of the RX architectural choice. Fig. 2 (a) shows a single-element block diagram of a 2x2 phased-array RX with the proposed G_m-assisted MN. Similar to [3], this RX includes a translational feedback loop to significantly reduce the power consumption of the LO driver by using smaller switches, while maintaining a low mixer input impedance. However, in contrast to [3], this RX utilizes the on-chip MN not only to preserve the advantages of wideband input match of a passive mixer-first RX, as was done in [3], but also functions as an amplifier when combined with a feedforward G_m stage to deliver a modest amount of gain prior to the noisy down-conversion mixers.

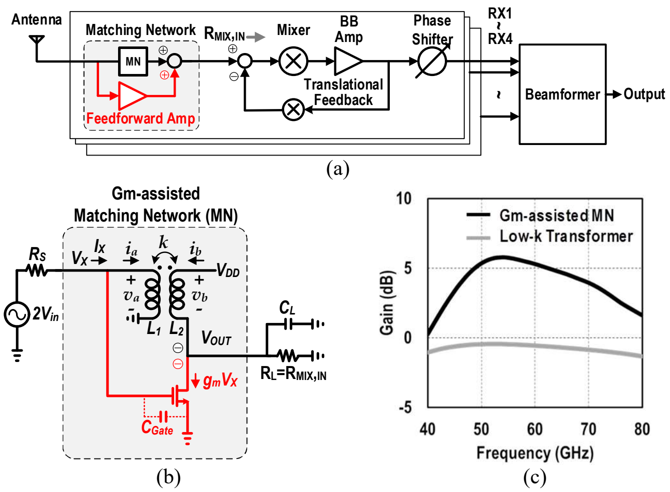


Fig. 2. (a) The proposed 2x2 RX with G_m-assisted matching network. (b) The G_m-assisted matching network. (c) Gain comparison between G_m-assisted matching network and conventional low-k transformers.

The G_m-assisted MN uses an auxiliary G_m common-source amplifier inserted in parallel with a transformer-based MN to provide active gain through a feedforward path from the antenna port to the mixer input, as shown in Fig. 2 (a). With the feedforward amplifier, both the RX gain and noise performance can be improved. The MN is implemented using an ***inverting*** transformer. Both the transformer and common-source G_m have the *same inverting polarity* between the input and output, which is in contrast to traditional drain-to-gate transformer-based feedback amplifiers introduced in [5], see Fig. 2 (b). Moreover, there are significant differences between the two topologies which include: 1) the transformer used in the G_m-assisted MN *has the opposite polarity* as compared to [5], 2) the G_m-assisted MN has a weak amount of *positive* feedback with a loop gain of <-10dB, allowing a modest gain when the output drives a relatively *low-input-impedance* mixer and maintains a high-linearity. In contrast, [5] uses ***negative*** shunt-shunt feedback and can only achieve gain when loaded with a *high-input-impedance* mixer. A key advantage of this feedforward amplifier topology relates to the use of an already existing MN to resonate out the extra parasitic capacitance introduced by the feedforward amplifier without requiring an extra passive component.

In short, the transformer-based MN serves a dual purpose of providing both matching to the antenna impedance, and as a load to the feedforward G_m amplifier realized as a gain stage, while requiring negligible additional silicon area. Fig. 2 (c) compares the simulated gain from the antenna to the mixer input with the G_m-assisted MN and a conventional 4th-order low-k transformer described in [2]. The G_m-assisted MN shows a ~5dB increase in gain while consuming an additional current of 7-mA for the G_m device. Note that more gain can be added by further increasing the size and current of the G_m amplifier. However, this will also add more the capacitive load to both sides of the transformer and make it difficult to satisfy both high gain and wide BW.

III. Circuit Implementation

The block diagram of the 2x2 phased-array RX is shown in Fig. 3. This work employs Cartesian phase shifters in the BB to perform current-mode signal combining. The mixers are driven by 4-phase IQ LOs which are generated locally using poly-phase filters (PPF). A single-ended LO is converted to a differential signal with a matching transformer, then routed to each of the 2x2 arrays using an H-tree LO distribution.

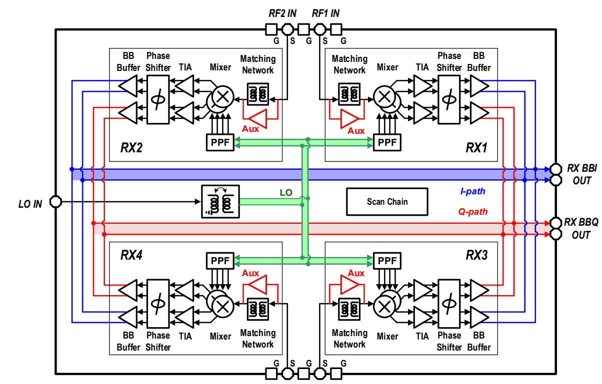


Fig. 3. Block-level diagram of the 50-58GHz 2x2 phased-array RX.

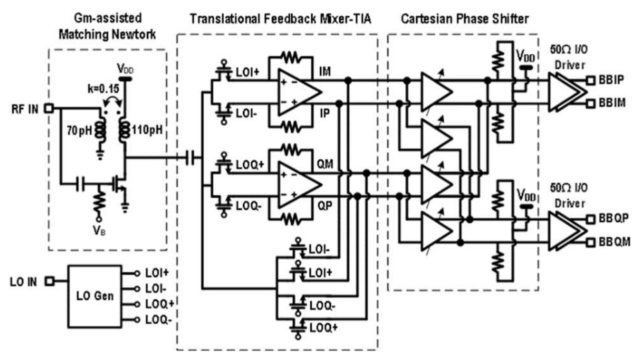


Fig. 4. Detailed schematic of one receiver element.

Fig. 4 depicts a simplified RX signal path schematic of one element in the 2x2 phased array. The matching transformer is designed with a turns ratio of 1:1.25 (70pH:110pH) and a coupling factor of 0.15. The G_m amplifier is placed in parallel with the inverting transformer. The translational shunt-shunt feedback is formed by using a mixer-TIA chain with a mixer switch ratio of 5:1 between the receiving and feedback paths. The Cartesian phase shifter is implemented as a variable gain amplifier (VGA) controlled by the gate voltage of the cascode device similar to [6], which performs vector modulation by summing currents. The quadrature LO phases were generated by using a 2-stage poly-phase filter followed by LO drivers.

IV. Experimental Results

This work was fabricated in TSMC 28nm HPC+ CMOS process with an area of 0.53mm^2. The die photo is shown in Fig. 5. The 4 inputs of the RX elements are on the North and South of the die. The external LO comes in on the left, passing through the LO matching transformer before being distributed to the 2x2 phased array. The differential quadrature BB outputs exit on the chip's right side. This chip was measured using on-chip probing of all external I/O signals and DC bias. The active die area of one RX element is 0.049mm^2 where the G_m-assisted stage occupies an insignificant area of 0.0004mm^2. One RX element consumes 28.5mA from a 0.95-V supply.

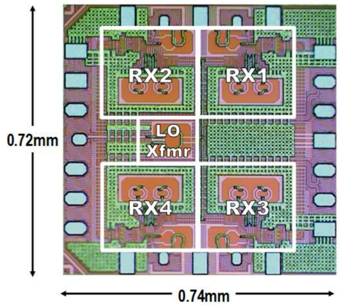
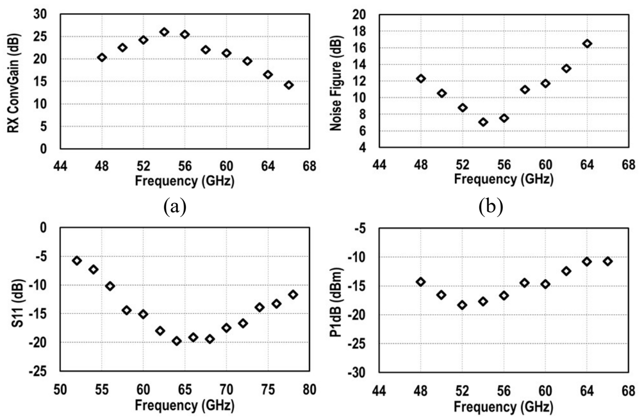
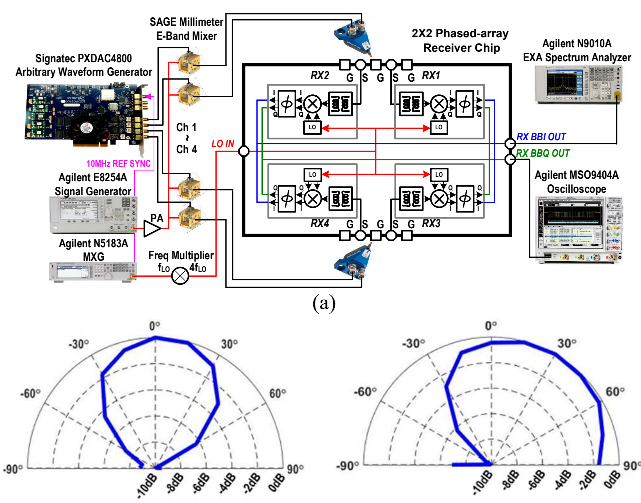


Fig. 5. Die photo of mm-Wave 2x2 phased-array RX.



(a) (b) (c) (d)

Fig. 6. Measured results of one RX element: (a) RX conversion gain, (b) cascaded NF, (c) input return loss (S_{11}), and (d) input P_{1dB}.



(a) (b) (c)

Fig. 7. (a) Lab bench setup. Measured beam patterns results of the proposed 2x2 phased-array RX with two steering angles: (b) 0° and (c) 45°.

The single-element RX performance was measured using a standalone structure on the same chip, results are shown in Fig. 6. The RX achieves a 26-dB peak gain and a 7-dB NF with a 3-dB BW from 50-58GHz and $S_{11} < -10$dB from 56-78GHz. The input P_{1dB} is -20dBm. The RX core consumes a total power of 15mW (excluding phase shifters and buffers).

The setup for the 2x2 phased-array measurement is shown in Fig. 7 (a). An arbitrary waveform generator (AWG) card with 4-ch outputs was used to generate phase differences between the 4 RX inputs to emulate different delays associated with incident angles of an incoming signal. The 4 BB signals were then up-converted and passed through an external PA and a 4-way power divider. Two dual probes (GSGSG) were used to provide the 4 signals for each of the 4 RXs (Fig. 7). The RX LO was generated through an active X4 Frequency Multiplier. All signal generators were synchronized by sharing a common 10-MHz reference clock to ensure the frequency alignment.

To measure the beam pattern, the phase shifters of 4 RXs elements were first set to a steering angle with a fixed static phase error among all RX elements being compensated. The 4 input signals were provided by manipulating the phase difference among the 4-ch outputs of the AWG card with different incident angles from -90° to +90°. Fig. 7 (b) and (c) show two beam patterns with steering angles of 0° and 45°, respectively.

V. Conclusion

This paper presents the design and measurement of a 50-58GHz 2x2 phased-array RX in 28nm process which demonstrates the feasibility for compact, low-power, wide BW, and high-performance mm-Wave radios. Table 1 summarizes the performance of the RX and compare with prior-art RXs

TABLE I. Comparison to Prior-art mm-Wave Rx Publications

	[2]	[1]	[4]	[3]	This Work
Technology	40nm	22nm FinFET	65nm	28nm	**28nm**
Topology	Heterodyne	Direct Conv.	Direct Conv. Mixer-first	Direct Conv. Mixer-first	**Direct Conv. Mixer-first**
Matching Network	Transformer	Transformer	Low-pass π	Shunt LC + L	**Gm-assisted Transformer**
V_{DD} (V)	1.1	1	1.2	1	**0.95**
Freq. Range (GHz)	51-71	71-76	49-67[f]	70-100[f]	**50-58**
BB BW (GHz)	9-11	2[b]	0.32	1.8	**1.2[b]**
RX Gain (dB)	20	36.7	13	25.3	**26**
Single NF (dB)	7.8-9.3	6[g]	11-14	8-12.7	**7-10**
Input P1dB (dBm)	-24	-28[d]	-12	-16.8	**-20**
Power (mW)	115	168[e]	14	12	**15[c]**
Area per RX (mm²)	0.42[a]	0.6[a]	0.39[a]	0.085	**0.049**

[a] Estimated from die photo, without pads. [b] I+jQ BW. [c] The power of buffer driving off-chip is not included. [d] Calculated from reported IP_3. [e] Single element. [f] Frequency range based on S_{11} response. [g] Including T/R SW loss.

References

[1] S. Pellerano *et al.*, "A Scalable 71-to-76GHz 64-Element Phased-Array Transceiver Module with 2×2 Direct-Conversion IC in 22nm FinFET CMOS Technology," in *IEEE ISSCC*, Feb. 2019, pp. 174–176.

[2] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, "An Ultra-Wideband IF Millimeter-Wave Receiver With a 20 GHz Channel Bandwidth Using Gain-Equalized Transformers," *IEEE JSSC*, vol. 51, no. 2, pp. 323–331, Feb. 2016.

[3] L. Iotti, G. LaCaille, and A. M. Niknejad, "A 12mW 70-to-100GHz mixer-first receiver front-end for mm-wave massive-MIMO arrays in 28nm CMOS," in *IEEE ISSCC*, Feb. 2018, pp. 414–416.

[4] A. Moroni and D. Manstretta, "A Broadband Millimeter-wave Passive CMOS Down-converter," in *IEEE RFIC*, Jun. 2012, pp. 507–510.

[5] M. P. van der Heijden, L. C. N. de Vreede, and J. N. Burghartz, "On the design of unilateral dual-loop feedback low-noise amplifiers with simultaneous noise, impedance, and IIP3 match," *IEEE JSSC*, vol. 39, no. 10, pp. 1727–1736, Oct. 2004.

[6] J. Han, Y. Lu, N. Sutardja, K. Jung, and E. Alon, "Design Techniques for a 60 Gb/s 173 mW Wireline Receiver Frontend in 65 nm CMOS Technology," *IEEE JSSC*, vol. 51, no. 4, pp. 871–880, Apr. 2016.