A 0.0023 mm^2/ch. Delta-Encoded, Time-Division Multiplexed Mixed-Signal ECoG Recording Architecture With Stimulus Artifact Suppression

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***Abstract*—This article demonstrates a scalable, time-division multiplexed biopotential recording front-end capable of real-time differential- and common-mode artifact suppression. A delta-encoded recording architecture exploits the power spectral density (PSD) characteristics of Electrocorticography (ECoG) recordings, combining an 8-bit ADC, and an 8-bit DAC to achieve 14 bits of dynamic range. The flexibility of the digital feedback architecture is leveraged to time-division multiplex 64 differential input channels onto a shared mixed-signal front-end, reducing channel area by 2x compared to the state-of-the-art. The feedback DAC used for delta-encoding also serves to cancel differential artifacts with an off-chip adaptive loop. Analysis of this architecture and measured silicon performance of a 65 nm CMOS test-chip implementation, both on the bench and in-vivo, are included with this paper.**

***Index Terms*—BCI, biopotential, delta-encoding, electrocorticography (ECoG), electrocorticography, low-power, neural amplifier, time-division multiplexing.**

I. Introduction

BIDIRECTIONAL Brain-Computer Interfaces (BBCIs) are electronic systems that allow computers to simultaneously record, process, and stimulate neural activity. These systems have become critical technologies for enabling scientific inquiry into human brain function [1] and are ushering in a new era of neuroprosthetics [2], [3]. These advances have the potential to enable new treatments for a number of neurological disorders including Parkinson's Disease [4], epilepsy [5], and depression [6]. Simultaneously, BBCI research continues to drive progress in the field of human-computer interaction.

Fig. 1 illustrates an example BBCI implementation. Bidirectional communication with the brain is made possible by recording the signals emitted by the brain and stimulating the tissue either in the cortex or in the peripheral nervous system. In-line computation elements allow for closed-loop bidirectional communication with the central nervous system.

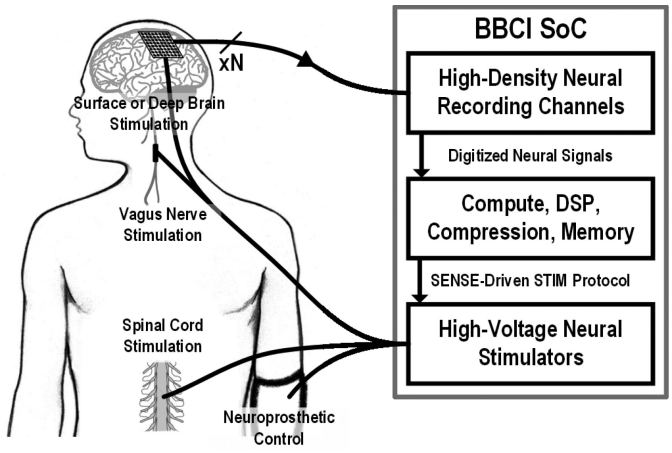

Fig. 1. Conceptual diagram of a closed-loop Bidirectional-Brain Computer Interface (BBCI) which includes neural recording, real-time digital computation, and stimulation.

Chronic (long-term) BBCI applications face several key engineering challenges. The desire for high electrode density and large spatial coverage motivates neural interfaces with thousands of electrodes [2]. However, the silicon area required to scale existing solutions is prohibitive. Concurrent stimulation and recording activity resulting from closed-loop neuromodulation generates large stimulation artifacts that obfuscate important signals during and shortly after stimulation. Power density requirements due to tissue heating remain restrictive, particularly in monolithic solutions [7].

This paper presents a channel, process, and frequency scalable recording system in standard 65 nm CMOS which makes several contributions to the state-of-the-art: 1) Time-domain multiplexed recording channels to enable a demonstrated two-fold reduction in silicon area for ECoG recording. 2) A delta-encoded feedback loop exploits neural signal statistics to provide large dynamic range by combining low-precision data converters to achieve high-precision recording. 3) Real-time, event-driven

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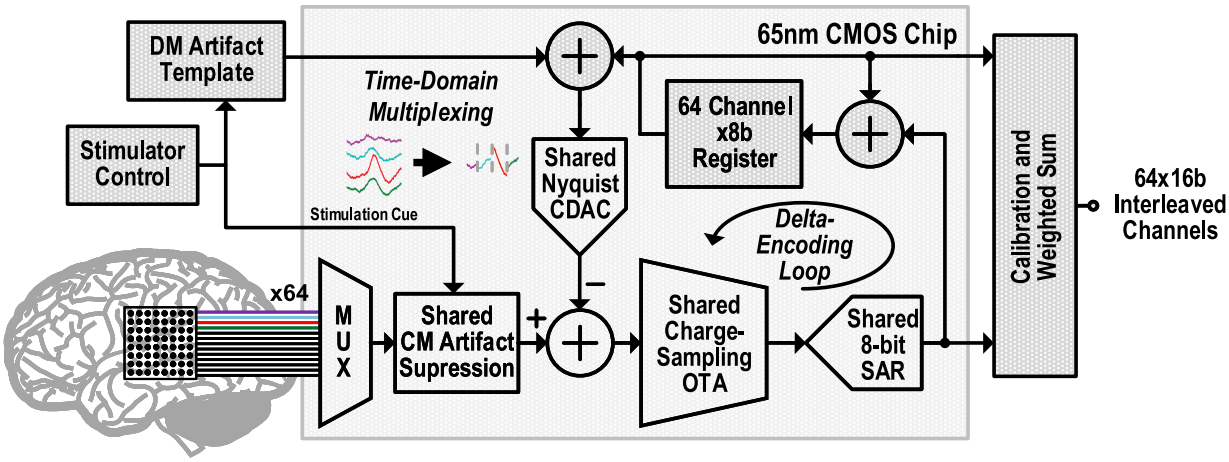


Fig. 2. Functional block diagram of the highly-multiplexed, digitally-delta-encoded ECoG signal chain with common- and differential-mode artifact suppression that is selectively enabled when cued by the stimulator.

common- and differential-mode artifact suppression that is enabled at the amplifier inputs during artifact events.

This paper is organized as follows: In Section II we discuss the system architecture and analysis that led to the implemented prototype. Section III describes the details of the fabricated test chip. Bench and in-vivo measurements are presented in Section V. Finally, we discuss conclusions and potential next steps of this work in Section VI.

II. Artifact-Suppressing Multiplexed Digital-Feedback Architecture

Many biopotential signals, including ECoG, are highly colored, exhibiting an approximately $1/f^2$ relationship to the Power Spectral Density (PSD) [8]. Therefore, high-frequency low-amplitude portions of the signal spectrum set the sampling rate requirements of the system while large-amplitude, low-frequency spectral content requires a large front-end dynamic range. These PSD characteristics strongly motivate delta-encoded signal acquisition, where recording the differences between samples allows dynamic range requirements to be significantly reduced. Fig. 2 shows a block diagram of the system architecture, optimized for multiplexing and frequency-shaped dynamic range. While stimulation artifacts do not exhibit the same helpful PSD structure, their occurrence can be accurately anticipated with a cue communicated by the stimulator to the recording system. Knowledge of the arrival of an artifact is exploited to enable (learned) template-based artifact cancellation of differential-mode (DM) artifacts, and double-sampled switched-capacitor based common-mode (CM) artifact cancellation. Because these artifacts are suppressed effectively at the amplifier front-end, an impact on amplifier dynamic range is avoided. Both these techniques are applied on-cue from the stimulator and suppress artifacts at the amplifier input to avoid adversely impacting amplifier dynamic range. The proposed architecture also provides several other significant enhancements including multiplexed amplifier operation, scalable sampling frequency while using simpler, more robust circuit blocks to achieve similar system specifications. As we will show, these architectural enhancements demonstrably do not affect the first-order noise performance of the system.

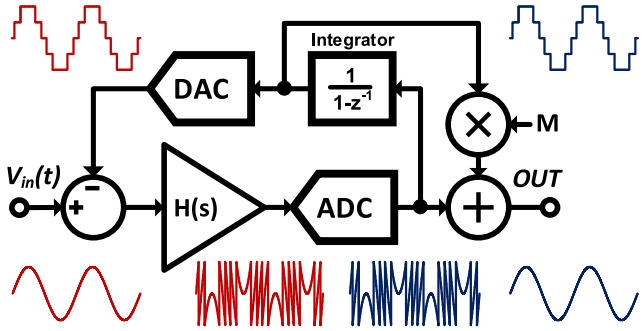


Fig. 3. Delta encoding using an accumulating digital feedback loop. The aggregate count in the accumulator tracks the coarse voltage level that is fed back to the DAC, while the ADC output is the delta between the accumulated value and input voltage. Summing the ADC residue with the DAC interpolates the coarsely quantized DAC output to reconstruct the full signal waveform.

A. Delta Encoding

We have previously shown in [9], [10] that the PSD characteristics of biopotential signals can be exploited to reduce amplifier and ADC dynamic range requirements. In this work, we implement delta-encoding using mixed-signal feedback to similarly shape the signal spectrum (Fig. 3). In contrast with existing mixed-signal feedback schemes that implement DC servo-loops [11]–[15], delta-encoding [16], [17], or auto-ranging circuits [18] that require high-precision oversampling converters, the proposed architecture uses delta-encoding to track differences between successive samples with Nyquist rate conversion. This approach significantly reduces the ADC dynamic range requirement for signals containing low-amplitude, high-frequency and high-amplitude, low-frequency content. Delta encoding also

compensates for DC offset in DC-coupled systems, such as this one.

The input signal is differenced with the previous sample, and this low-dynamic-range residue is passed through a gain stage $H(s)$ and then digitized at moderate resolution (8 bits). The ADC provides a code to a digital accumulator that tracks the large-scale variation of the signal based on the incremental differences between values. This accumulation is fed back to the input to complete the delta-encoding operation [19], [20].

Implementation with a full-scale feedback DAC would require oversampling. Instead, a truncated portion (MSB-intact) of the ADC is accumulated and stored as coarse representation of prior channel voltage, allowing for a 8-bit Nyquist-rate feedback capacitive-DAC. The signal can still be fully reconstructed by adding the accumulator output weighted by the gain factor M to the ADC residue output. Thus, the ADC acts as an interpolator for the delta-encoder, allowing high-resolution data acquisition using moderate-resolution converters. M is calibrated to compensate for DAC transfer function nonidealities which are amplified at the ADC input.

B. Multiplexing for Channel Area Reduction

The proposed digital feedback architecture makes it possible to multiplex the feedback networks for many channels using compact memory storage. Multiplexing the entire signal chain allows this implementation to achieve recording channel density approximately two-times the state-of-the-art, without a dependence on specialized low-offset electrodes or trading off power for area reduction [21]. The accumulated residue in Fig. 3 is stored independently for each channel and then recalled periodically, providing programmable support for up to 64 channels with a common front-end.

To achieve a large number of multiplexed channels, the amplifier must have a wide bandwidth so that settling is possible between adjacent independent channels. However, this requirement directly contradicts the need for a low-pass response to eliminate noise aliasing from higher frequencies at the amplifier inputs. Filtering is achieved by the rectangular integration time window, which creates a $sinc$ envelope filter on the input signal and input noise, while leaving the amplifier noise of a single stage amplifier in terms of kT/C. The bandwidth is extended with minimized power draw by operating partially in the charge sampling region. The amplifier output impedance can be higher, as τ is larger than the sampling window, reducing the necessary current.

As described in [22], the total noise power due to noise sources before the charge integration stage is proportional to the sampling interval, which is nominally reduced by a factor of N, the number of independent channels. This increased power corresponds to an increase in the noise voltage by a factor of $\sqrt{N}$. Because of this penalty, additional gain stages before the integrating amplifier should be avoided, so that only biological and electrode noise is amplified by this factor. This penalty is reasonable for many electrode configurations where electrode noise does not limit the signal acquisition [23], [24]. Switching the CDAC does introduce kT/C noise before the gain stage. However, because this noise is shunted toward the much larger electrode-tissue capacitance, upon sampling, the contribution of this noise is negligible.

Crosstalk between adjacent samples should also be considered for multiplexed channels. Residual voltage from the previous channel can considerably influence the trajectory and sampled value of the current channel, especially when charge sampling, because the signal is not allowed to settle. To avoid this problem, each node in the circuit is auto-zeroed with high-precision settling between samples.

III. Detailed System Implementation

Details of the overall system are shown in Fig. 4. Multiplexer switches connect 64 differential electrode pairs (represented as an RC model) to a shared switched-capacitor front end. The input DC-blocking capacitors C_{IN} can be reconfigured as sampling capacitors for common-mode artifact suppression (CMS). The complimentary 8-bit CDAC moves charge at the amplifier inputs to track similarities between subsequent samples, using a thresholding operation and register file to independently integrate the ADC outputs for 64 channels. The residual difference is integrated onto C_L for the sampling period and quantized by an 8-bit SAR ADC.

Charge sampling in the amplifier eliminates the added power requirements of 7τ settling (assuming 8-bit resolution) typically required to sample the input signal after transitioning to a new channel [25]. Excessive clock jitter can significantly degrade precision in a charge sampling implementation, but the jitter resulting from a ring oscillator powered by a regulated supply was found to be low enough for this application. A return-to-zero technique implemented at the amplifier inputs eliminates crosstalk between channels (measured at -92 dB) and offers a time-invariant switched-capacitor DC input resistance to each channel. Use of a single amplifier for recording an array of channels naturally offers correlated double-sampling using a dummy channel to reduce flicker noise if required by the application.

Mixed-signal delta-encoding is enabled by combining digital storage for each channel with an 8-bit feedback DAC to perform the differencing operation. Delta-encoding allows an 8-bit Nyquist-rate ADC to provide the dynamic range required for ECoG signal acquisition. The signal can be reconstructed by adding the stored signal state to the ADC output (the digitized delta-encoder residue). The accumulated value, to be provided to the DAC in the next cycle, must be updated to allow the system to track the input signal. The update quantity is determined based on comparing the ADC code to user-programmable thresholds (Fig. 2, blue and green bacnds). These comparisons motivate an update of $+1$, -1, and 0 to maintain tracking.

The G_m stage gain is highly configurable for flexible use and is calibrated first by minimizing the size of the load capacitance for a given gain setting, and then by fine tuning with the precise integration time. This provides the optimal noise performance for a given configuration, as shown by τ in Equation (3). Configuring the gain with the integration time alone, while effective, is suboptimal for noise performance and should be avoided. In general, the value of capacitance for a given sampling rate and

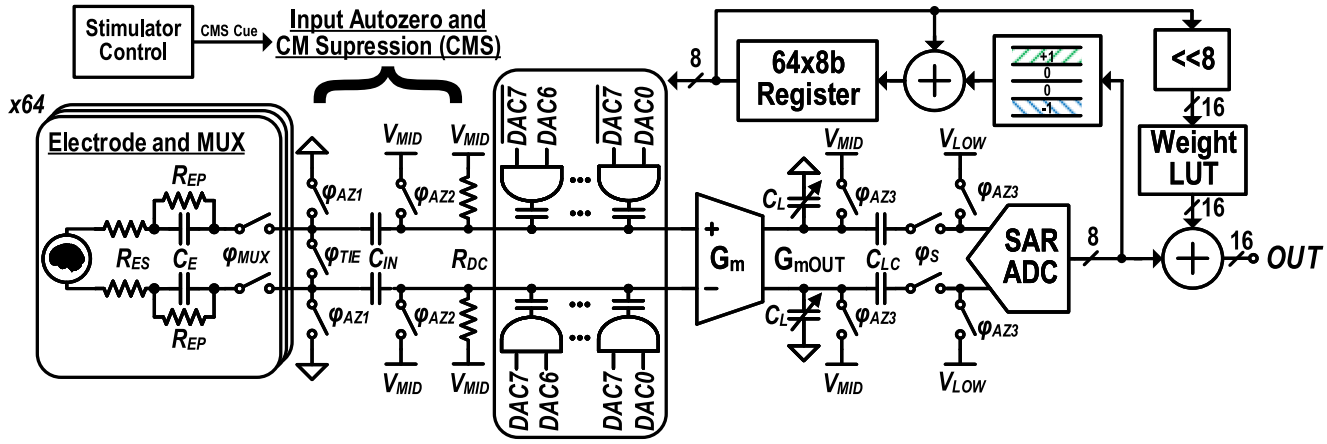


Fig. 4. Detailed schematic of the analog front end, including delta-encoded feedback loop with 8-bit DAC and 8-bit ADC, CMS system, autozero technique, and interpolation.

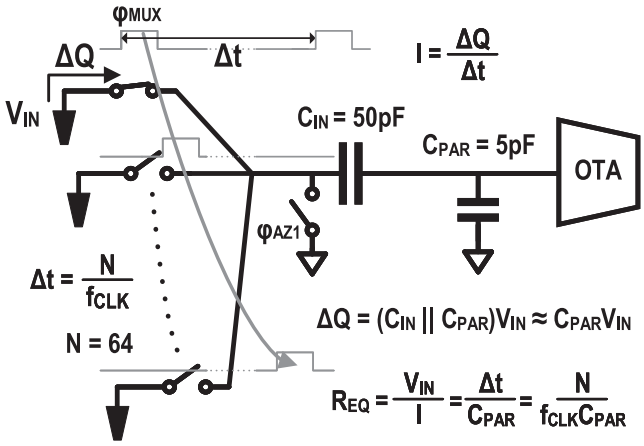


Fig. 5. Conceptual diagram of input network charging and resulting equivalent input resistance, as see from the perspective of each recording electrode.

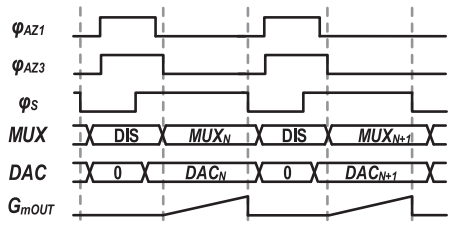


Fig. 6. Autozero and sampling operation timing diagram for normal recording mode. Note: Switch AZ2 remains open during normal operation.

number of channels is fixed, and fine tuning the integration time is unnecessary due to the DAC calibration procedure.

This one-time calibration of the DAC weights is performed by fitting them to a bathtub curve during post-processing and is a sufficient approach for handling systematic DAC nonlinearity [26]. Charging the 5 pF equivalent input capacitance from the electrodes creates a sampling-frequency-dependent input resistance, as shown conceptually by Fig. 5. This input resistance forms a high-pass corner with the series electrode capacitance (C_E) that is on the order of 1 Hz for most electrodes [27].

A multiplexed front end results in a system that is inherently DC coupled. Switching between channels using auto-zeroed inputs requires the channel to charge the amplifier input, leading to the presence of a switched capacitor resistor at the amplifier input. Importantly, this switched capacitor consists of the capacitance of the DAC and the g_mC amplifier (amounting to approximately 5 pF) and not C_{in}. Although the potential across C_{in} changes in this multiplexed front-end, the system is designed to ensure that the charge delivered to C_{in} is provided by the supply voltage, not the input signal.

A. Timing

Figure 6 shows the timing of the system in normal operating mode. When the system is ready to transition to the next channel the input MUX is disabled and the DAC is returned to zero-state, ensuring that sampling, amplification and quantization for each channel are performed with identical impedances independent of the state of the previous channel. Next, the auto-zero switches are activated, bringing both the input and output to a known voltage. During nominal operation the transconductor input is not auto-zeroed, but instead uses a large pseudoresistor to set the bias. Using a pseudoresistor avoids the injection of kT/C noise at the amplifier inputs that would occur when the switch samples the reference voltage. This differs from the switching noise contribution at the MUX output node, because the series capacitor creates a high-impedance between the switch and ground. In contrast, the MUX output node has a low-impedance path to ground through the MUX that almost entirely dissipates the switching noise before amplification begins.

After the auto-zero is completed, the sampling switch at the input to the ADC is closed. The system is still not sampling, because the output auto-zero remains active. Next, the DAC is enabled just before ϕ_{AZ1} is opened, ensuring that the DAC sees a uniform impedance. The MUX is then enabled. Finally, the auto-zero switch at the output is opened, which allows the OTA to begin accumulating charge at the output. When the sampling window is completed, the sampling switch opens and the whole process begins again on the next channel.

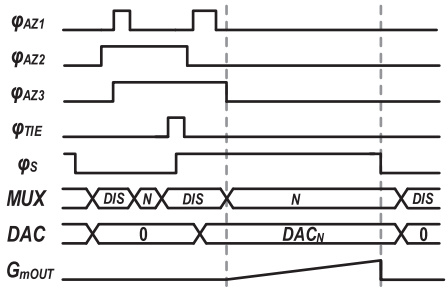


Fig. 7. Autozero and sampling operation timing diagram for CMS operation.

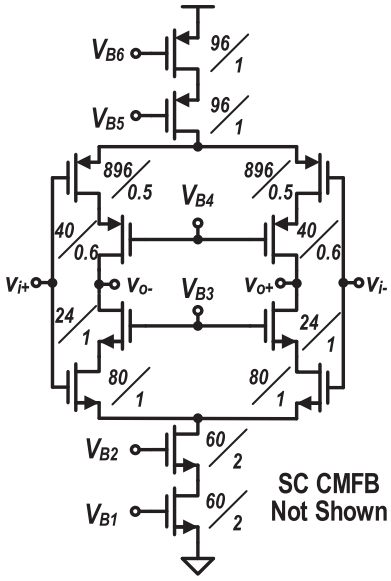


Fig. 8. Transistor level implementation of the charge-sampling OTA, similar to [28].

Front-end operation under CMS conditions, as described in Section IV-B is shown in Fig. 7. This mode is enabled for a brief duration during and after stimulation events, and is similar to the nominal operating mode, with the key difference that the common mode voltage is first sampled across the input capacitors through a simple switching scheme. As previously mentioned, CMS introduces kT/C noise at the input node. Given the typically low duty-cycle of stimulation, this does not have a significant impact on overall system noise performance.

B. OTA Stage

A schematic for the operational transconductance amplifier (OTA) is shown in Fig. 8. The cascoded current-reuse amplifier topology, similar to [28], leverages the presence of a 2.5 V supply needed by a stimulator on a monolithically integrated chip, allowing a large amplifier device stack using thick-oxide devices, which improves noise efficiency and CMRR without gate-leakage concerns.

The two sets of input pairs are sized to operate deep in weak inversion, with very large device areas to mitigate flicker noise. Cascode devices are sized in moderate inversion to maximize gain while minimizing the effects of their capacitance. The input CM voltage to the PMOS and NMOS devices is designed at $V_{DD}/2$, so the tail devices are cascoded with the available headroom to improve CMRR and PSRR.

C. ADC Implementation

The ADC at the output of the amplifier serves as the sampling switch and a portion of the load capacitance for the charge-sampling amplifier. It is implemented as a top-plate sampling, monotonic-switching asynchronous SAR ADC [29], [30]. In this fully differential implementation, a 7-bit DAC combined with an initial sign measurement creates an 8-bit output. The unit capacitor is implemented using a Metal-Oxide-Metal (MOM) capacitor structure with a unit size of 7.7fF. The large unit capacitor provides robust operation, and the resulting marginal increase in power dissipation is insignificant given that the OTA dominates overall power. The entire ADC is powered with a 0.5 V supply and reference voltage. This small reference voltage reduces the dynamic range requirements of the OTA and the LSB size of the converter and also reduces ADC power consumption.

D. DAC Implementation

The DAC was implemented using a monotonic switching structure similar to the ADC. 10fF unit capacitors are binary weighted over 7 bits with an additional sign bit from differential operation. The aggregate capacitance of the DAC forms a voltage divider with the 50 pF input capacitors and parasitic capacitance from the amplifier inputs. The capacitors are initially sized based the flicker noise requirements of the transconductor devices, and the input capacitors are designed at 10-times the total parasitic capacitance to prevent capacitive division of the input signal. Driven at 2.5 V, this voltage divider creates a nominal DAC LSB of 500 μV. This LSB size covers approximately half of the input-referred differential range of the forward signal path. Variations in the common-mode voltage due to monotonic switching of DAC elements are partially mitigated by inverting the switching direction of the MSB [31]. The residual variation in the common-mode range does not affect the linearity of the system output with a THD specification of 0.1%.

IV. Analysis

A. Noise Analysis

Two general paradigms exist for sampling of signals, as illustrated in Fig. 9. Conventional sampling requires several time constants, τ, to achieve a desired settling accuracy in the sampling interval. Charge sampling, as discussed above, relies on a precise sampling period so does not require settling for multiple time constants. Therefore, charge sampling reduces the required amplifier bandwidth substantially, decreasing power consumption and amplifier noise when compared with traditional sampling.

Noise analysis of the system must be performed to identify the optimal time-constant for this first-order system. For simplicity, this analysis is limited to thermal circuit noise. Other noise sources will scale in the same fashion. The noise generated by a

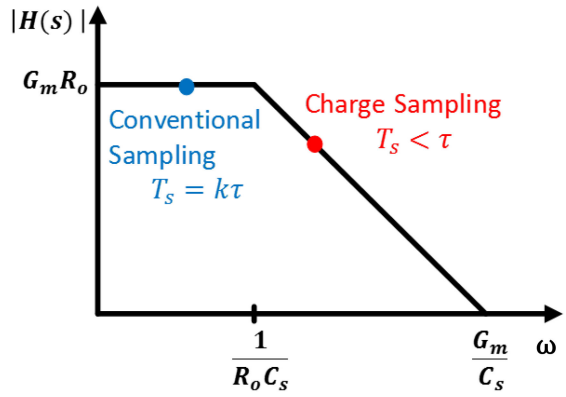


Fig. 9. Qualitative frequency-domain description of charge sampling with respect to conventional sampling. Charge sampling occurs above the 3 dB bandwidth of a single-pole amplifier and sacrifices some gain for faster settling response.

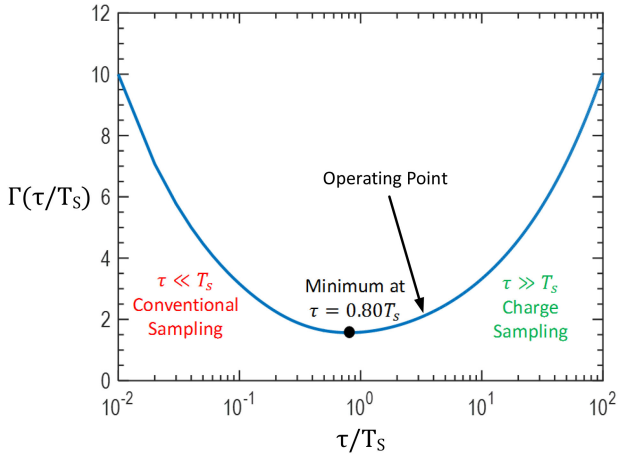


Fig. 10. Equation (3) has a minimum at $\tau \approx 0.80\,T_s$.

transconductance amplifier is given by $\overline{i_N^2} = 4kT\alpha G_m$, where G_m is the stage transconductance, α captures topological, sizing, and process constraints on transconductor noise performance, k is Boltzmann's constant and T is temperature. From this expression, the output noise voltage from one sampling operation can be shown to be:

$$\overline{v_{N-out}^2} = \overline{i_N^2} R_o^2 f_{noise} = \alpha G_m R_o \frac{kT}{C_L} \tag{1}$$

where R_o is the amplifier output resistance and C_L is the sampling capacitor. The gain of the circuit, including transient effects, is given by $A = G_m R_o[1 - e^{-\frac{T_s}{R_o C_L}}]$, where T_s is the sampling interval bounded by the sampling rate. Therefore, the input referred noise can be written as:

$$\overline{v_{N-in}^2} = \frac{\overline{v_{N-out}^2}}{A^2} = \frac{\alpha kT}{C_L G_m R_o \left[1 - e^{-\frac{T_s}{R_o C_L}}\right]^2} \tag{2}$$

After grouping terms, the input-referred noise voltage is given by Equation (3), where $\tau = C_L R_o$. An efficiency factor, $\Gamma(\tau/T_s)$, captures the effect of finite per-channel charge-sampling time. For the chosen operating point, where $\tau \approx 0.8T_S$, $\Gamma(\tau/T_s)$ becomes $\Gamma_{\min}$.

$$\overline{v_{N-in}} = \sqrt{\frac{\alpha kT}{G_m T_s}} \frac{\sqrt{\frac{T_s}{\tau}}}{\left[1 - e^{-\frac{T_s}{\tau}}\right]} = \sqrt{\frac{\alpha kT}{G_m T_s}}\ \Gamma_{\min} \tag{3}$$

This expression demonstrates the expected inverse proportionality between noise voltage and $\sqrt{Gm}$. It also shows that the sampling interval, T_s, should be set to the maximum value allowable by the sampling frequency. For a given T_s, noise efficiency is achieved by minimizing Γ across possible values of τ/T_s (Fig. 10). From the figure, the optimal choice corresponds to $\tau \approx 0.8T_S$.

Since the analysis assumes a single-pole transconductor, the amplifier has optimal noise performance with a sampling interval just above the 3 dB bandwidth. However, this bandwidth is highly dependent on the process-sensitive output resistance of the amplifier. Given this additional consideration, we instead designed the amplifier 3 dB bandwidth to be slightly below the corresponding sampling angular frequency, in the integrating region of the curve where sensitivity to the output resistance is sufficiently mitigated (Fig. 10).

In this implementation, digital calibration is necessary to compensate for open-loop transconductance and load capacitance variability. First-order calibration is implemented through a judicious combination of digitally-tunable load capacitance and integration time.

Assuming weak-inversion operation, $G_m = 25I_{D,N}$. We denote the amplifier current of this N-channel system as $I_{D,N}$. Under the optimality criterion prescribed by Fig. 10, Eq. (3) can be re-written to analyze the system in the context of supporting N channels as follows:

$$\overline{v_{N-in}} = \sqrt{\frac{\alpha kT}{G_m \cdot T_s}}\ \Gamma_{\min} = \sqrt{\frac{\alpha kT}{25 I_{D,N} T_s}}\ \Gamma_{\min} \tag{4}$$

Proportionally scaling the current with channel count yields $I_{D,1} = I_{D,N}/N$, where $I_{D,1}$ is the equivalent amplifier current for a single channel. T_s must scale by N to support concurrent recording at a target sampling rate per channel, where $T_{s,1} = T_s/N$. Writing T_s in terms of $T_{s,1}$ and substituting yields:

$$\overline{v_{N-in}} = \sqrt{\frac{\alpha kT}{25 I_{D,1} T_{s,1}}}\ \Gamma_{\min} \tag{5}$$

The sampling period, proportional to N, cancels the accompanying scaling of the amplifier current with channel count in Eq. (5). Multiplexing is therefore, to the first order, neutral in circuit power for a given input-referred noise target when compared with non-multiplexed, single-amplifier-per-channel approaches.

B. *Artifact Suppression*

Common- and differential-mode artifacts (Fig. 11) severely degrade recording performance in BBCIs because the required stimulation voltages are much larger than the recorded signals.

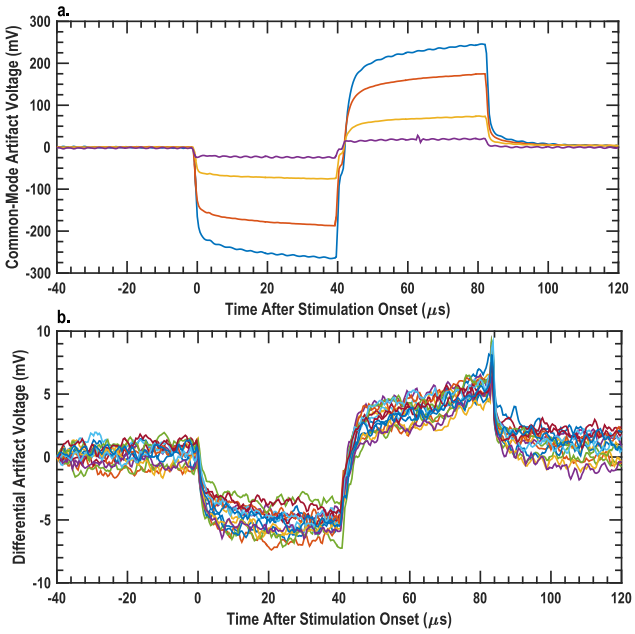


Fig. 11. Common-mode (a) and differential-mode (b) artifacts for an H-bridge type stimulator. The amplitude and shape of both artifacts can vary considerably with the stimulation current and electrode.

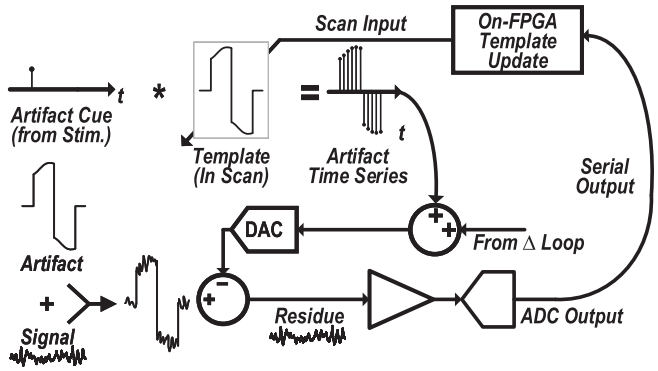


Fig. 12. Template-subtraction based architecture. A cue from the stimulator during a stimulation event enables look-up of the learned artifact. Samples of this template are combined with the Delta-Encoding feedback signal to cancel stimulation artifacts at the amplifier input.

Neuroscientists are interested in neural behavior that occurs shortly after stimulation [1]. As a result, techniques that suppress common- and differential-mode artifacts are critical enabling technologies for BBCI applications. This system includes differential- and common-mode artifact suppression that can be selectively enabled during artifact events when provided a cue from the stimulator.

In this mixed-signal feedback implementation, the feedback DAC can be leveraged to enable differential stimulation artifact suppression at the amplifier inputs, as shown in Fig. 12. Off-chip artifact template training uses a least mean-squared (LMS) algorithm [32] to iteratively learn the optimum template using the ADC output on the FPGA controller.

The FPGA also controls the stimulator and provides the correct template for each stimulation event. A multiplexed recording architecture requires template interleaving because each channel sees a different voltage artifact. The interleaved templates are synchronously serialized with the on-chip recording clock domain, transmitted, and de-serialized on chip. These transmitted artifact codes are summed sample-by-sample with an adder into the delta-encoding loop feeding the input DAC. Implementing the LMS algorithm and artifact template storage on chip would require 256 bits of SRAM per artifact channel, multiplexers, adders, and a bitwise shift. With low-voltage logic, a sign-error LMS algorithm can be performed with 100nW and less than 0.02 mm^2 per channel [33].

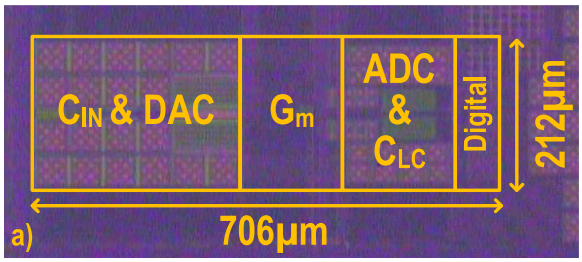
The proposed architecture also supports more sophisticated adaptive equalization methods implemented on the FPGA. The efficacy of differential suppression techniques is limited by the DAC dynamic range: very large artifacts would require a large DAC range. Additionally, DAC quantization limits the precision of artifact suppression. However, the objective of DM cancellation is to suppress artifact to within the linear range of the amplifier, enabling downstream signal processing for more aggressive removal of these artifacts [34], [35].

Large common-mode (CM) artifacts on the order of 100 s of mV are often overlooked but can also degrade performance, particularly with the noise-efficient open-loop amplifiers employed in modern neural recording systems. Recently published worked demonstrates suppression of CM artifacts using an active CMFB stage [36]. This technique works well for conventional non-multiplexed approaches, but an analog CM loop would require prohibitively high amplifier bandwidth for multiplexed architectures. We implemented a passive, switched-capacitor technique for CM artifact suppression, elaborated upon in [37]. The CMS is selectively enabled on-cue by the stimulator to stabilize the amplifier operating point for the duration of the artifact. CMS maintains gain across the input signal range and suppresses distortion by using a correlated double-sampling technique. Use of the CMS mode introduces kT/C noise when releasing the auto-zero at the transconductor input, resulting in a 12 dB SNR reduction while CMS is enabled during stimulation. This scheme is included in the multiplexed amplifier discussed herein, but can also be utilized for non-multiplexed topologies.

C. Frequency Scalability

An additional benefit of charge sampling is that the system scales efficiently with frequency by tuning of the sampling capacitor C_L. The gain of the amplifier in the charge-sampling regime is given by $A_v = G_m T_s / C_L$. As T_s changes due to higher or lower sampling frequencies, the gain can be held constant without modifying the G_m. This characteristic allows for scaling of the system without modifying the transistor-level design of the amplifier. Coupled with the ability to select the number of channels, the system can be scaled in frequency with only a square-root impact on noise efficiency as T_s decreases, as can be seen from Equation (4).

Scaling sampling frequency also affects the system input impedance and bandwidth. The series capacitive component of electrode-tissue impedance forms a high-pass corner with the input impedance. Sampling on the front-end input capacitance creates an equivalent input resistance proportional to sampling



b)

Power Breakdown			
DAC:	400 nW (0.2%)	Reg.:	3.4 µW (1.8%)
ADC:	764 nW (0.4%)	MUX:	3.6 µW (1.9%)
Logic:	2.5 µW (1.3%)	Gm:	180 µW(94.4%)

Fig. 13. (a) Die photomicrograph of 65 nm 1p9m TSMC CMOS 64-channel multiplexed recording prototype and (b) system power breakdown.

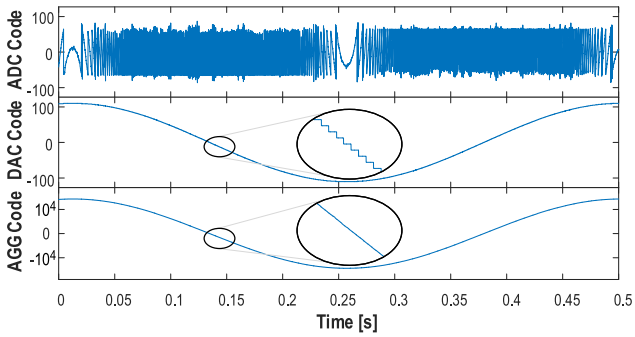


Fig. 14. Demonstration of the ADC+DAC aggregation for a 2 Hz, 35 mV rms sinusoidal input demonstrating the DC offset cancellation range of the system and basic operation. The ADC residue interpolates the coarsely quantized DAC signal to create a 14-bit aggregated output.

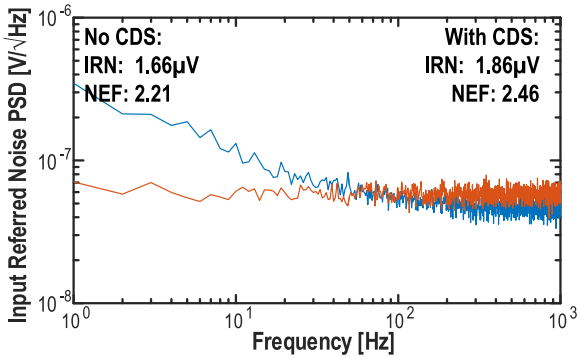


Fig. 15. Input-referred noise measurements for ECoG recording configurations operating with time-domain multiplexing. Noise measurements are shown for one of the 64 operational time-interleaved channels. Switching noise is below the amplifier noise floor by design. Correlated-double sampling (CDS) operation is also shown (in orange).

frequency by $1/f_sC_{in}$. During normal operation, C_{in} is the parasitic capacitance of the CDAC and OTA, approximately 5 pF. During CMS, signal is sampled onto the 50 pF series input cap. Electrode capacitance and input resistance combine into a high-pass corner, $f_{HP} = 1/2\pi R_{in}C_{el} = f_sC_{in}/2\pi C_{el}$. Secondly, pre-charging C_{in} with the CDAC reduces f_{HP} by partially using charge from the supply rather than the electrode for sampling low frequencies. For an 800 pF microwire electrode, the theoretical high-pass corner without pre-charging is $f_{HP} = 2kHz5pF/2\pi 800$ pF $= 2$ Hz. A 700 mHz corner was measured in this scenario due to the pre-charging effect. Enabling CMS temporarily increases the input capacitance to 50 pF, only during stimulation events. A corresponding a 10 Hz corner was measured sampling off of an 800 pF electrode capacitance at 2kS/s.

V. Measurement Results

This system prototype was fabricated in a 1P9M 65 nm CMOS process. The die photo is shown in Fig. 13. The chip has been tested both on the bench for performance measurements and in-vivo to verify functionality in living tissue.

A. Bench Measurements

Bench measurements used an emulation of a Platinum-Iridium microwire with $R_{ES} = 7.5$ kΩ, $C_E = 820$ pF, and $R_{EP} = 5$ GΩ [23]. A Stanford Research Systems DS360 signal generator was used for high-resolution sinusoidal signal generation at low frequencies, and a Terasic DE1-SOC FPGA board was used for digital acquisition and analysis.

Figure 14 demonstrates a measured signal recording of a full-scale 35mVrms sinusoid applied at the inputs. This figure displays the interpolation of the accumulated output voltage that drives the DAC with the ADC output residue to form a complete high-resolution waveform.

The noise performance of the system sampling at 2kS/s is given in Fig. 15. The use of correlated double sampling (CDS) is also demonstrated for ECoG recording to demonstrate that flicker noise can be mitigated—if necessary—at the expense of an increase in the thermal noise floor [38]. This increase is due to uncorrelated thermal noise from the signal and reference electrodes.

Fig. 16 shows the INL and DNL of the system before and after calibration. Minimizing INL is a key objective to maximize system performance. Before calibration, the INL of the system varies considerably because the 8-bit DAC linearity is insufficient after amplification when compared to the ADC output linearity. Post-processing of the DAC code weights to minimize INL addresses these linearity constraints. The gain variation due to amplifier CM-DM conversion also contributes to INL by varying the slope of the interpolating sections. This variation increases the INL to < 3 LSB.

Linearity is also often evaluated using total harmonic distortion (THD). The mixed-mode feedback of this architecture allows for large signal swing at low frequencies, shaping the linear dynamic range as seen in Fig. 17. The delta-encoded feedback creates a dynamic range profile that matches the characteristic $1/f^2$ ECoG signal profile.

The measured signal transfer function (STF) of the system for 2kS/s ECoG recording is shown in Fig. 18. The results show a 3 dB bandwidth below 1 Hz. The STF is also shown for the reduced-impedance case where CMS is enabled. These modes are enabled intermittently during stimulation events, and

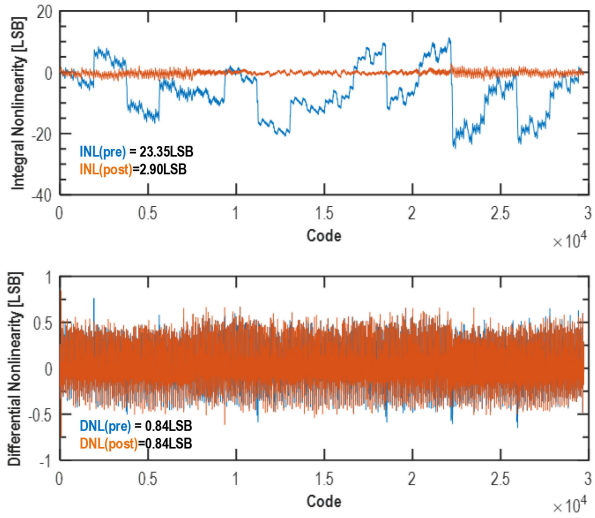


Fig. 16. INL and DNL measurements of the prototype both before and after calibration obtained using the histogram method over 16777216 samples. The DNL is dominated by the noise floor of the amplifier, while the INL shows 2.90LSB linearity after calibration, demonstrating very strong linear performance across the entire input range.

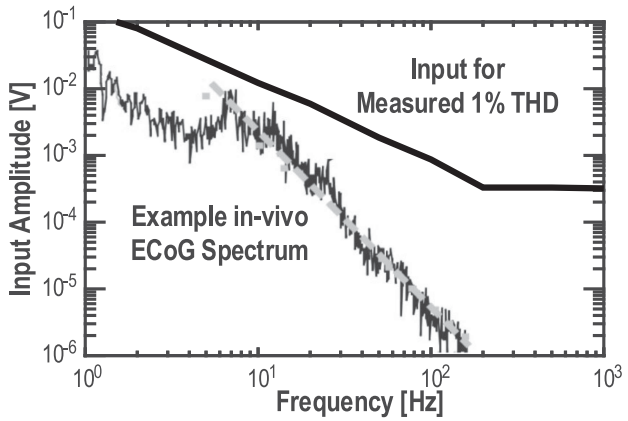


Fig. 17. RMS input amplitudes causing 1% Total Harmonic Distortion, measured with single-tone sinusoids across frequency for ECoG recording. Overlaid with a typical ECoG PSD (2kS/s) adapted from [27].

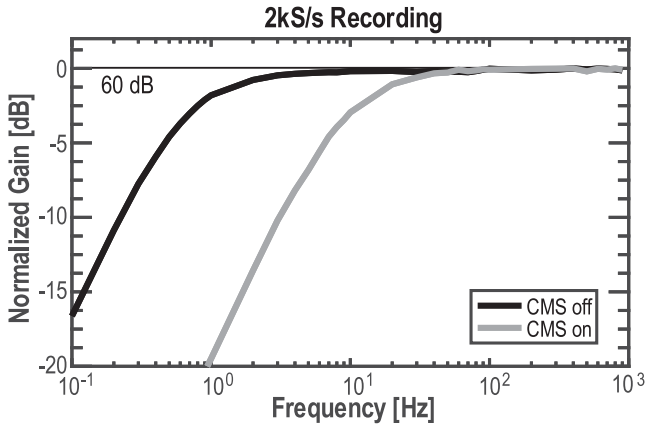


Fig. 18. Measured full signal chain transfer functions for ECoG (2kS/s).

the input impedance decreases from 92 MΩ to 9.2 MΩ. This decreased input impedance primarily impacts the low-frequency voltage transfer, which as shown in the figure primarily impacts the Delta-band frequencies below 4 Hz. The remaining motivation for a high input impedance relates to common-mode to differential-mode conversion [39], which this CMS scheme already directly addresses.

Bench measurements of the CMS system are shown in Fig. 19(a). Without the CMS system, even small common-mode artifacts can substantially modulate the gain of the amplifier, which creates a nonlinear intermodulation product with the common-mode artifact and potentially sets the operating point of the amplifier in a highly nonlinear region. With CMS enabled, the gain remains very consistent until the complementary transmission-gate based switches of the multiplexer begin to enter the accumulation region. A 6% degradation of the gain near mid-range is observed due to the complementary switches employed at the MUX input. The linearity of these switches is sufficient for recording purposes, but is degraded in the presence of large voltage swings. This reduction in linearity could easily be corrected by bootstrapping the MUX switches, which could also be leveraged for increased voltage range [40], [41].

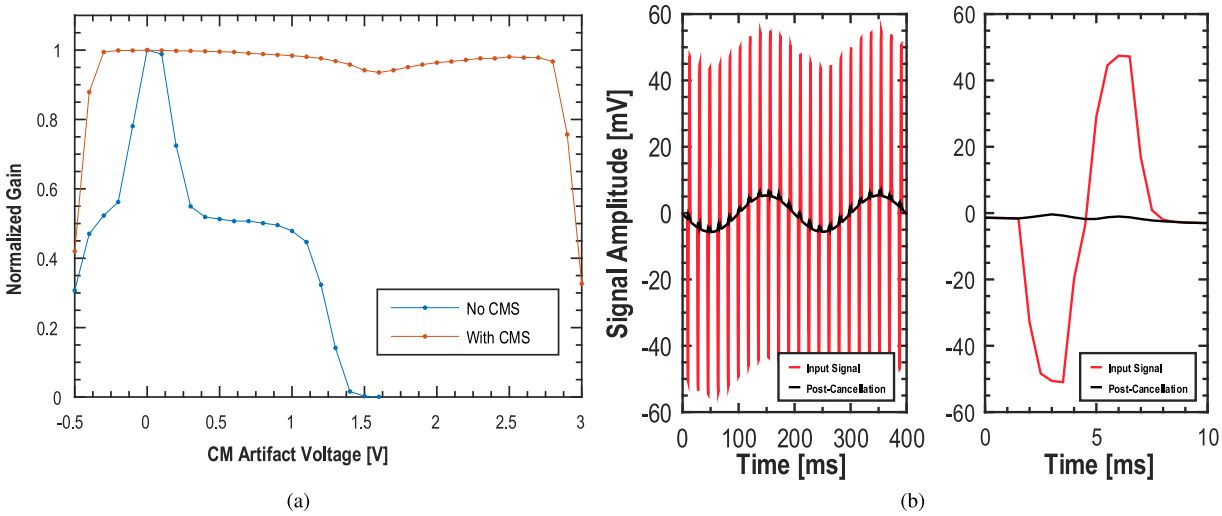
Although the proposed CMS architecture achieves a cancellation range of 2.5 V (Fig. 19), significantly higher than prior works [36], capacitive sampling adds noise at the input. Reducing this kT/C noise by increasing C_{IN} would further reduce input impedance and increase area. To measure the input-referred noise impact of CMS, we continuously enabled the feature and measured the noise performance in this worst-case condition. The input-referred noise was measured to be 14.4 μV, consistent with kT/C noise from a C_{IN} of 50 pF at each input.

In real-world applications, CMS is only enabled during stimulation pulses. For duty cycle, D, the resulting impact on input referred noise can be approximated as: $\overline{v_{in,eff}} = 1.66\mu V + D \times 12.7\mu V$. A typical D value of 4% [42] yields input referred noise of $2.17\mu V$, resulting in a NEF of 2.89. This expression is applicable for applications that rely on frequency-domain analysis. If low-noise measurement of time domain data during stimulation events is required, another method must be used.

Differential-mode suppression is demonstrated in Fig. 19(b). An H-bridge stimulator [43] in combination with a signal generator to create a test signal with a realistic artifact. A 5 Hz, 10 mV sinusoid with a ±54 mV biphasic differential stimulation artifact is input to the system and suppressed at the amplifier inputs, demonstrating 46 dB of artifact suppression before the amplifier inputs. This number is limited by the step size of the input DAC, but further post-processing suppression is possible because 46 dB of suppression brings the artifact into the linear range of the signal chain.

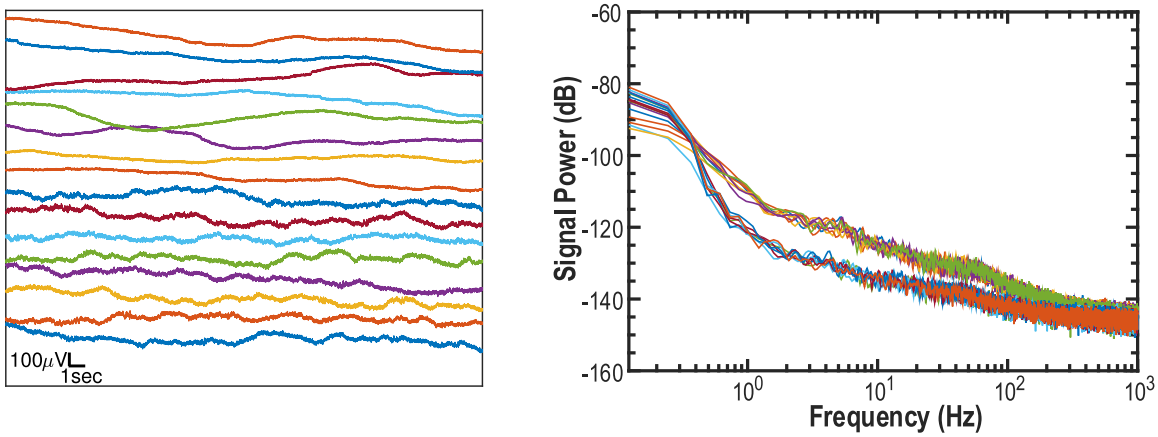
B. In-Vivo Measurements

In-vivo measurements were taken from two hemispheres of a chronically implanted μECoG array in a sedated macaque. Fig. 20 demonstrates operation on 16 channels simultaneously using the time-division multiplexing implemented on chip. Both



(a) (b)

Fig. 19. Bench measurements of the CMS (a) and DMS (b) systems. (a) shows the CMS system swept over CM artifact voltage levels both with and without CMS enabled. The CMS largely mitigates gain variation compared to the nominal case. (b) shows a 10 mV sinusoidal 5 Hz signal with a ±54 mV biphasic stimulation artifact (differential) before and after front-end suppression.



(a) (b)

Fig. 20. Simultaneous 16-channel in-vivo measurements from an implanted μECoG array in a sedated non-human primate, shown in the (a) time domain and (b) frequency domain.

the time- and frequency-domains are shown for clarity. Signal amplitude varies significantly between hemispheres, as apparent in both plots. High-quality recordings with a 1 kHz bandwidth were obtained, showing low-frequency behavior consistent with suppressed brain activity under sedation.

In Fig. 21, the common- and differential-mode suppression techniques are demonstrated in-vivo. Fig. 21(a) shows the common-mode suppression technique across 3/64 channels. The buffered common-mode voltage at the amplifier inputs is measured using an oscilloscope with and without the suppression enabled. When suppression is disabled, large common-mode variation is seen due to sampling of stimulus artifacts on the 3/64 channels that are connected. When enabled, the common-mode voltage is stabilized and is always within 10 mV of the nominal common-mode input voltage. Fig. 21(b) shows the behavior of the differential-mode suppression system. While the suppression capability is limited by the coarseness of the input DAC, as discussed in Section III above, we demonstrate that the amplifier does not saturate when suppression is enabled. This allows for linear post-processing of the signal after digitization.

C. Comparison to State-of-the-Art

Table I compares the results from this chip to other recent works representing the state-of-the-art in cortical biopotential acquisition. This work performs comparably to the literature along all metrics and scales well with frequency without a major performance impact. Our primary contributions include the CMS technique for common-mode artifacts and full signal-chain multiplexing which improves the channel density by a factor of >2x. We also demonstrate excellent crosstalk performance because of the auto-zero technique and the lack of parasitic paths between channels past the multiplexer inputs, which are next to the individual pads.

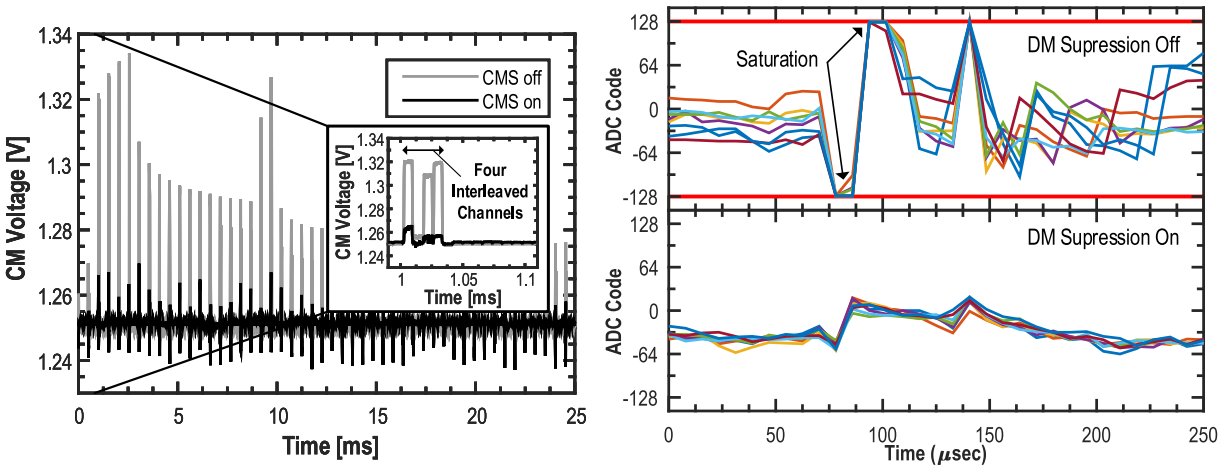


Fig. 21. In-vivo recordings in the presence of artifacts for common- (a) and differential-mode (b). (a) shows the voltage at the input to the amplifier with and without common-mode suppression. (b) shows the reconstructed output waveform with and without front-end suppression. Measurements were performed with 300 μA biphasic stimulation in PtIr microwire electrodes adjacent to recording electrodes, creating 100 mV Pk-Pk stimulus artifact at the recording inputs.

TABLE I
PERFORMANCE COMPARISON OF PROTOTYPE WITH OTHER BIOPOTENTIAL AMPLIFIERS

	JSSC'15 [11]	VLSI'15 [32]	JSSC'14 [44]	ESSCIRC'16 [45]	This Work
Technology	65 nm	0.18 μm	0.18 μm	0.13 μm	65 nm
Supply Voltage (V)	0.5	0.5, 1	1.8	1.2, 1.8	0.5, 2.5
DM Artifact Suppression	—	Yes[1]	—	—	Yes[2]
CM Artifact Suppression	—	—	—	—	Yes[3]
Multiplexing	—	—	ADC	Shank	Complete
Number of Channels	64	8	8	768	64
Channel Area (mm^2/ch)	0.025	0.17	N/A	0.12[4]	0.0023
Power per channel (μW)	2.3	0.33	56.7	3	2.98
Input Referred Noise (μV_{rms})	1.2	3.05	5.2[5]	12.4[5]	1.66[6]
Noise Efficiency Factor	4.76	1.63	1.77[5]	8.5[5]	2.21[6]
AFE Bandwidth (Hz)	1-500	1-2k	0.1-700	0.5-8k	1-1k[7,8]
Input Impedance	28MΩ @ 8kHz	—	—	13.27MΩ @ 20kHz	92MΩ @ 2kHz
ADC Resolution / ENOB	15b / —	10b / —	10b / 9.57b	10b / —	8b + 8b / 15.7b[9]
CMRR (dB)	88	—	—	—	76
PSRR (dB)	67	—	—	—	82
Peak-to-Peak Range (mV)	100	—	—	—	110
Crosstalk (dB)	-85	—	—	-63	-92

[1] Least-mean squares algorithm operating on a DAC at the amplifier inputs.
[2] Serial chip input to DAC at amplifier inputs.
[3] Switched-capacitor offset correction scheme.
[4] Full Probe.
[5] Amplifier Only.
[6] For nominal recording operation, not CMS.
[7] DC coupled to electrode.
[8] High-pass corner is 10 Hz during CMS.
[9] At low-frequencies (frequency dependent).

VI. CONCLUSION

We have demonstrated a delta-encoded digital feedback biopotential amplifier with both CM and DM artifact suppression capabilities. The delta-encoding architecture enables a large dynamic range using low-resolution data converters and enables high-density multiplexing to reduce area. The resulting prototype performance is comparable to the state-of-the-art with up to a 2x reduction in area per channel in the 64 channel configuration. Future work includes integrating this recording architecture with high-voltage compliance stimulation and a digital back-end capable of adaptive artifact cancellation computations. The architecture itself could be improved with increased CDAC resolution (for more differential artifact suppression) and introduction of a servo loop into the common-mode cancellation scheme to maintain a high input impedance.

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