A Dual-Mode V-Band 2/4-Way Non-Uniform Power-Combining PA with +17.9-dBm P_{sat} and 26.5-% PAE in 16-nm FinFET CMOS

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***Abstract*—This paper presents the design of a dual-mode V-band PA with efficiency enhancement at power back-off via load modulation. The design utilizes a reconfigurable 2/4-way non-uniform power combiner to enable two discrete modes of operation – full power and back-off power. The 2-stage PA achieves a peak gain of 21.4dB with a fractional BW of 22.6% (51-64GHz). At 65GHz, the PA has a P_{sat} of +17.9dBm with an OP_{1dB} of +13.5dBm and a peak PAE of 26.5% in full-power mode. In back-off power mode, the measured P_{sat}, OP_{1dB}, and peak PAE are +13.8dBm, +9.6dBm, and 18.4%, respectively. The PAE is enhanced by 6-% points at 4.5-dB back-off. The PA is capable of amplifying a 6-Gb/s 16-QAM modulated signal with an EVM_{rms} of -20.7dB at an average P_{out}/PAE of +13dBm/13.6%, respectively. This PA is implemented in 16-nm FinFET, occupies a core area of 0.107mm^2, and operates under a 0.95-V supply.**

***Keywords*—power amplifiers, millimeter wave circuits, power combining, load modulation, FinFET.**

I. Introduction

The demand for increased data rates of various wireless applications has driven radio communications to operate with increased bandwidth (BW) in millimeter-wave (mm-wave) bands while reducing form factor and cost. As CMOS technologies continue to scale-down which enables high-speed operation and smaller devices, the design of efficient, wideband PAs with high output power remains a major challenge for the development of fully-integrated system-on-chips (SoCs). Furthermore, although several mm-wave CMOS PAs have been published [1]–[4], only a few of them were implemented in FinFET (FF) CMOS [3][4], which is a prime candidate technology for implementing next-generation mm-wave SoCs.

The output power and efficiency of PAs are key performance metrics as PAs often consume the majority of power in radio transceivers. Moreover, a desirable exists to support spectrally efficient modulation methods that exhibit high peak-to-average power ratio (PAPR). As a result, several techniques have been proposed to enhance efficiency at power back-off (PBO), thereby improving average efficiency when transmitting high PAPR signals. Mm-wave Doherty PAs show impressive back-off efficiencies, with one implementation at 60GHz exhibiting a peak PAE of 26% with an enhanced PAE of 16.6% at 7-dB PBO [1]. However, the large footprint associated with Doherty PAs complicates SoC integration. In addition, Doherty PAs suffer from narrow BW imposed by the λ/4 impedance rotation on the aux path. While wideband mm-wave PAs have been demonstrated [2][3], their back-off efficiencies typically drop by more than half at PBO levels necessary for high-order modulations. As such, it is of interest to develop compact, wideband, high-output-power PAs in deeply-scaled CMOS with enhanced efficiency at PBO.

This paper presents a wideband reconfigurable 2/4-way power-combining PA implemented in 16-nm FinFET CMOS. The PA can be configured in two output power modes: full power (FPM) and back-off power (BPM). The PA applies a load modulation technique similar to [5] for efficiency enhancement in BPM which is further improved by utilizing a proposed non-uniform power combiner. Moreover, a load modulation switching scheme is proposed which minimizes the variation in frequency response between the two modes and improves performance in BPM.

This paper is organized as follows. Section II discusses the architecture and design of the proposed PA. Section III presents measurement results. Section IV concludes the paper with a comparison to state-of-art CMOS PAs.

II. Circuit Implementation

A. PA Architecture

Fig. 1 depicts the PA topology. It consists of two stages of amplification, an input matching transformer, interstage power splitters, and a reconfigurable 2/4-way series-parallel power combiner at the output. In FPM, all gain stages are ON with SW1-4 open, thereby placing the PA in its highest P_{out} mode. In BPM, DRV1-2 and PA2-3 are ON, while PA1 and PA4 are OFF and SW1-4 are closed. In this configuration, the PA output stage becomes a 2-to-1 combiner and ideally operates at 6-dB PBO as compared to FPM, assuming uniform power combining (all transformers are 1:1).

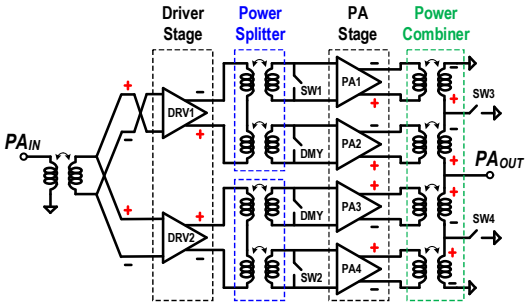


Fig. 1. The 2-stage PA architecture with a reconfigurable 2/4-way series-parallel power combiner. Polarities of the gain stages are shown.

Fig. 2 shows the detailed transistor-level schematic for the bottom-half of the PA. Capacitively-neutralized differential pairs are used in all gain stages for an increased G_{max}. The capacitances are obtained by overlapping drain and gate routing in layout, similar to [4]. A common-mode source degeneration

inductor of 145pH is placed in the driver stage for better common-mode stability and common-mode rejection, as the driver stage contributes to the majority of gain and is more susceptible to oscillation.

A high-k (k=0.6) transformer is used for the input matching network for minimal loss, while low-k (k=0.3) transformers are used for the interstage power splitters to enhance the bandwidth [6]. Series power splitting is utilized for two reasons. First, the resulting transformer *inductance ratio* (1.6:1) is much lower than that of a parallel splitter (6.5:1), thereby resulting in lower transformer insertion loss. Secondly, series power splitting enables the usage of shunt switches at the front of PA1 and PA4 to disable these paths in BPM (Fig. 1). In contrast, a parallel power splitter would require a large OFF impedance from PA1 and PA4, which is hard to achieve at mm-wave frequencies due to large input capacitance associated with the PA devices. As such, the shunt switch in a series splitter leads to reduced loading of the OFF paths in BPM (PA1 and PA4).

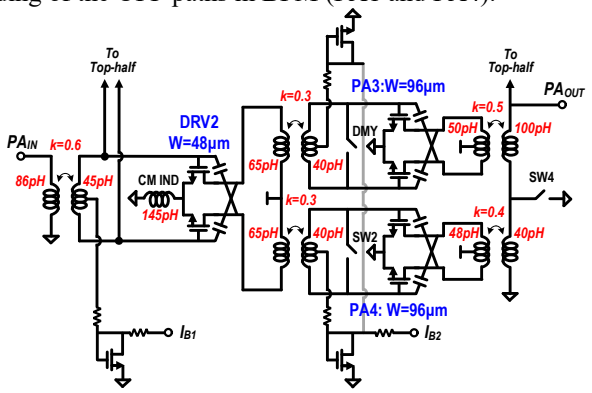


Fig. 2. Detailed transistor-level schematic for the bottom-half of the PA.

B. Non-Uniform Power Combining and Load Modulation

The PA employs a 2/4-way series-parallel power combiner with non-uniform turns ratios for the transformers. Using non-uniform turns ratios improves the PA performance in BPM due to the reduced change in PA load impedance between the two power modes as described next.

Fig. 3 shows the conceptual diagram of a non-uniform power combiner with the 50-Ω antenna load modeled as two 100-Ω resistors in parallel. The non-uniform turns ratios of transformers for PA1, PA2, PA3, and PA4 are 1:1, 1:$\sqrt{2}$, 1:$\sqrt{2}$, and 1:1, respectively. Fig. 3 (a) shows the configuration of the combiner in FPM. When all the paths are ON, the voltages across each transformers' secondaries are V_{in}, $\sqrt{2}V_{in}$, $\sqrt{2}V_{in}$, and V_{in}, respectively, assuming each PA outputs the same V_{in}. Moreover, the currents flowing through each transformer's secondary are equal. As a result, each of the 100-Ω terminations are distributed as 59-Ω and 41-Ω impedances across the secondaries of the transformers of PA2/PA3 and PA1/PA4, respectively. These impedances are then transformed, via the respective turns ratios, to 29Ω and 41Ω loads which are presented to each PA device. In BPM, PA2 and PA3 will see a load impedance of 50Ω as shown in Fig. 3 (b), where PA1 and PA4 are OFF and SW3 and SW4 are ON.

By contrast, with the conventional uniform power combining, the impedance presented to each PA is 50Ω/100Ω in FPM/BPM. Now, assuming the impedance presented to the PA in FPM is its optimal load, this impedance should also be presented to PA2 and PA3 in BPM for optimal performance. Therefore, by applying non-uniform power combining, the impedance change between FPM and BPM is reduced to 1.72x (29Ω:50Ω), as compared to 2x (50Ω:100Ω) in uniform combining, and improves the output power and efficiency in BPM.

Note that the impedance change between FPM and BPM can be further minimized by choosing proper combining turns ratios. For instance, the turns ratios of 1:1, 1:$\sqrt{3}$, 1: $\sqrt{3}$, and 1:1 can reduce the impedance mismatch to 1.57x (21Ω:33Ω), thereby improving the P_{sat} and PAE in BPM further. However, implementing a turns ratio of 1: $\sqrt{3}$ (or 1:3 *inductance ratio*) is challenging and exhibits higher loss at mm-wave frequencies.

Lastly, it is worth noting that the back-off efficiency can also be improved by reducing the drive strength of each PA while simultaneously adjusting the load line [7]. In this scenario, an *increase* in the impedance presented to the PA for BPM is desirable; however, this is not the case for this design since the drive strength of each PA remains constant between two modes.

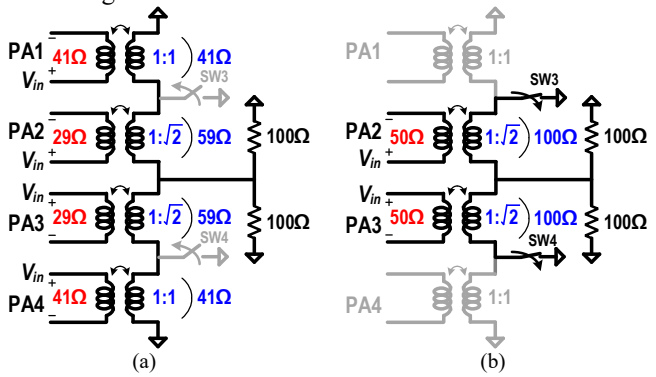


Fig. 3. Conceptual diagram of non-uniform power combining. The impedances seen from each PA stage in (a) FPM and (b) BPM.

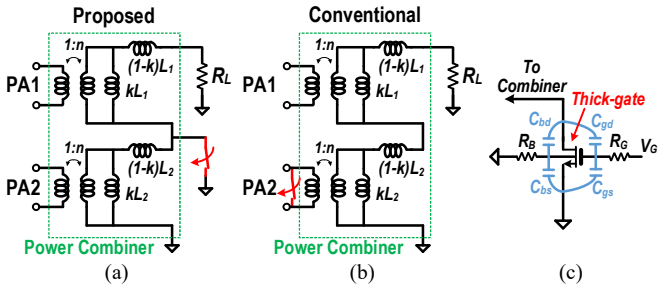


Fig. 4. Comparison of implementing the switch at transformer's (a) secondary and (b) primary. (c) The switch architecture for high voltage swing.

C. Proposed Switching Scheme

The proposed load modulation is implemented by placing the switch at the transformer's secondary to eliminate both the coupling and leakage inductances for the OFF path of the combiner, as seen in Fig. 4 (a). The equivalent circuit model of the power combiner is shown which is composed of two transformers and a switch. Assuming the switch is ideal, the switch can short both the coupling inductance, kL_2, and the leakage inductance, $(1\text{-}k)L_2$ to ground. In contrast, Fig. 4 (b) shows a commonly used technique for implementing load

modulation which places a shunt switch at the outputs of the PAs (transformer's primary). In this configuration, the switch can short kL_2 term, but not the $(1\text{-}k)L_2$ term. As a result, the leakage inductance becomes an undesired reactance in series with the secondary of the ON path to ground, thereby degrading the performance and frequency response in BPM. This effect is more severe at mm-wave frequencies where the transformer's coupling factor is usually lower and thus leakage inductance is non-negligible.

The switches are implemented using thick-oxide devices with both gate and bulk terminals biased through kΩ-order resistors, R_B and R_G, to allow high voltage swing, see Fig. 4 (c). This technique is commonly used in T/R switch designs [8].

The power combiner is implemented using the ultra-thick metal (UTM) and RDL layers of the process. The simulated insertion loss of the power combiner is 1.1dB in FPM.

III. Measurement Results

This PA is fabricated in16-nm FinFET CMOS technology and operates from a 0.95-V supply. The die photo is shown in Fig. 5. The core area of the PA is 0.107mm^2.

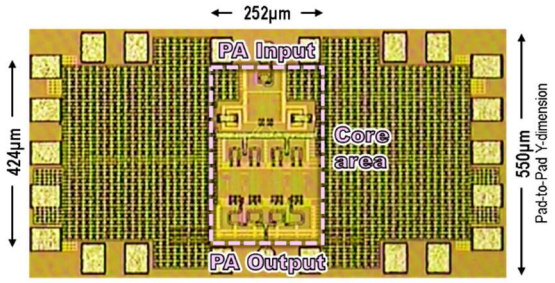


Fig. 5. The die photo of the PA in 16-nm FinFET CMOS.

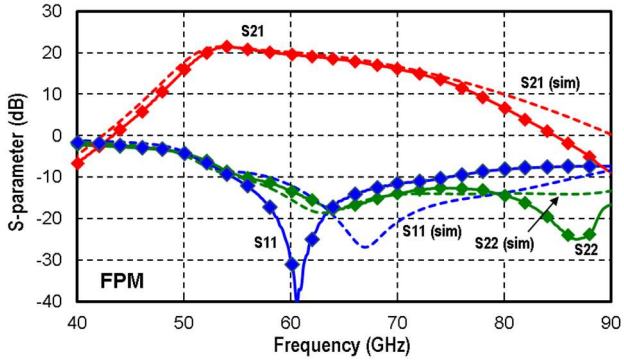


Fig. 6. Measured vs. simulated S-parameters in FPM.

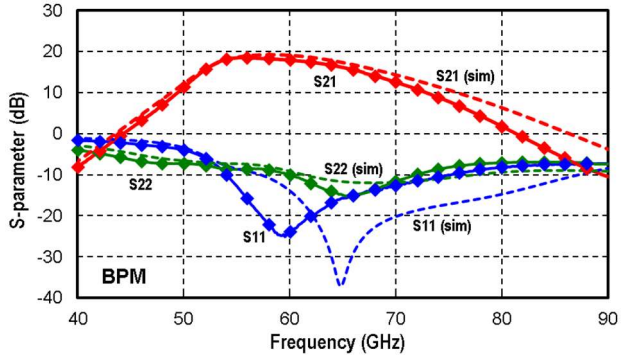


Fig. 7. Measured vs. simulated S-parameters in BPM.

The measured and simulated S-parameters in FPM and BPM are shown in Fig. 6 and Fig. 7. In FPM, the PA achieves a peak gain of 21.4dB at 54GHz and a 13-GHz BW (51-64GHz), see Fig. 6. In BPM (Fig. 7), the PA achieves a peak gain of 18.5dB at 55GHz and a 14-GHz BW (52-66GHz). S_{11}<-5.5dB and S_{22}<-5.2dB are achieved with S_{12} <-45dB (not shown) over the band of interest. The results show good agreement between measurements and simulations for S_{21} and S_{22} while the measured S_{11} null is shifted ~6GHz lower.

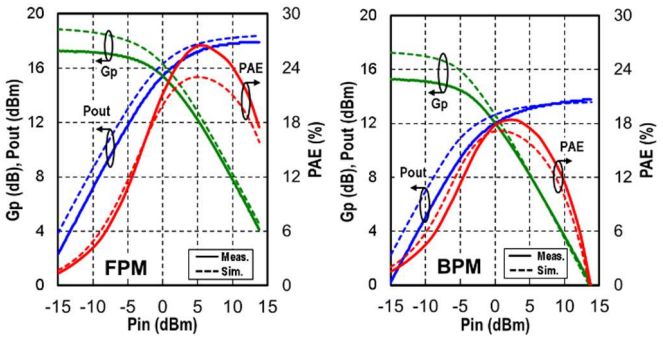


Fig. 8. Measured vs. simulated large-signal performance (G_p, P_{out}, and PAE) vs. P_{in} in (a) FPM and (b) BPM at 65GHz.

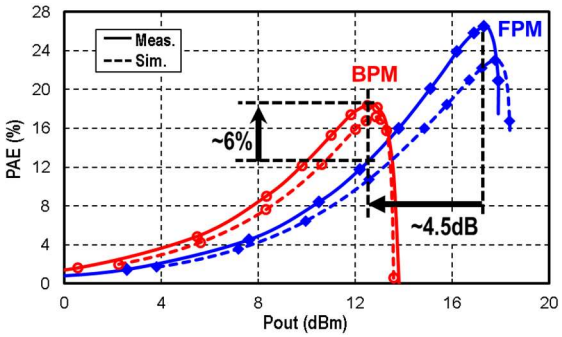


Fig. 9. Measured vs. simulated PAE vs. P_{out} in FPM and BPM at 65GHz.

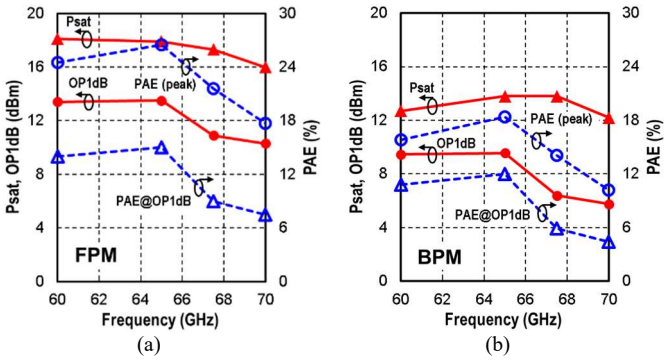


Fig. 10. Large-signal measurements across 60-70GHz in (a) FPM and (b) BPM.

Fig. 8 shows the measured and simulated large-signal performance at 65GHz. In FPM, the PA delivers a P_{sat} of +17.9dBm with a +13.5-dBm OP_{1dB} and a 26.5-% peak PAE. In BPM (Fig. 8b), the measured P_{sat}, OP_{1dB}, and peak PAE are +13.8dBm, +9.6dBm, and 18.4%, respectively. A reasonable agreement is achieved between measurements and simulations.

Fig. 9 plots the measured and simulated PAE curves vs. P_{out} at 65GHz. In FPM, the PA can deliver an output power of 12-18dBm with >12-% PAE. For output powers below +12dBm,

the PA can be switched to BPM for an enhanced efficiency. The PAE is ~6-% points higher in BPM over an output power range of 8-12dBm.

Fig. 10 shows key large-signal performance vs. frequency, including P_{sat}, OP_{1dB}, peak PAE, and PAE at OP_{1dB}. The PA maintains good performance within the bandwidth of 60-70GHz. The lowest frequency of large-signal test is limited to 60GHz due to the band-limited test setup. However, the PA is expected to still maintain good performance down to 52GHz since it is within the 3-dB BW.

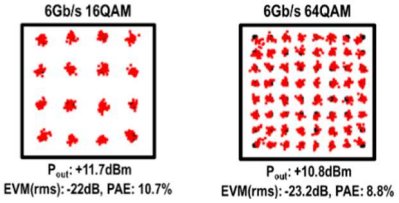
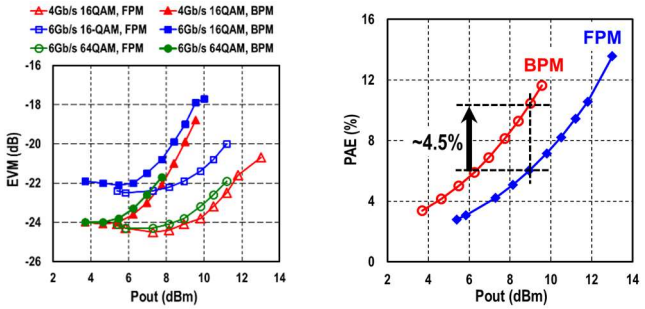


Fig. 11. Measured constellations for 6Gb/s 16QAM and 64QAM at 65GHz.



(a) (b)

Fig. 12. Measurements of modulated signals. (a) EVM_{rms} vs. P_{out} for various modulations. (b) PAE vs. P_{out} with 4Gb/s 16QAM modulation in FPM and BPM.

The PA was also tested with modulated signals at 65GHz. Fig. 11 shows constellations for two test cases. The PA achieves an average EVM_{rms} of -22dB/-23.2dB with an average P_{out} of +11.7dBm/+10.8dBm and an average PAE of 10.7%/8.8% for 6Gb/s 16QAM/64QAM, respectively. Fig. 12 (a) shows the EVM_{rms} vs. P_{out} in FPM and BPM for various modulations. Note that the test setup is the same as in [3], however, these measurements are at a lower frequency. As a result, mitigation of spectrum aliasing and noise folding due to LO harmonics of the VDI converters could not be done due to the lack of a waveguide BPF in this band. This is believed to be the cause of a degraded test setup EVM_{rms} floor of -22dB/-24dB for 6Gb/s 16-/64-QAM, respectively. Therefore, the true PA performance is expected to be better than what is reported. Fig. 12 (b) plots the PAE vs. P_{out} in FPM and BPM which is similar to Fig. 9, but in this case it is for modulated signals at 65GHz. As seen in the figure, the average PAE can be improved by 4.5-% points at the P_{out} of +9dBm when switched to BPM while maintaining reasonable EVM_{rms} of -20dB for 4Gb/s 16QAM modulation.

IV. Conclusion

This paper presented the design of a dual-mode V-band 2/4-way non-uniform power combining PA. Back-off efficiency enhancement is demonstrated by switching the PA mode. Table 1 compares the PA's performance with prior-art. The PA achieves back-off efficiency enhancement on par with prior-art while obtaining high gain and a large fractional bandwidth. This demonstrates the viability of high-power PA design in FinFET, enabling development of mm-wave SoCs for next-gen systems.

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Table 1. Comparison to Prior-Art Mm-wave Power Amplifiers

	[1]	[2]	[4]	[3]	This Work	
Technology	45nm SOI	40nm	14nm FF	22nm FF	**16nm FF**	
Topology	Doherty	4-Way PwrComb	3-Stage CS	2-Stage CS	**2/4-Way Non-Uni Pwr Comb**	
V_{DD} (V)	2	0.9	1	1	**0.95**	
Frequency (GHz)	60	80	71	74	**65**	
Peak Gain (dB)	12.9	18.1	16.7	16.6	**21.4**	**18.5**
Frac. BW (%)	10[1]	19.1	10.4	32	**22.6**	**23.7**
P_{sat} (dBm)	20.1	20.9	7.4	12.8	**17.9**	**13.8**
OP_{1dB} (dBm)	19.3	17.8	2	5.7	**13.5**	**9.6**
Peak PAE (%)	26	22.3	8.9	26.3	**26.5**	**18.4**
PAE @ OP_{1dB} (%)	25.9	10[1]	4.8	11.6	**15**	**12**
Enhanced PAE @ PBO[6] (%)	18.5[1,5] @4.5dB PBO	-	-	-	**18.4[5] @ 4.5dB PBO**	
Core Area (mm^2)	0.76	0.19	0.1	0.054	**0.107**	

	[1]	[2]		[3]			This Work		
Frequency (GHz)	65	73		75			**65[3]**		
Modulation (M-QAM)	64	16	16	16		64	**16**		**64**
Data Rate (Gb/s)	3	3	3	3	6	9	**4**	**6**	**6**
RMS EVM (dB)	-23.1	-20[3]	-25[3]	-26[2]	-26[2]	-28[2]	**-20.7[2,3]**	**-21.6[2,3]**	**-21.9[2,3]**
Avg. P_{out} (dBm)	13.8	-	11.9	5.6	5	1.3	**13**	**11.8**	**11.2**
Avg. PAE (%)	15.7	-	4.5[1,4]	11	10	5	**13.6**	**10.6**	**9.4**

[1] Estimated from figures
[2] w/ equalizer on
[3] Limited by setup
[4] Tested at 80GHz
[5] Tone-based tests
[6] PBO from P_{sat}