A Bidirectional Brain Computer Interface with 64-Channel Recording, Resonant Stimulation and Artifact Suppression in Standard 65nm CMOS

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***Abstract*— A single-chip bidirectional brain-computer interface (BBCI) enables neuromodulation through simultaneous neural recording and stimulation. This paper presents a prototype BBCI ASIC including a 64-channel time-multiplexed recording front-end, 4-channel high-voltage compliant resonant-stimulator and electronics to support concurrent multi-channel differential- and common-mode stimulus artifact cancellation. A cascaded charge pump-based stimulation driver provides +/-11V compliance using 1.2V devices. High-frequency (~3GHz), self-resonant clocking is used to reduce capacitor area while suppressing associated switching losses. A 32-tap LMS-based digital adaptive filter achieves 60-dB artifact suppression, enabling simultaneous neural stimulation and recording. The entire chip is powered by 2.5/1.2V supplies, dissipating 205µW in recording, 142µW in the cancellation back-end, and 31% DC-DC efficiency in the stimulation drivers, each with a maximum output power of 24mW. This 4mm² neural interface chip was implemented in 65nm 1P9M LP CMOS.**

Keywords— brain computer interfaces, neural stimulation, time-division multiplexing, artifact cancellation

I. Introduction

Future realizations of small-form factor, ultra-low power and bidirectional brain-computer interfaces (BBCI) will radically impact both scientific and clinical applications, including study of brain function and treatment of neurological disorders such as Parkinson's disease, depression, obsessive-compulsive disorder and reanimation of damaged neural tissue [1]. The integration of complete BBCI implantable systems in CMOS will allow the combination of recording, stimulation, energy harvesting and communication with sophisticated digital computation/signal processing for closed-loop neural modulation using minimally invasive implantable devices. However, critical integration challenges remain, namely: 1) high voltages required by most stimulator applications exceed the voltage limits of advanced, scaled CMOS technologies, 2) electrical stimulation creates in-band artifacts that are several orders of magnitude larger than signals targeted by neural recording front-ends (~100mV vs ~100µV). Recent implementations address these problems by migrating to high-voltage-compliant CMOS processes for stimulation [2,3] where large core devices are less suited for digital integration, overdesigning the recording front-end dynamic range to accommodate large stimulus artifacts [3], or using mixed-signal feedback in the front and back-ends for artifact suppression [3-7]. This work achieves high voltage compliance (±11V) with stacked circuits in low-voltage scaled CMOS, in addition to exploiting digital time-division multiplexed adaptive feedback to enable recording during stimulation without the need to enhance the sensing front-end dynamic range. The resulting monolithic 65nm CMOS chip includes all front-end components to allow simultaneous 64-channel recording and 4-channel stimulation for BBCI-clinical applications.

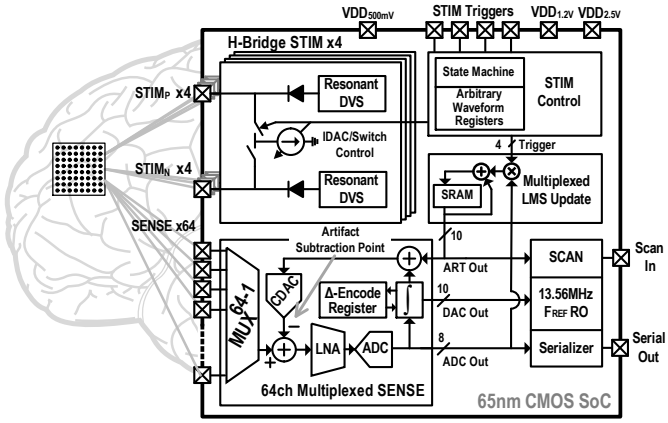

Fig. 1 Functional block diagram of the BBCI chip architecture.

The implemented system contains four integrated differential stimulators which are digitally programmable for current waveforms with a peak amplitude of 2mA. Dynamic voltage supplies generate up to ±11V to drive sink-regulated current into the electrode-tissue load. A time-multiplexed, delta-encoded recording front-end [7] concurrently records 64 channels at 2kS/s, using a multiplexer to route signals to a common recording chain, thus sharing an input capacitive DAC (CDAC), a front-end amplifier, and a SAR ADC between channels. The digital back-end contains an adaptive filter-based artifact canceler that uses recording output and stimulator cues, to converge to the waveform of unwanted stimulus artifacts by applying a cancellation signal at the recording inputs. Fig. 1 shows the full system architecture.

II. Resonant H-Bridge Stimulator

This work implements an area-optimized version of the high-power H-bridge stimulation topology presented in [8]. Multi-stage charge pumps generate ±12V (limited by on-chip diode

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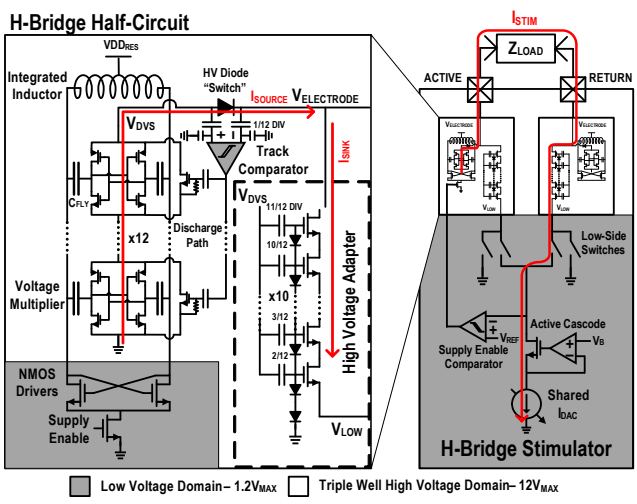

Fig. 2 Schematic of charge-pump based stimulator with stacked, high-voltage compliant driver.

breakdown) for sink-regulated current pulses through a shared current DAC (IDAC). High-voltage supplies in the 1.2/2.5V 65nm CMOS process require use of a diode as a high-voltage switch. The maximum output swing is limited to ±11V by the diode drop. When a H-bridge half circuit is sinking current, a comparator-based feedback loop discharges the charge pump to ensure that the diode "switch" is reverse-biased and "off." While one side of the H-bridge supplies voltage across the electrode-tissue interface, current flows from the return-side electrode through a high-voltage adapter (HVA) into the stimulation IDAC, as shown in Fig. 2. The HVA is a multi-stage cascode operating as a current buffer, protecting the 1.2V IDAC from large voltages seen at the stimulator-electrode interface. During stimulation, a second comparator-based feedback loop maintains sufficiently high voltage across the load to ensure all IDAC devices remain in the saturation region. In addition, by adaptively scaling the supply voltage as needed during the delivery of a stimulation pulse, the feedback loop ensures the charge-pump-based supplies only dissipate as much power as needed. An active cascode using a high-gain op-amp provides a high IDAC output impedance (600 MΩ simulated).

The maximum stimulator output current is proportional to the switching frequency and C_{FLY}, the charge pump flying capacitance. However, C_{FLY} dominates stimulator area, and increasing the clock frequency to shrink C_{FLY} increases parasitic energy loss. To suppress this loss, integrated spiral inductors are used to create a differential resonant tank around the switched-capacitor charge pumps (Fig. 2). Resonance recovers a significant portion of the reactive energy lost to parasitic capacitance. Large, cross-coupled NMOS devices generate negative impedance to compensate for resistive losses in the LC-tank. Oscillator power is applied through an inductor center tap set at VDD_{RES}, allowing a clock swing of $2 \cdot VDD_{RES}$. Compared to prior work with charge pumps clocked at 100MHz [8], this architecture achieves similar losses while operating at 3GHz. The higher resonant switching frequency reduces overall charge pump area by 6x, including the additional integrated 200pH inductors.

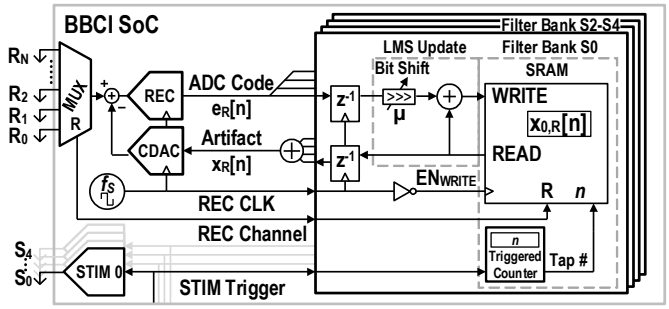

Fig. 3 Digital artifact cancellation adaptation implementation details.

All stimulator control is integrated on chip with a scan-configurable state machine. Stimulation pulse timing and amplitudes are pre-programmed and triggered by digital pad inputs. The stimulator provides support for programmable current waveforms to enable current neuroscience inquiry into the impact of non-traditional stimulation techniques, as demonstrated in Fig. 5. After stimulation, the tracking comparator is switched to compare residual voltage on the two electrode terminals. Charge is balanced with active discharge through the HVA and IDAC or a passive discharge resistor.

III. Artifact Cancellation

The time-multiplexed recording system in this work uses a 10-bit CDAC at the input of the transconductance amplifier to delta-encode low-frequency signal content which relaxes the required dynamic range of the single ADC, an improved version of the system in [7]. Adaptive differential digital artifact cancellation is performed through a separate feedback loop which supplies an output to the same CDAC at the recording channel input, as shown in Fig. 1.

Using an algorithm based on the least mean squared (LMS) error-update technique, the canceler learns a set of CDAC codes which map to synchronized artifact samples at each recording channel input and stimulator pair. The LMS update of canceller output $x_{S,R}[n]$ for stimulator S and recording channel R is as follows:

$$x_{S,R}[n+1] = x_{S,R}[n] + \mu\, e_R[n] \qquad (1)$$

The update error signal derives from the ADC output, given by:

$$e_R[n] = \Sigma_S\{x'_{S,R}(n/f_S - t_0) - x_{S,R}[n]\} \qquad (2)$$

Here, $x'_{S,R}(t)$ is the input artifact, quantized at the recording sampling frequency, f_S. The canceller outputs corresponding to each stimulator are summed before subtraction through the CDAC, this assumes that the artifacts from each stimulator linearly superimpose in the tissue. The update coefficient, μ, tunes the update step size. Decreasing μ increases loop stability and noise immunity while slowing convergence time.

The artifact computation hardware is also time-multiplexed for energy-efficient operation at 128kHz, amortizing leakage energy across multiple computations; six adders and four bit-wise shifts execute the entire LMS update algorithm for four stimulators and an arbitrary number of recording channels. The

canceler code sequence for each sense/stim. channel pair is stored in an on-chip static random-access memory (SRAM) and recalled for each filter tap. Signal flow and algorithm implementation is shown in Fig. 3. Each stim-sense channel combination has a dedicated memory bank, and each stimulator has a separate LMS update loop, rotating between recording channels. This allows the canceller to simultaneously learn different artifact shapes for each stimulator on a given recording channel, assuming the four stimulation pulses are uncorrelated. The four canceller outputs, each corresponding to one stimulator, are summed together before feeding into the front-end CDAC, allowing overlap between artifacts from different stimulation channels. The full analog cancellation range is the CDAC dynamic range (±125mV in this work).

Scaling the cancellation architecture to support more stimulation channels, or taps, only requires more memory. This implementation includes reconfigurable on-chip memory for 16 possible artifacts, each with 32 10-bit taps. The 5120-bit SRAM occupies 250µm x 300µm. The canceller can also interface with off-chip memory through source-synchronous serialized communication with an FPGA. Increased artifact cancellation depth can also be achieved with off-chip post-processing, given the canceller suppresses the artifact to within the dynamic range of the recording front-end.

IV. Measurement Results

The system was fabricated in TSMC 65nm LP 9M CMOS process and evaluated on the bench and in-vivo, using non-human primates. In-vivo measurements were taken with a chronically implanted Utah array (Blackrock Microsystems) in a ketamine sedated macaque monkey. The recording front-end dissipates 205µW across 64 channels, sampled at 2kS/s. Fig. 4 shows recorded evoked local field potentials at 16kS/s in the sedated macaque. Applying 20µA, 400µs-wide biphasic stimulation pulses at 10 pulses/s created individual responses, 1000 of which were averaged to create Fig. 4. This demonstrates the system's ability to record useful biopotentials while stimulating.

The resonant stimulation driver topology has a measured ±11V voltage compliance while driving up to 2mA of output current. The stimulator achieves 31% power efficiency while delivering maximum current/power output. During real stimulation pulses, the charge pumps are periodically enabled to maintain voltage across the electrode load, reducing current draw. Additionally, residual charge on capacitive electrodes from the first phase of a biphasic stimulation pulse is adiabatically re-used to sink current until the electrode is fully

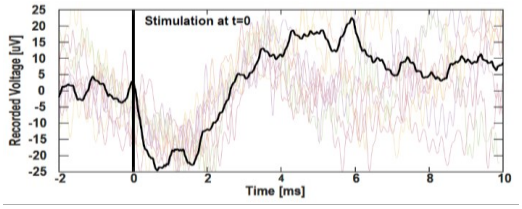

Fig. 4. Recorded in-vivo local field potentials evoked by 20µA stimulation pulses. Black trace is average of 1000 stimulation events, time aligned to place stimulation at time 0. Background exemplifies individual recordings.

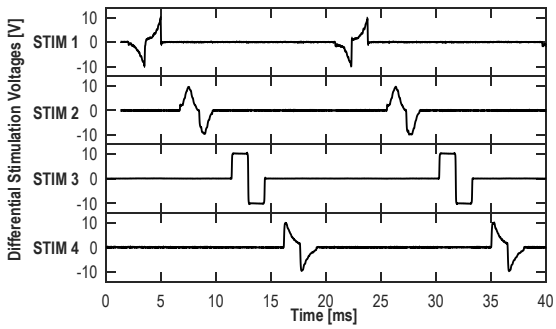

Fig. 5. Measured output waveforms of all four stimulators concurrently delivering peak currents of 2mA with equal 5kΩ resistive loads. Stimulator current waveforms programmed with the following shapes: 1) rising exponentials 2) half-sines 3) square waves 4) decaying exponentials.

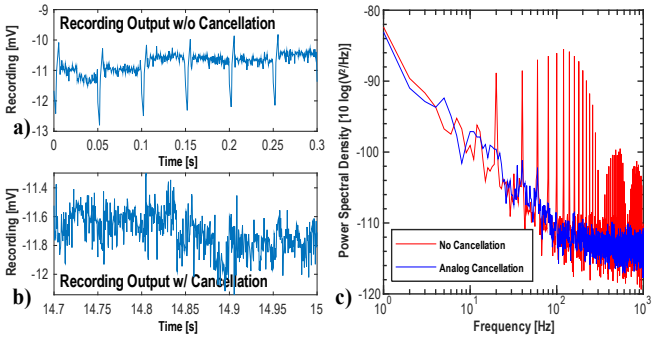

Fig. 6. Measured canceler performance (in-vivo). a) Input-referred recording in the presence of 35mV$_{Pk-Pk}$ artifact. b) Recording output after cancellation. c) Power spectral density of signal before and after cancellation.

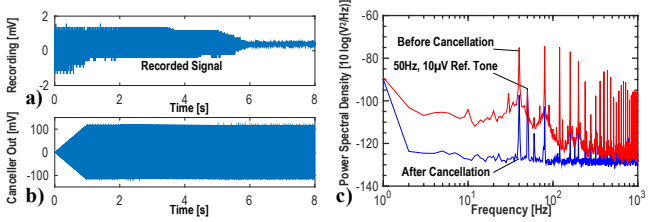

Fig. 7 Measured canceller bench performance. a) Input-referred recordings of a 50Hz 10µV tone in the presence of a 125mV$_{Pk-Pk}$ artifact. b) Canceller output signal. c) Recording signal power before and after cancellation, showing suppression of artifact spurs below the 10µVtest tone.

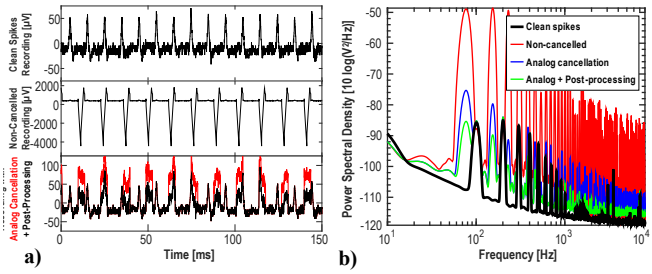

Fig. 8. a) Measured bench-top transient recordings demonstrating artifact cancellation at 16kS/s. Signals recorded before stimulation, during stim. without cancellation, and post-cancellation with and without post-processing. b) Power spectral density profiles for 16kS/s neural spike recordings in a).

discharged. A demonstration of multi-channel stimulation and the ability of this chip to deliver programmable current shapes is shown in Fig. 5.

Figure 6 shows artifact canceler performance in-vivo, demonstrating simultaneous stimulation and recording in the motor cortex of a sedated non-human primate. This measurement shows suppression of ±35mV differential artifacts to ±200µV, which maps to 44dB of on-chip cancellation. Limits to safe stimulation currents through the intracortical electrodes prevented exercising the full cancellation range. Fig. 7 shows an example of filter convergence and full-scale cancellation depth with bench recordings at 2kS/s. A ±125mV artifact was generated using the on-chip stimulator and combined with a 10µV, 50Hz test tone. The power spectral density (PSD) plot in Fig. 7c shows signal integrity after artifact cancellation on the bench.

Figure 8 shows bench testing of artifact cancellation at 16kS/s with artificial 50µV neural spikes at 100 spikes/sec generated using a bio-signal calibrator in the presence of ±125mV artifacts at 77 pulses/sec. Fig. 8a shows recording measurements under the following conditions: a) recording of transient signals without stimulation, b) with stimulation and artifact cancellation disabled, and c) artifact cancellation hardware enabled and post-processing for further cancellation. Fig. 8b shows the corresponding PSD of each signal, demonstrating the full 60dB of cancellation (30dBm in power); note: this does not include the additional 20dB of cancellation provided by back-end post-processing.

The entire test chip consumes 620µW while operating 64-channel recording, multiplexed artifact cancellation, and four stimulator back-ends. Stimulator output power is generated as needed by the on-chip resonant supplies. The full system occupies 2mm x 2mm total silicon area. A die photo of the fabricated 65nm LP test chip is shown in Fig. 9. A performance summary and comparison with prior art is found in Table I.

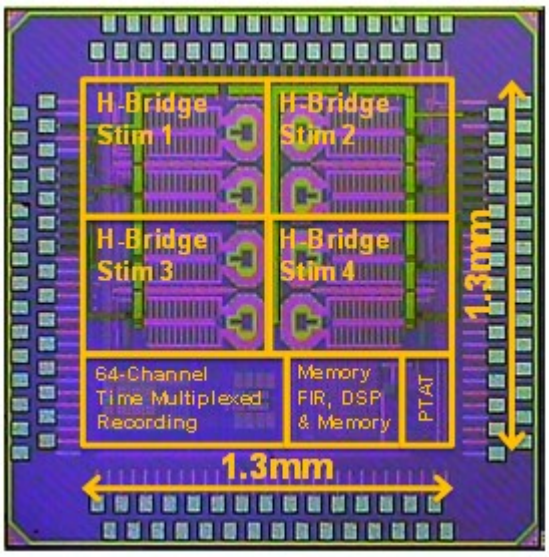

Fig. 9 Micrograph of fabricated 65nm test chip.

		ISSCC'16 [9]	VLSI'17 [2]	JSSC'17 [10]	SSCL'18 [4]	ISSC '18 [5]	ISSC'19 [6]	THIS WORK
System	Technology / Voltage	HV180nm 30V	HV180nm 30V	130nm 3.3V	65nm 2.5V	65nm 2.5V	130nm 3.3V	65nm 1.2/2.5V
	Artifact Suppression	None	Fast Recovery	None	77dB†	92dB†	Rail-Rail†	60dB DM 2.5V CM
	Total Power (mW)	18▼	0.7	1.07	-	-	-	0.62
	Chip Area (mm²)	25	11.52	4.98▲	5.14	1	11▲	4
	# of Ch.	16 SENSE 160 STIM	64 SENSE 4 STIM	64 SENSE 64 STIM	64 SENSE 2 STIM	16 SENSE	64 SENSE 64 STIM	64 SENSE 4 STIM
Stimulator	Voltage Compliance	±12V	±12V	3.1V (VDD)	Not Given	-	N/A E-Field	±11V
	Efficiency	From Supply	From Supply	From Supply	Not Given	-	From Supply	31%
	Area/Ch.	-	-	w/ Sense	Not Given	-	w/ Sense	0.36mm²
	Istim Shape	Square	Arbitrary	Arbitrary	Not Given	-	Arbitrary	Arbitrary
Recording	Area/Ch. (mm²)	-	-	0.013	0.18	0.024	0.018	0.0025
	Ch. Power (µW)	5.4	8	0.63	2.7	0.8	0.79	3.21
	IRN (μV_{rms})	7.68	1.12	1.13	8.2	0.73	2.1	2.9
	Bandwidth	7kHz	500Hz	500Hz	8.3kHz	5kHz	5kHz	Tunable <32kHz
	Max DM Range	-	100mV_{pp}	13mV_{pp}	200mV_{pp}	260mV_{pp}	Rail-Rail	110mV_{pp}
	CM Range	-	-	-	60mV	-	-	2.5V
	ADC Type	10b Pipeline	Oversampled SAR (10b)	$\Delta^2\Sigma$	-	$\Delta^2\Sigma$	$\Delta^2\Sigma$	8b SAR + Δ Encode (14b)

▼Includes stimulation power ▲Reported area includes Wireless Power/TX or DSP † AFE dynamic range

Table I State-of-the-art comparison table.

V. Conclusion

We have demonstrated a BBCI system with simultaneous recording and stimulation capabilities, optimized for area efficiency and scalability in advanced CMOS technology (65nm LP). This chip advances the state-of-the-art by integrating high-voltage stimulation in mainstream LP CMOS with low-power recording and digital back-end computation.

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