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Two-Way Traffic Ahead

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Integration of discrete radios onto a single-silicon CMOS substrate [1]–[6], followed by commercialization of single-chip cellular, Bluetooth, and Wi-Fi radios [7]–[9], has shaped the wireless world that we live in today. Although integration of wireless transceivers with powerful microprocessors in very large systems on chip (SoCs) is currently commonplace in consumer electronics, the demand for lower power consumption, higher effective data rates, and higher network capacity continues to drive research on integrated radios. By some estimates, the demand for mobile data per volume area will increase 1,000× during the next decade, with end-user data rates increasing by as much as 10–100× [10].

Numerous efforts during the last 10 years have focused on methods to improve the data rate of mobile wireless devices. Research from diverse areas including communication theory, electromagnetics, and circuit/

device implementation techniques have shown significant progress toward increasing spectral efficiency and exploiting underutilized spectrum to achieve higher data rates. However, these methods typically come at the expense of added radio complexity, which implies higher costs and power consumption compared to existing systems. For example, multiple input/multiple output (MIMO) radios increase throughput by exploiting the spatial diversity offered by massively arraying transceiver elements. Millimeter-wave (mm-wave) bands above 30 GHz have demonstrated multigigabit per second data rates [11] and will likely be better utilized with the evolution of 5G wireless standards. However, these systems suffer from high path loss and unfavorable propagation characteristics, which implies more complex radio hardware (phased-array systems) that typically translates to higher power consumption [12].

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Digital Object Identifier 10.1109/MMM.2018.2880489

Date of publication: 11 January 2019

Full-duplex (FD) communication uses a single channel to both transmit and receive simultaneously and is another technique to achieve higher spectral efficiency that could be used as a standalone solution or as a way of complementing both MIMO and mm-wave transceivers [13]–[15]. Compared to traditional frequency-division duplex (FDD) systems, which use dedicated channels to transmit and receive, FD radios combine the two channels (Tx and Rx) into one common Tx/Rx band, thus freeing up one of the two bands for another user, which ideally increases the spectral efficiency by two times (Figure 1). Compared to traditional time-division duplex systems, where users only transmit or only receive at any given moment, FD systems increase the spectral efficiency up to two times by transmitting and receiving simultaneously. The bands from 100 MHz to 5 GHz represent the most favorable characteristics for wireless communication, due to the relatively low path loss and the reasonably small size of components used to implement transceiver building blocks (antennas, LC tanks, and transformers). However, these bands are completely occupied by communication applications that include emergency services (police and fire), cellular networks, media broadcast, and Wi-Fi. The value of the bands below 10 GHz was recently highlighted by a US\$8 billion acquisition of a 31-MHz band around 600-MHz frequency by T-Mobile [16]. If FD communication could be applied to all bands below 10 GHz, this would potentially translate to more than a trillion dollars in savings for carriers and end users.

There are significant challenges when simultaneously transmitting and receiving on the same frequency, mainly the presence of a large interfering signal from the transmitter that is presented to the receiver input, which is often referred to as Tx *self-interference* (SI). This SI will degrade the signal-to-noise ratio (SNR) at the back end of the receiver, potentially eroding any improvement in spectral efficiency. Enabling an FD transceiver relies on cancellation techniques to suppress the Tx SI. These cancellation methods find use in other applications, including interference suppression in radar and cable modem systems. In fact, with the advent of DOCSIS 3.1 modems, FD transceivers are currently used by commercially available cable modems [17].

FD System Overview

A key challenge in realizing an FD transceiver is the strong Tx output signal that appears as interference at the Rx input of the same transceiver (Figure 2). Before the desired received signal is demodulated in the Rx's digital back end (DBE), the interference should reside 10 dB below the noise floor at the Rx back end to limit the SNR degradation to 0.5 dB. The SI at the Tx output contains several nonidealities along with the linearly amplified and upconverted Tx baseband input signal.

First, the circuits used for upconversion and amplification have a limited linearity, which results in unwanted harmonics and intermodulation products in the Tx spectrum. Also, the quantization noise of the Tx digital-analog converter (DAC), in addition to the noise contributed by any active circuits along the Tx signal path, contributes to broadband noise in the Tx spectrum. Finally, the phase noise of the local oscillators (LOs) used for up-/downconversion will potentially degrade the achievable SI cancellation [18].

The three basic components associated with undesired Tx SI consist of 1) the modulated carrier at the Tx output, 2) the broadband noise generated by the Tx signal path, and 3) interference generated by the nonlinearities in the Tx resulting in intermodulation components and spectral regrowth. The flow of Tx SI in both the Tx and Rx signal paths is shown conceptually in Figure 2. To illustrate the impact of intermodulation around the carrier, two tones are shown as they pass through the transmitter and back to the receiver. This will become particularly important in future multicarrier systems where the in-band subcarriers can intermodulate with each other, creating distortion products around the signal bandwidth. This intermodulation then appears with both the Tx noise and the transmitted modulated signal to present a source of interference to the receiver. Thus, the challenge of Tx SI cancellation is not only confined to simply canceling the modulated signal produced by the Tx but also the distortion and noise components generated along the Tx signal path. This ultimately limits the amount of SI suppression that can be performed by using purely the DBE as a reference source.

SI cancellation techniques can be generally divided into three domains: Tx-to-Rx air interface (multiple antennas, circulators, and duplex filters), cancellation in the RF and analog front end (AFE), and SI suppression using the DBE. Ultimately, the goal is to suppress as much of the Tx SI (including the intermodulation, Tx circuit noise, and phase noise) before the desired received signal is demodulated at the receiver back end. Future implementation of FD radios will likely accomplish this cancellation task by implementing

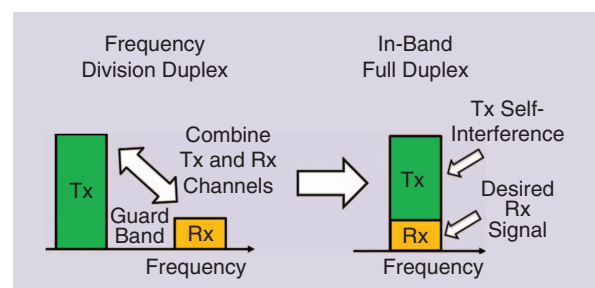


Figure 1. A conceptual diagram illustrating the improvement in spectral efficiency in FD communication as compared to more traditional FDD.

cancellation functions in each of the three domains shown in Figure 3.

Each domain could contain multiple components that perform cancellation. For example, the radio AFE may have multiple cancellation paths that tap off different points in the transmitter, from the baseband up to the power amplifier (PA) output. Likewise, the output of the cancellation paths could be injected into various points along the Rx path. The radio air interface, often considered as the antenna(s) with a circulator or filter, will comfortably supply 20 dB of Tx-to-Rx isolation before the Tx SI hits the radio receiver AFE input. From an Rx linearity performance perspective, it is better to provide some level of cancellation as close to the antenna as possible. Similarly, the origin of the cancellation path is influenced by which SI components are being suppressed. For example, if the noise and nonlinearities generated by the Tx are to be suppressed, the cancellation path should start later in the Tx chain (ideally at the PA output). Finally, digital cancellation can be employed to suppress any residual carrier signal.

Different Tx-to-Rx isolation techniques can be found throughout the literature, e.g., two or more distanced

antennas [19]–[22], dual-polarized or phased-array antennas [23]–[25], circulators [26]–[29], and electrical balance duplexers (EBDs) [30]–[33] (Figure 4). The Tx-to-Rx isolation in a two-antenna system depends on the antenna separation and the orientation of the antennas [34], [35]. Although using two antennas, one dedicated for the Tx and the other for the Rx, could provide a higher Tx-to-Rx isolation by increasing their separation [24], this would also imply more space and a higher-cost solution, which is undesirable for consumer handheld devices. An alternative strategy for the air interface of FD transceivers would be the use of a single antenna for both Tx and Rx, coupled with the use of a circulator, which is a three-port device characterized by nonreciprocal paths that allows signals to flow in one direction (Tx-to-antenna, antenna-to-Rx, and Rx-to-Tx) while providing a high isolation in the reverse path (e.g., Tx-to-Rx, Rx-to-antenna, and antenna-to-Tx).

As an example, ferrite circulators use magnetic materials [26] to provide a wideband (>80 MHz) Tx-to-Rx isolation with high Tx power-handling capability (>25 dBm) and minimal insertion loss (<0.3 dB) [27]. However, these devices typically occupy a large

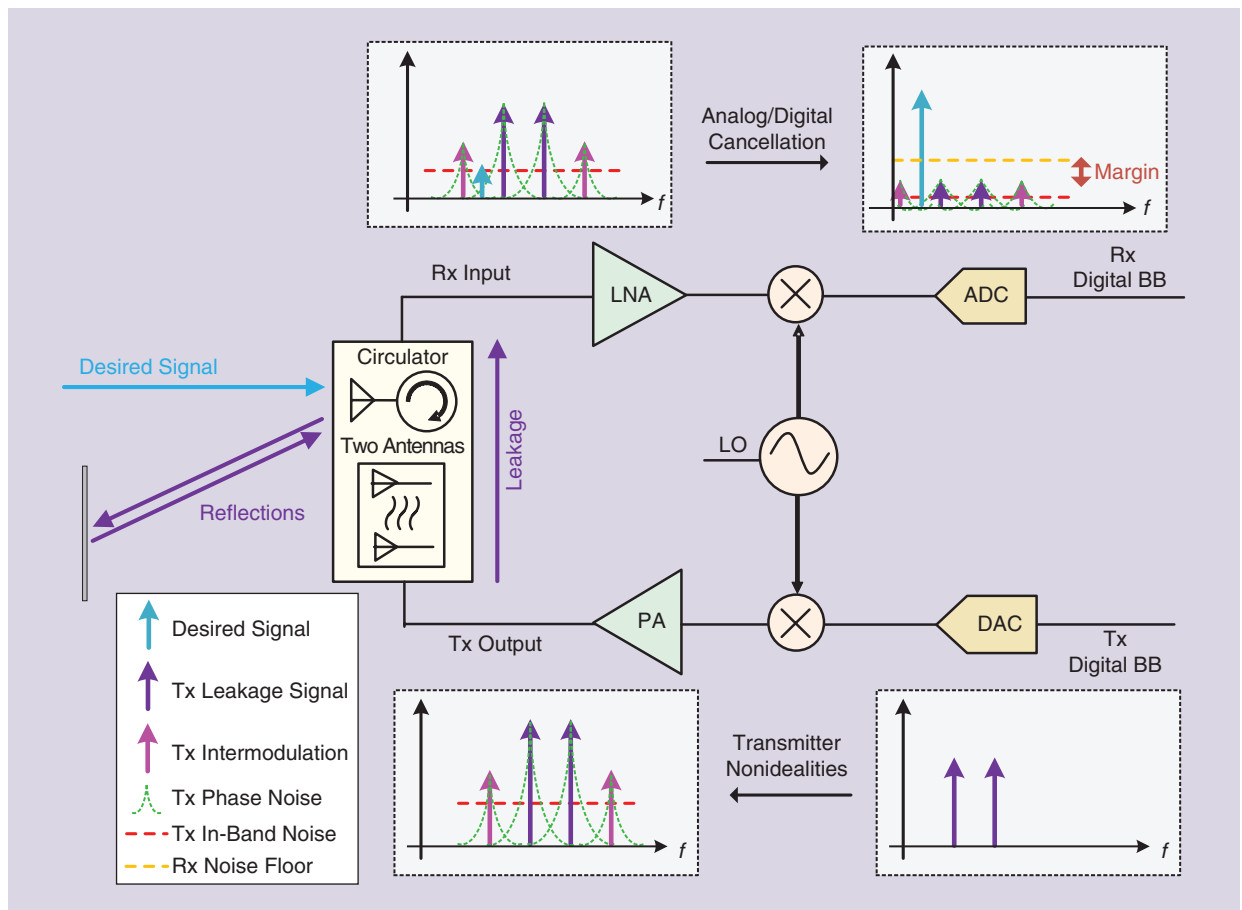


Figure 2. The Tx leakage and reflections appear as SI in the receiver of an FD transceiver. The SI signal and nonidealities generated in Tx should be suppressed at least 10 dB below the Rx noise floor to have a minimal impact on Rx noise figure (NF). BB: baseband.

footprint. Integrated CMOS circulators that show significant promise have been proposed recently [36]. They exploit the time-variance characteristic of N-path filters to break the on-chip reciprocity. A recent version of this device has the ability to handle +8-dBm signal supplied by the transceiver [36].

An alternative implementation approach to realize a circulator-like function is an EBD, which is based on a hybrid transformer [32] [Figure 4(c)]. EBDs can be integrated with the rest of the transceiver on the same silicon substrate and show promise toward achieving very high linearity (>70 dBm [37]), thus allowing their use with high-output power signals from a Tx. However, EBDs suffer from a high inherent insertion loss [32] due to reciprocal properties that translate to a minimum insertion loss of 3 dB in both the Tx and Rx signal paths. Also, similar to other single-antenna FD systems, to maintain a high Tx-to-Rx isolation, the balancing impedance must be tuned dynamically in response to antenna impedance changes [38], where the tuning circuitry has the potential to degrade the linearity performance. The mentioned Tx-to-Rx isolation methods differ from each other in size, depth of suppression, isolation bandwidth, power-handling capability, linearity, and

insertion loss, all of which are currently being explored by researchers in the RF community.

There are a number of considerations that must be taken into account when implementing any circuitry to perform RF/analog cancellation [39]. In general, an ideal integrated Tx SI canceler would possess the following characteristics:

- introduce minimal noise in the Rx signal path, particularly if the SI mitigation component is placed prior to the low-noise amplifier (LNA)
- be highly linear, especially any cancellation/filtering blocks past the PA
- occupy minimal silicon area, implying minimum use of inductors and transformers
- present negligible loading (high impedance) to the Tx/PA output, which minimizes any output power loss and efficiency degradation
- have minimal sensitivity to packaging and electromagnetic interference effects.

From the perspective of maximizing the Tx-to-Rx isolation, it is most beneficial to capture the entire Tx spectrum as close to the antenna as possible (PA output) to include the modulated signal centered at the

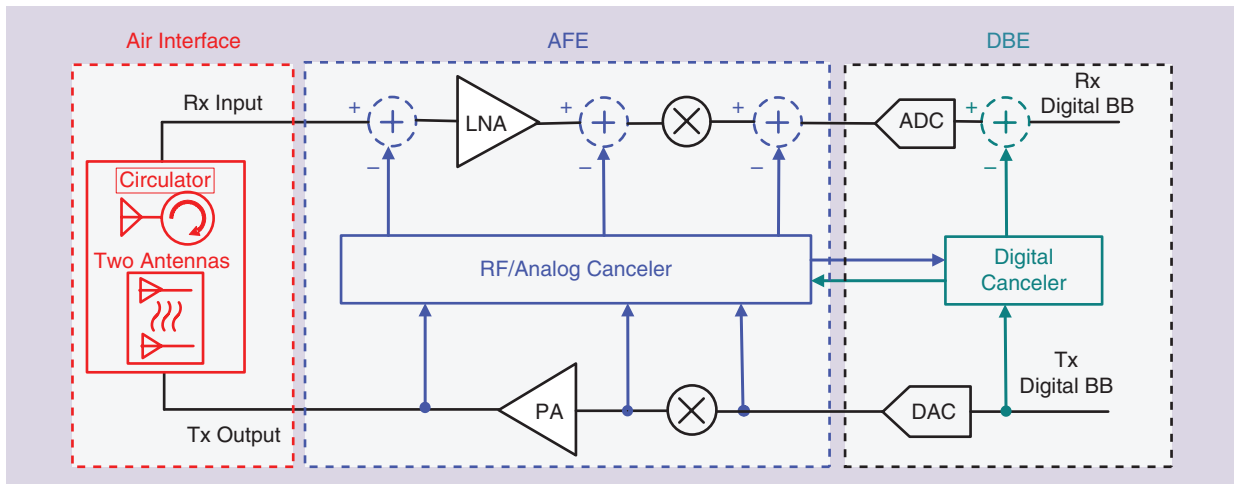


Figure 3. The categorization of SI cancellation methods in FD transceivers: Tx–Rx air interface, RF and AFE cancellation, and digital cancellation in the DBE.

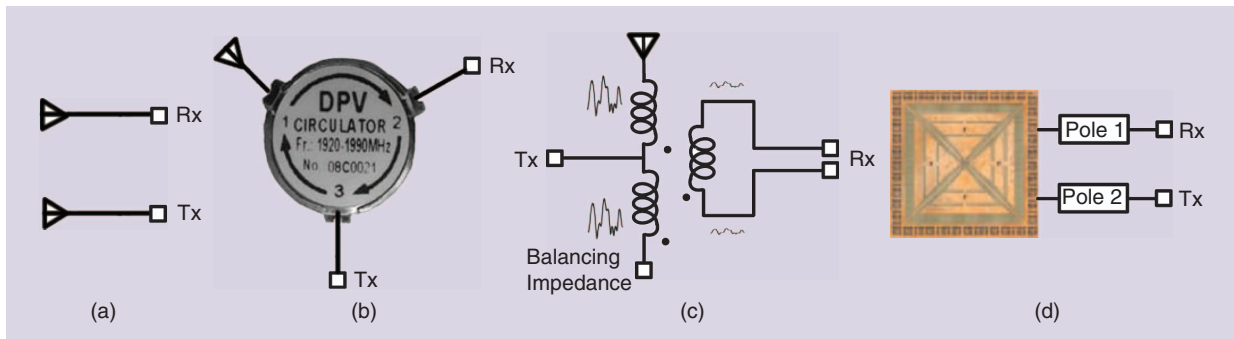


Figure 4. The different Tx-to-Rx isolation methods: (a) two antennas, (b) a circulator, (c) an EBD [32], and (d) a dual-polarized antenna [23].

carrier frequency as well as the noise and nonlinearities generated by the Tx/PA. Likewise, the point of injection for the cancellation signal should be as close to the Rx input as possible to reduce the required linearity and blocking performance of subsequent blocks in the Rx chain. Therefore, to enhance the Tx-to-Rx isolation, some level of SI suppression should be performed between the Tx output and Rx input (Figure 5).

Numerous efforts have explored methods to mitigate Tx leakage signals that track the SI over a broad bandwidth by synthesizing a frequency response in the cancellation path [40]. Feedforward cancelers, e.g., [29], [41], [42], copy the Tx output and inject an amplitude-adjusted and phase-rotated signal into the Rx signal path. In [22], a second-order G_m -C N-path filter was used to perform frequency domain equalization. An alternative method synthesizes an inverse leakage signal at the LNA input using a current DAC [43]. However, for applications requiring high Rx sensitivity, the DAC noise will likely degrade the Rx sensitivity (see Figure 5).

Other SI suppression techniques include passive vector modulator downconversion mixers [44], baseband

Hilbert transform equalization [45], integrated high-Q passive filters using bond wires [46], transformer coupling [47], polyphase filters [48], active bandpass sink filters [49], a least-mean-squares adaptive filter [50], a mixer-first FD LNA [51], a harmonic-reject PA to suppress out-of-band SI [52], and an LC phase-shift network [53]. However, these approaches typically rely on some resonant circuitry that delivers a relatively narrow-band solution.

After Tx SI cancellation is performed at the air interface and AFE, digital cancellation can be employed to further suppress the SI signal to levels below the Rx noise floor. A sufficient analog-digital converter (ADC) dynamic range is required to capture the SI as well as desired signal, with enough resolution to cancel the former and demodulate the latter. Digital cancelers use the original transmitting data together with channel model estimates to cancel the Tx residual signal in the Rx baseband. These residual signals could originate from linear and nonlinear parts of the Tx signal as well as signals generated in the circulator, canceler, or Rx due to the Tx data.

Several efforts achieve high digital cancellation, particularly by accurately modeling the nonlinearity of

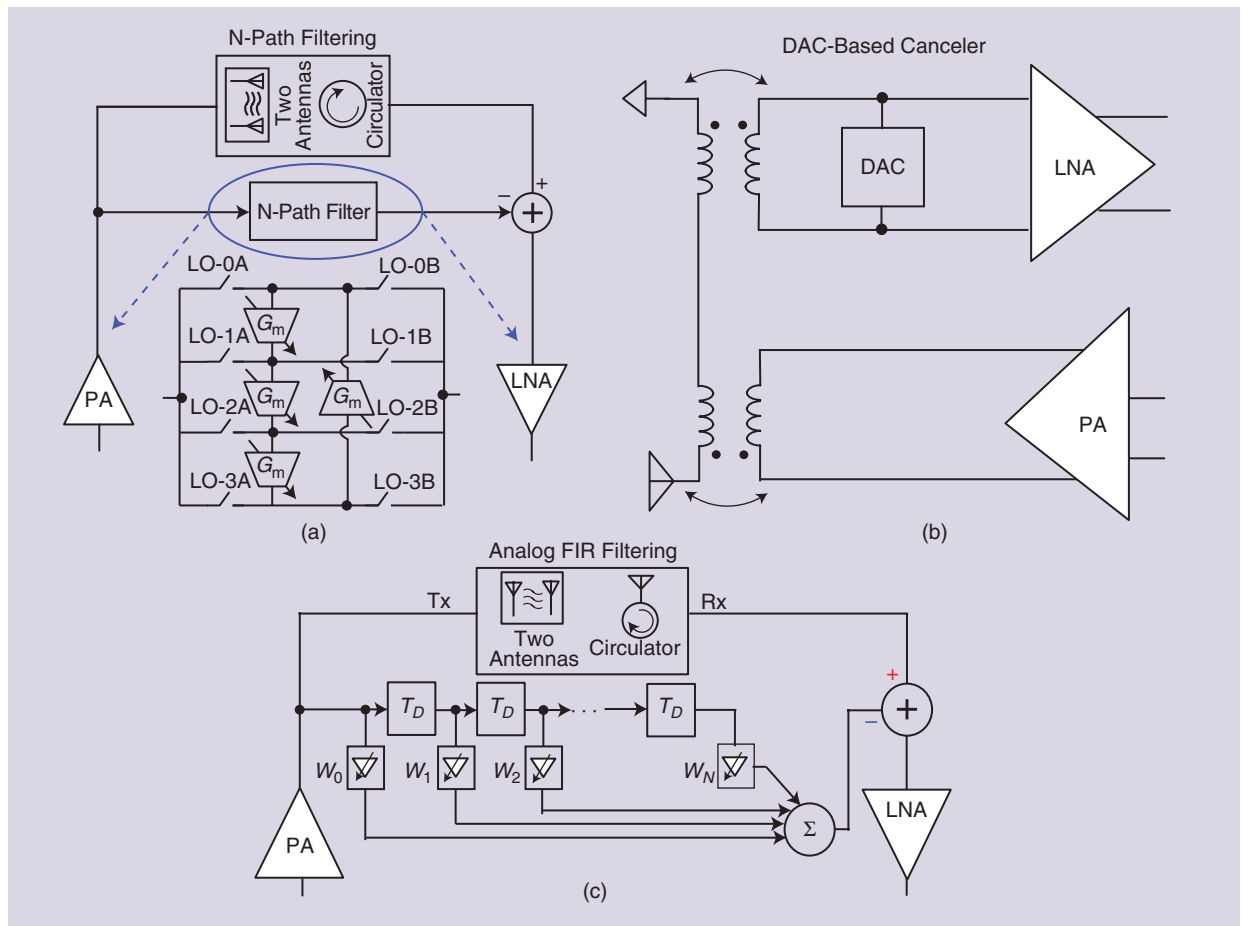


Figure 5. The suggested techniques to perform wideband SI cancellation, including an N-path filter [22], DAC-based cancellation [43], and analog FIR [29].

the Tx signal path [54]–[58]. In [54], a general nonlinear model that considers up to an 11th-order nonlinearity of the Tx signal is used to achieve 48-dB digital cancellation. In [55], a parallel Hammerstein model is used to address the nonlinearity generated by a low-cost PA. It achieves 25-dB linear digital cancellation and 8.5-dB nonlinear digital cancellation. In [56], three nonlinearity cancellation techniques—reconstruction, auxiliary Rx path, and precalibration—were simulated for different wireless channel coherence times and compared to linear cancellation.

The achievable digital cancellation is limited by the Tx and Rx impairments, such as Tx/Rx nonlinearities, DAC/ADC dynamic range, phase noise, and environmental reflections. The effect of these impairments can be lumped into the Tx error vector magnitude, which sets a high limit for achievable digital SI cancellation [24]. Note that a cancellation signal derived from the TX DBE will not include all the noise generated by the TX AFE (phase noise, in-band thermal noise, PA noise, etc.); thus, all the noise produced by the TX AFE will be coupled into the receiver without cancellation.

Table 1 analyzes several commercial wireless standards in terms of RF/analog canceler requirements for FD operation without significant SNR loss [59]–[61]. For each standard, channel bandwidth is extracted from the standard, and practical numbers are assumed for the Tx maximum output power and the Rx NF. The required SI suppression is calculated based on (1):

$$\text{required SI can} = \text{Tx}_{\text{Power}} - \text{Rx}_{\text{noise floor}} + \text{margin}. \quad (1)$$

A 10-dB margin is assumed to calculate the values in Table 1. As can be seen in the table, standards with higher Tx output power and narrower channel bandwidths require more SI cancellation. For example, such cellular standards as LTE require almost 140 dB of SI cancellation, whereas Wi-Fi may demand as much as 125 dB, and such short-range standards as Bluetooth only demand 115 dB of SI suppression.

Signal strength at different points along the Rx chain depends on the achieved Tx leakage suppression and the Rx gain distribution. To calculate linearity requirements for the Tx, Rx, and RF canceler, achievable interface isolation, digital linear and nonlinear cancellations, and RF cancellation are assumed for an FD transceiver based on recent advances. Equations (2)–(4) are used to calculate the required linearity in terms of third-order intercept point (IIP3) for the Tx, Rx, and RF canceler (assumed to be connected between the Tx output and Rx input):

TABLE 1. The SI cancellation and linearity requirements for FD transceiver implementation of selected commercial standards.

Standard	BLE*	Wi-Fi	GSM	WCDMA	LTE
Channel bandwidth (MHz)	1.0	40.0	0.2	5.0	5.0
Tx max power (dBm)	4.0	20.0	30.0	24.0	23.0
Assumed Rx NF (dB)	14.0	4.0	10.0	5.0	4.0
Rx noise floor (dBm)	−100.0	−94.0	−111.0	−102.0	−103.0
Required SI suppression (dB)	114.0	124.0	151.0	136.0	136.0
Required Tx OIP3 (dBm)	18.0	34.0	44.0	38.0	37.0
Required canceler IIP3 (dBm) ⁺	38.5	59.5	83.0	69.5	68.5
Required Rx IIP3 (dBm)	−31.5	−10.5	13.0	−0.5	−1.5

*Power class II.
+Assumed to be connected between Tx output and Rx input.

$$\begin{aligned} \text{required Tx OIP3} = & 1.5 \times \text{Tx max power} - 0.5 \\ & \times (\text{interface isolation} \\ & + \text{RF cancellation} \\ & + \text{nonlinear digital} \\ & \text{cancellation} - \text{Rx}_{\text{noise floor}} \\ & + \text{margin}), \end{aligned} \quad (2)$$

$$\begin{aligned} \text{required canceler IIP3} = & 1.5 \times \text{Tx max power} - 0.5 \\ & \times (\text{interface isolation} \\ & + \text{nonlinear digital} \\ & \text{cancellation} - \text{Rx}_{\text{noise floor}} \\ & + \text{margin}), \end{aligned} \quad (3)$$

$$\begin{aligned} \text{required Rx IIP3} = & 1.5 \times (\text{Tx max power} \\ & - \text{interface isolation} \\ & - \text{Rf cancellation}) \\ & - 0.5(\text{nonlinear digital} \\ & \text{cancellation} \\ & - \text{Rx}_{\text{noise floor}} + \text{margin}). \end{aligned} \quad (4)$$

The required linearity values in Table 1 are calculated based on an assumed interface isolation equal to 25 dB, digital linear cancellation equal to 48 dB [54], nonlinear digital cancellation equal to 20 dB [54], and RF cancellation equal to 30 dB [62], with the margin set to 10 dB. As expected, cellular standards with higher maximum output power have higher linearity requirement compared to lower power standards. Also, it can be seen that the canceler has the stringent linearity requirement. Any nonlinearity in Tx output is suppressed by air interface, the RF canceler, and nonlinear digital cancellation in the baseband, so higher nonlinearity levels at the Tx output can be tolerated. The Rx nonlinearity requirement is relaxed due to the fact that the leakage signal power at the Rx input is suppressed by the air interface and the RF canceler. However, the

signal power at the RF canceler input is very high because it is connected to the PA output; at the same time, its output is connected to the Rx input. Thus, a modest nonlinearity generated at the RF canceler output will degrade the Rx SNR.

Example of Single-Chip FD Transceiver

A transceiver with a dual-point injection feedforward canceler and EBD is described in this section. This device achieves a deep SI cancellation (>70 dB) over wide bandwidth (>40 MHz) using three Tx SI suppression blocks (Figure 6).

The first SI cancellation component that acts as the air interface is the EBD, where the PA output current splits and flows into different directions toward the antenna port and impedance balancing port. The balancing impedance port should be connected to the same impedance as seen by the antenna port. Due to the symmetry, current flows equally from the center tap in the two coils, emerging at the antenna and balance ports. The two coils generate equal magnetic flux with the opposite polarity, effectively canceling each other in the secondary coil (Rx side).

Two RF feedforward analog cancelers, both of which have their inputs attached to the Tx output matching network, further suppress the Tx SI in the Rx chain. The first RF canceler resides between the PA output and the LNA input, with the primary function of sufficiently reducing the Tx SI power to prevent saturation in the Rx front end. The second RF canceler additionally

suppresses the remaining SI signal with an injection point at the LNA–Rx downconversion mixer interface (Figure 6). This relaxes the linearity demand on the Rx downconversion mixers and filters in the analog baseband and obviates the need for complex in-phase/quadrature auxiliary downconversion mixers and the analog finite-impulse response (FIR) filters as in [29]. The filters in the RF feedforward cancelers can be set to suppress the Tx carrier and/or noise when in FDD mode, independent of the Rx and Tx carrier frequencies.

Each analog canceler is made up of a five-tap analog FIR filter, where each tap includes a delay line and a variable gain amplifier (VGA; see Figure 6). Adding more taps to the FIR filter would increase the SI cancellation bandwidth. However, it would also degrade the Rx NF [63]. Passive resistor-capacitor based first-order all-pass filters are used in each tap to generate the true-time delay. The VGA is implemented using the inverter-based amplifier. Each of the VGA taps has 7-b gain control with one additional bit that determines the signal polarity. An additional bit in the VGA will provide 6 dB more dynamic range and better cancellation. However, this also has the undesired effect of reducing the output impedance of the canceler by half, which loads the LNA input, thus increasing Rx input insertion loss. A push–pull buffer stage was added between each tap delay to minimize the loading effects of later stages. The current outputs of different taps are summed with the ac signal coming from the Rx input (antenna) in the current domain.

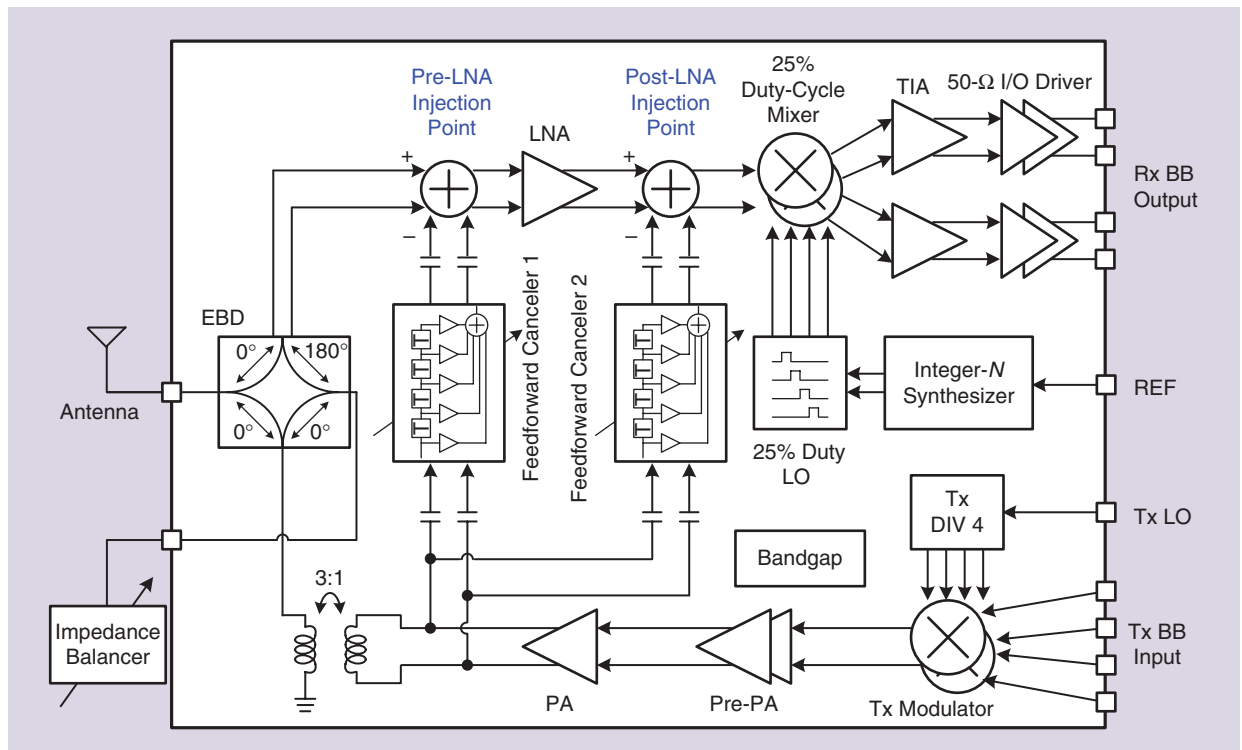


Figure 6. The improved dual-injection path canceler with EBD to allow both FD and FDD operation.

The upconversion mixer, LO dividers/drivers, PA predriver, and a class-AB PA form the Tx chain. The Rx signal path includes a Gm-based LNA that converts the received signal into a current, a passive mixer followed by a baseband transimpedance amplifier, and an integer-N synthesizer. Both the integrated EBD and a transformer at the PA output eliminate the need for off-chip RF components, including a circulator and RF baluns. The balancing impedance is implemented off chip for tunability purposes and to achieve a high linearity.

A one-to-three transformer is placed after the PA to translate the 50- Ω impedance of the antenna down to 6 Ω , which is the optimum resistance for the PA output. A two-to-four-turns ratio EBD converts the single-ended input to a differential signal and provides the LNA noise matching. The LNA is implemented with a current-reuse Gm stage, which provides a current-mode output to drive the passive downconversion mixers. The feedforward cancelers only cancel the differential mode Tx SI and have no effect on any common mode leakage through the EBD. To provide a first-order rejection of any common mode signals generated by the EBD, both PMOS and NMOS tail currents are utilized in the LNA [64].

This transceiver chip was fabricated in TSMC's 6 L 40-nm LP CMOS process with a die size of 4 mm² and consumes 106 mW (without PA) (Figure 7). The EBD occupies an area of 0.23 mm², whereas both RF cancelers occupy an area of 0.12 mm². To close the filter adaptation loop, an Altera Cyclone III field-programmable gate array (FPGA) with 14-b ADC/DACs operating at 100 MHz is used to find optimal codes for the canceler weights in real time with a gradient descent algorithm (Figure 8). The on-chip SI cancellation is tested by applying a 20-/40-/80-MHz orthogonal frequency-division multiplexing (OFDM) multicarrier 64 quadrature amplitude modulation (QAM) modulated signal, and the 72.8-/70.1-/65.2-dB difference in channel power (maximum 77.6 dB from a single-tone sweep) is measured with an integration bandwidth of 22/45/85 MHz, respectively (Figure 9). A more thorough description of this chip is given in [62], while the key data are summarized in Table 2.

Future FD Radios—Confronting SI with Multiple Environmental Reflections

In a practical usage scenario, when FD transceivers are used in either an indoor or outdoor environment, there are multiple leakage paths from the Tx output to Rx input, where each leakage path has a different associated time delay. All of the paths together form the total SI presented to the Rx. The first component of SI results from a direct coupling path through the board or chip substrate. Because of the immediate vicinity

of the Tx relative to the Rx, this coupling path has the shortest delay to the Rx input, as compared to other SI components. The second large response is attributed to a quick reflection at the antenna interface, which is the result of an impedance mismatch between the antenna and its driver. The signal strength of the antenna reflection depends on the matching accuracy and varies as the antenna impedance changes due to user interaction or environmental changes (e.g., as the handheld moves relative to the user's head); the antenna impedance varies, as does the amplitude of the reflected SI.

Finally, a third major component to the Tx SI is attributed to what is commonly called *environmental reflections*, which result from the Tx signal reflecting off nearby (several meters away) objects. The power, delay, and channel response of these reflections depend on the propagation characteristics and the material associated with the reflection. Although environmental reflections have lower power than the signals due to direct leakage and antenna mismatch, they could have much longer delays, on the order of several hundreds of nanoseconds, for a typical indoor environment [65].

To characterize the SI power as a function of time (i.e., delay), the leakage channel time-delay profile should be characterized [35], [66]. As an example, the environmental reflection power for a 0-dBm signal at 2.4–2.5 GHz through a discrete circulator (Meca Electronics #CS-2.500, 2.3–2.7 GHz) was characterized with measurements in different environments (Figure 10). The direct leakage path and antenna mismatch are combined to form the first peak. There is a wide variation both in the amplitude and delay of various coupling paths, including the antenna and environmental reflections. The

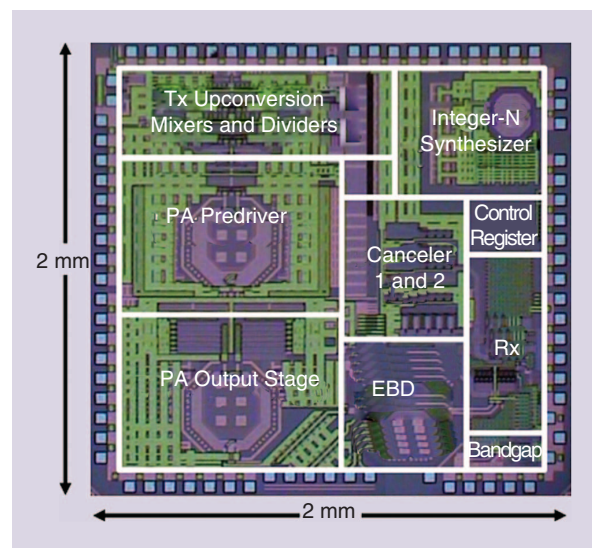


Figure 7. A die photo of the improved dual-injection-path radio with EBD implemented in a 40-nm TSMC CMOS process.

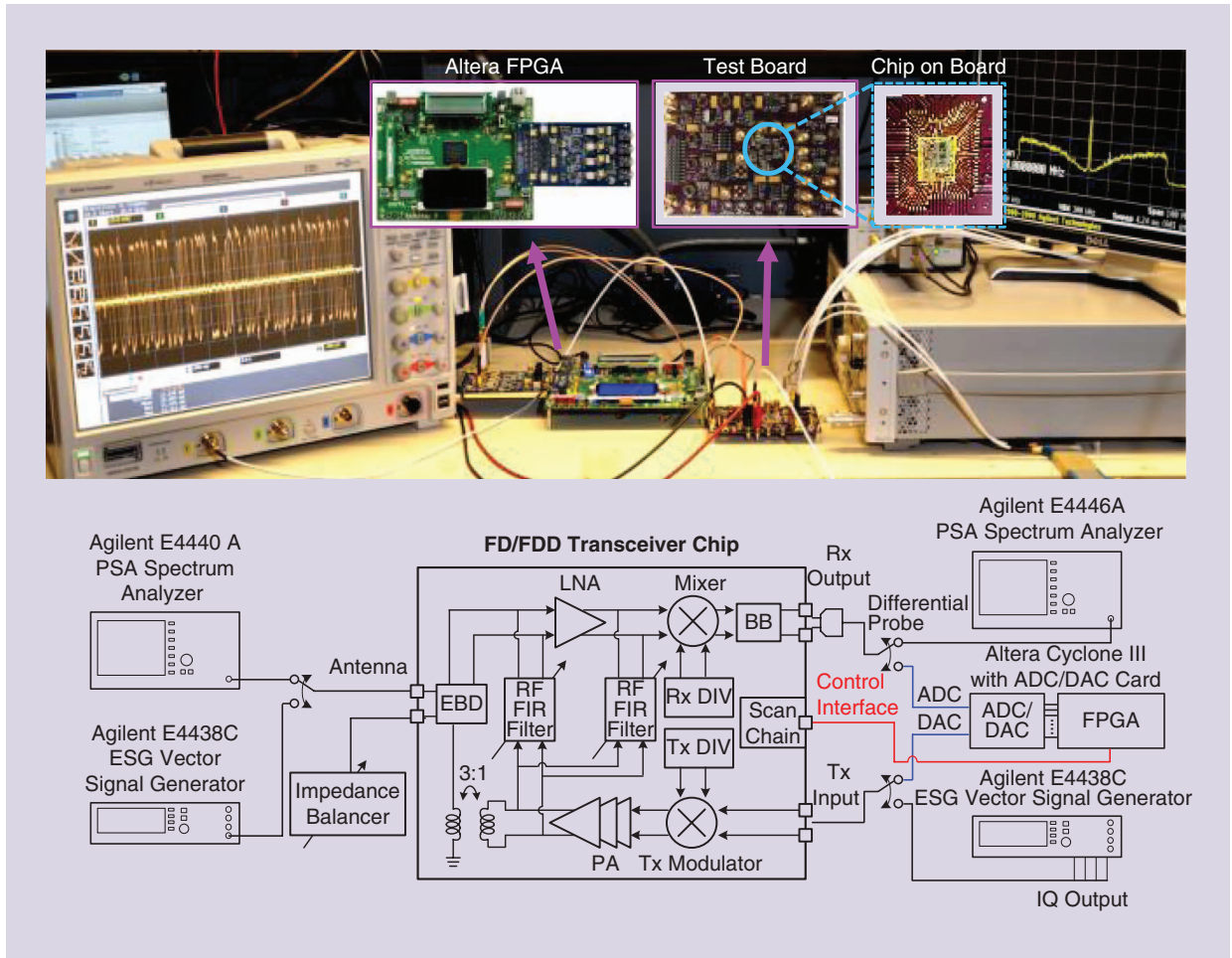


Figure 8. The test setup, which includes an FPGA board to emulate the digital baseband and perform real-time calibration.

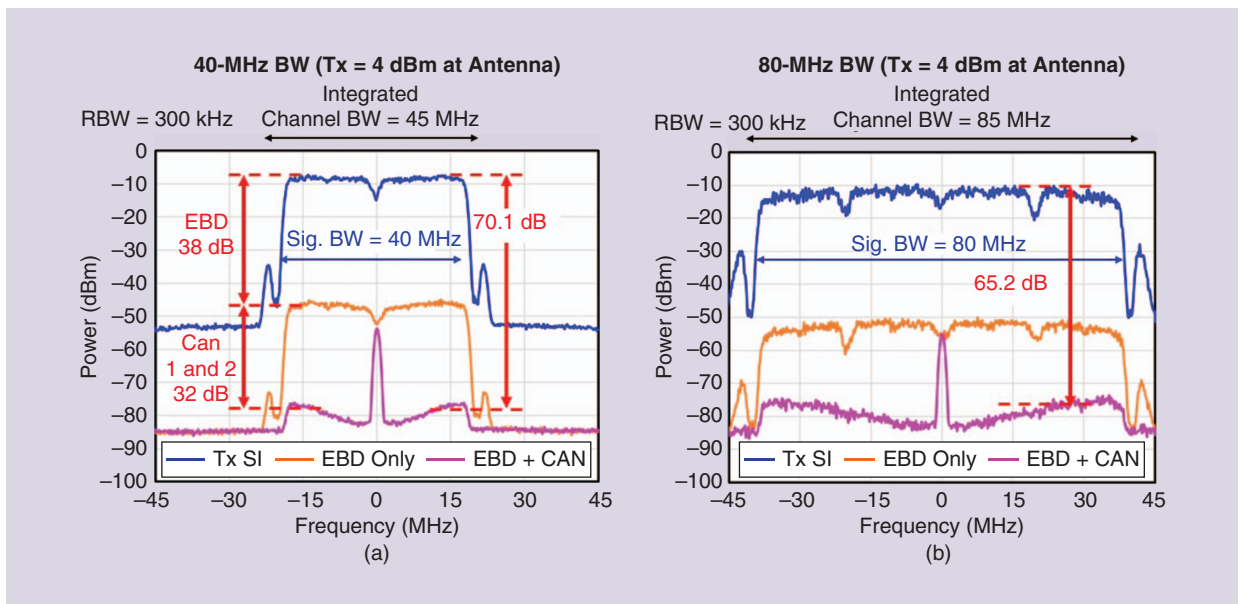


Figure 9. The measured SI cancellation using IEEE 802.11 (OFDM multicarrier) sample packets with different bandwidths: (a) at 40-MHz bandwidth (with Tx = 4 dBm at the antenna) and (b) at 80 MHz bandwidth (with Tx = 4 dBm at the antenna). BW: bandwidth; RBW: resolution BW.

TABLE 2. A comparison of recently published FD transceivers and components, including circulators.

Architecture	Cancellation Current-Steering DAC [43]	Frequency Domain Equalization [22]	On-Chip Circulator + Duplexing LNA [36]	EBD + SAW Filter [30]	EBD + Rx [33]	SIC VM Downmixer + Mixer-First Rx [18]	Transformer Coupling [39]	Polyphase Filter + Active Gm Stage [48]	Dual Path + Adaptive Filter [29]	EBD + Double-RF Adaptive Filter [62]
Technology	65 nm	65 nm	65 nm	0.18 mm SOI	28 nm	65 nm	40 nm	40 nm	40 nm	40 nm
Frequency range (GHz)	1.0–1.8	0.8–1.4	0.61–0.975	0.7–1.0	1.7–2.1	0.15–3.5	1.8–2.4	2.4	1.7–2.2	1.6–1.9
Tx Si										
$T_{\text{out}}\text{-to-Rx}_{\text{in}}$ isolation (dB)	0	30–50	40 ^e	50	40	25	50	20–30	30–35	39 ^a
	No external isolation	External circulator two antenna	On-chip circulator	On-chip EBD	On-chip EBD	Two antenna	External duplex filter	External circulator	External circulator	On-chip EBD
Total on-chip SIC Depth (dB)/bandwidth (MHz)	50/20	20/25 (15) ^h	40/20	50/10 (SAW) 50/2 (EBD)	45/14	21/16	20/3.84	30/4	50/42	72.8/20 ^b 70.1/40 ^c 65.2/80 ^d
Rx gain (dB)	6–18	27–42	28	7.5	35	24	18	45	36	42
NF (dB)	7.6	4.8	6.3	7.6	6.7	10.3–12.3	5	4.5	4	8.0 (EBD 5.6)
SIC NF degradation (dB)	1.1	1.1–1.5 (0.9–1.2) ^h	1.7	N/A	N/A	4	0.1	0.6	1.5	1.6
Canceler area (mm ²)	N/A	N/A	N/A	N/A	N/A	N/A	~0	0.015	0.349 (RF+BB)	0.12 (RF*2)
SI Circuitry power (mW)	60	44–91 ⁱ	36 ^f	0 (passive)	0 (passive)	1–10	0 (passive)	0.25	11.5 (RF+BB)	14.3 (RF*2)
Canceler IIP3 (dBm)	N/A ^g	N/A	N/A	N/A	N/A	21.5 ^j	N/A	15	36 (RF)/34.5 (BB)	N/A
Tx-ANT path IIP3 (dBm)	N/A	N/A	30	58	50	N/A	N/A	N/A	N/A	N/A
Max Tx operating power (dBm)	17	N/A	8	24	N/A	3.6	30	0	15	10
Tx SI to Rx LO suppression (dB)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	10	11
Integrated Tx upconversion path	Yes	No	No	No	No	No	No	No	No	Yes
Integrated PA	Yes	No	No	No	No	Yes	No	Yes	Yes	Yes
Integrated PLL	No	No	No	No	No	No	No	No	Yes	Yes
Active area (mm ²)	3.9	4.8	1.5	6.62	0.72	2	2.08	1.93	3.5	4

PLL: phase lock loop; SIC: self-interference cancellation; SOI: Si on insulator;

VM: vector modulator.

^aMeasured with on-chip test structure. ^bMeasured channel power difference with 20-MHz 64 QAM and 22-MHz integration bandwidth. ^cMeasured channel power difference with 40-MHz 64 QAM and 45-MHz integration bandwidth. ^dMeasured channel power difference with 80-MHz 64 QAM and 85-MHz integration bandwidth. ^eAveraged over 20 MHz. ^fAntenna interface. ^gMaximum TX power leakage is 12.6 dBm. ^hMeasurement with an antenna pair, 15-MHz bandwidth, 0.9–1.2-dB NF deg. is with one filter, 2.5-MHz, 1.1–1.5-dB NF deg. is with two filters. ⁱPower including 0–47-mW Gm cells and 44-mW LO for one buffer.

longer delays are typically associated with the environmental reflections, and naturally their power drops as their delay increases.

The measured attenuation over time can be used to derive the required RF/analog and digital SI cancellation as a function of time delay. The SI power at any instance of time is equal to the sum of $T_{x_{power}}$ and the attenuation. The required analog and digital SI cancellation is determined from the difference between the SI power and Rx noise floor plus margin. This difference is plotted in Figure 11 for a Tx power of 10 dBm and an Rx noise floor of -94 dBm. The required analog and digital cancellation is more than 90 dB for the leakage signal and drops for signals with longer delays:

$$\text{required SI can}(t) = T_{x_{power}} + \text{attenuation}(t) - R_{x_{noise\text{floor}}} + \text{margin}. \quad (5)$$

In the digital domain, longer delays can be synthesized more easily than in the analog domain by simply holding values in a digital memory. Therefore, SI signals with longer delays are easier to address in the digital domain. However, as discussed in the “FD System Overview” section, the maximum achievable digital cancellation is limited by Tx/Rx nonidealities. To achieve a delayed-SI cancellation beyond what is possible using the radio DBE, some level of cancellation in the AFE must be employed. The required AFE cancellation can be calculated by subtracting the achievable digital cancellation from the total required cancellation, assuming that the maximum cancellation that can be achieved by the radio’s digital baseband is 48 dB [54] and the suppression is independent of time (Figure 11). Higher digital cancellation would relax

the required AFE cancellation, given the condition that the Rx front end does not go into saturation. The AFE described in the “FD System Overview” section mainly targets SI resulting from short-delay reflections that have a higher power associated with them. However, the SI due to longer delayed environment reflections is more challenging to address in the AFE, mainly because synthesizing a longer delay on chip is less practical to implement.

As mentioned in the “FD System Overview” section, both the RF and the analog cancelers match the SI delay and amplitude before injecting a cancellation signal in the Rx signal path. The power or delay mismatch between the canceler path and the SI would decrease the AFE cancellation. To investigate the effect of delay mismatch, a model as shown in Figure 12 is simulated. This model uses a single delayed (τ_e) version of Tx output as the SI, whereas the canceler is a weighted sum of two fixed delays equal to τ_f and $\tau_f + T_c/4$, where T_c is the carrier period. The weights w_1 and w_2 are truncated to 12 b, and the input signal has 1-/5-/40-MHz channel bandwidth centered at 2.4 GHz. Figure 12(b) shows that this single-tap architecture with two fixed delays, separated in time by 104 ps, can provide 20-/12-/6-dB cancellation for the 40-MHz modulated SI with 2-/5-/10-ns delay mismatch.

The SI cancellation drops as the delay mismatch and signal bandwidth increase, i.e., the SI cancellation is inversely proportional to the ratio of delay mismatch over symbol time. This result is intuitive because delay mismatch over symbol time ratio determines the portion of time that both the SI signal and the canceler signal convey the same symbol information. The case of multitap cancelers and multiple delayed SI signals is examined in more detail in [67].

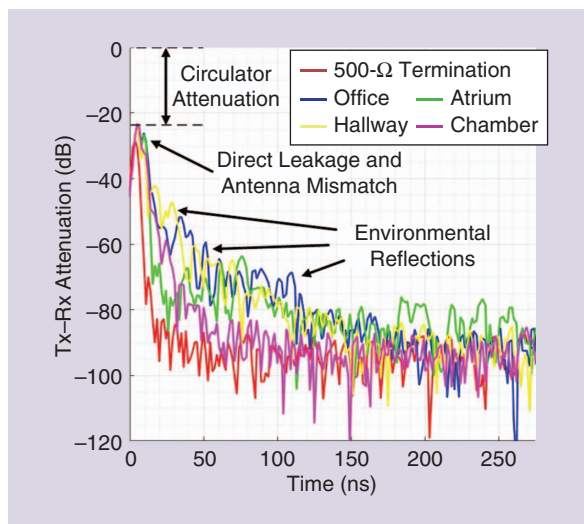


Figure 10. The various reflections measured as a function of arrival time using a Meca Electronics #CS-2.500 circulator.

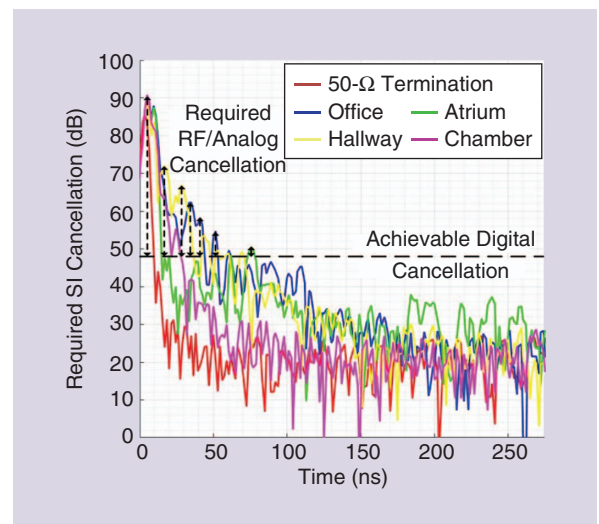


Figure 11. The required SI cancellation for a transceiver with 20-dBm Tx output power and -94-dBm sensitivity using the Meca Electronics #CS-2.500.

For a 40-MHz signal in Figure 12(b), the SI cancellation from the single-tap analog canceler falls faster than the required AFE SI cancellation shown in Figure 11. Thus, a single-tap canceler fails to achieve the required analog cancellation for every delayed SI. Instead, a multitap AFE canceler with different τ_f for each tap must be employed [Figure 13(a)]. The total achievable analog and digital cancellation by the multitap system is shown conceptually in Figure 13(b) (black curve), where multiple copies of cancellation achieved with a single-tap canceler are added together and used to provide enough cancellation for a broad range of time delays. The τ_f associated with different taps is positioned in time to force the valleys of total cancellation contributed between each tap to be above the desired cancellation (dashed curve in Figure 13). As mentioned previously, the required SI cancellation versus time is changing, i.e., more SI cancellation is required for stronger leakage with shorter delays as compared to SI with longer delays. From Figure 13, it becomes evident that the time delays associated with various delays (differences in τ_f) are not uniform.

The need for a multitap RF/analog canceler with delays as long as tens of nanoseconds highlights two challenges for future integrated FD transceivers. The first challenge relates to the implementation of long delays on chip. Printed circuit board traces and/or cables are used in [54] and [55] to generate multinanosecond delays that are impractical for integration on chip because of the physical component sizes. In [68] and [69], a Gm-C APF and LC delay lines are used, respectively, to generate subnanosecond delays at gigahertz frequencies. However, the achieved delay (subnanosecond) is far from the estimated requirement of 100 ns. Switched-capacitor circuits could be used to generate longer delays in the analog domain [70], but nonidealities, such as charge sharing, clock feedthrough, and noise, must be addressed carefully. The second challenge relates to finding the optimal weights for different taps of the RF/analog canceler, which produces an optimum cancellation in real time. As the number of filter taps required to cover a broader range of environmental delays increases, the total number of weights of the canceler also increases. Thus, this makes the calibration of the AFE filter coefficients increasingly more complex and is becoming one of the grand challenges of future FD radio design.

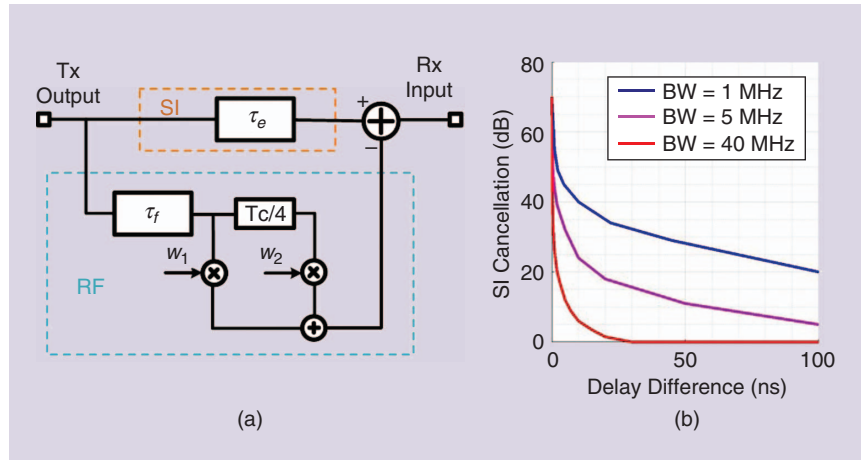


Figure 12. (a) A block diagram of a single-tap analog canceler with two fixed delays. (b) The effect of delay mismatch on SI cancellation for the analog canceler in (a).

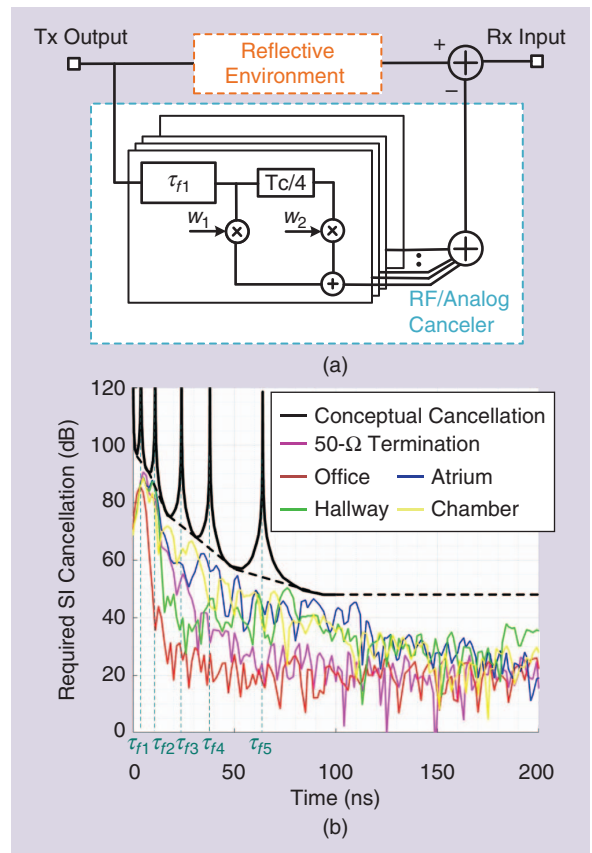


Figure 13. (a) The multitap RF analog canceler with different τ_f associated with various taps. (b) Conceptual achievable SI cancellation for environmental reflection signals by using multitap AFE and DBE cancelers.

Conclusions

This article presents an overview of methods for Tx SI cancellation toward FD integrated radios. An example of an integrated transceiver with 70-dB SI cancellation over 40-MHz bandwidth was described

and shows promise with respect to achieving the level of performance required for FD operation, compatible with some commercial standards-based radios. The challenges presented by environmental reflections in an FD system and the SI cancellation requirements for longer delayed SI were explored. Although advancements have been achieved with respect to realizing integrated, single-chip FD radios, there are still significant problems that remain to be solved, particularly with respect to providing a comprehensive, end-to-end Rx solution that includes SI suppression from the air interface to the radio DBE. RF integrated circuit design for new radio SoCs that include numerous techniques to improve power and spectral efficiency will likely keep designers engaged for years to come!

Acknowledgments

This work was supported by NSF #1408575, SRC-Intel, CDADIC, Google, Qualcomm, and Marvell.

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