Integrated CMOS Transceivers Design Towards Flexible Full Duplex (FD) and Frequency Division Duplex (FDD) Systems

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***Abstract*—This paper provides an overview of both the challenges and the current state-of-the-art in the areas of full duplex (FD) and frequency division duplex (FDD) integrated transceivers. Implementation hurdles in the form of the linearity, noise, bandwidth (BW) and power of transmitter (TX) self-interference (SI) cancellation circuitry are explored. The difficulty of performing SI cancellation is heavily influenced by the modulation method, the maximum TX power output and the receiver (RX) BW. This paper highlights some recent implementation examples of single-chip FD radios that range in performance from low-power cancellation techniques, to transceivers which target broad channel BW (>40MHz) using high output power transmitters. Several 40nm CMOS devices which range in performance from a narrowband low-energy Bluetooth transceiver to analog-frontends which integrate a +24dBm power amplifier (PA) with a dual-point feedforward cancellation architecture for broadband and deep SI suppression are discussed.**

Keywords—CMOS integrated circuits, Interference cancellation, Radio frequency, Radio spectrum management, Adaptive filters, Delay lines, 5G mobile communication.

I. INTRODUCTION

Nearly a quarter century has passed since a number of academic publications reported the integration of discrete radios on to a single-silicon CMOS substrate [1]–[6]. Commercialization of single-chip WiFi, cellular and Bluetooth radios quickly followed [7]–[9], which reduced the radio foot print from dimensions of centimeters to millimeters. This freed up valuable space on cellular handset platforms, allowing the introduction of increasingly powerful microprocessors and memory to usher in the "smartphone" as we know it today. Though integration of complex wireless transceivers seems common place, a number of challenges remain for future integrated radio platforms, mainly with respect to the continued reduction of power and an effective increasing in data rate as well as the network capacity. By some estimates, over the next decade, the demand for mobile data per volume area will increase 1000x and there will be a 10-to-100x increase in data rate to the end users [10].

The last ten years significant effort and numerous publications have focused on methods to improve the data rate of mobile wireless devices. Techniques which branch technical communities have shown significant promise/progress such as mutliple-input and multiple-output (MIMO) which enhance data rate through spatial diversity as applied to a transceiver array. In addition, the evolution of a 5th generation (5G) wireless standards will likely result in better utilization of the millimeter wave (mm-Wave) bands above 30GHz.

While the aforementioned techniques will enhance data rate to the end users and increase the network capacity, these methods are usually done at the expense of added complexity by requiring mutli-element arrays. Conversely, another approach which could be used as a standalone solution, or as a way of complementing both MIMO and mm-Wave systems, is the use of FD communication between two users. This concept combines a traditionally dedicated transmit and receive channels, into one channel BW, which effectively increases the spectral efficiency by 2x as compared to FDD systems. However, after the practical and obvious challenges of dealing with the TX Self-Interference (SI) in the RX, the gains in spectral efficiency are likely less than 2x.

If wireless data rates will indeed increase by more than 10x over the next decade, then the use of FD methods which have an upper bound in 2x spectral efficiency improvement, seems somewhat irrelevant. However, the spectrum below 5GHz is completely occupied by commercial, military and emergency services, to name a few. Moreover, the bands from 100MHz to 5GHz represent the "beach front" real estate of spectrum due to the perfect sweet spot between relatively low path loss and the reasonably small size of components used to implement transceiver building blocks. The value of the bands below 5GHz was highlighted by the recent $8 billion acquisition of a 31MHz BW around 600MHz frequency, by T-Mobile [11]. If FD communication could be applied to all bands below 10GHz, this would translate into more than a trillion dollars in savings for carriers and end users. Moreover, a key to enabling FD communication relies on suppression of TX SI signals which also finds the use for other applications including interference suppression in radar systems.

This paper explores some of the opportunities and challenges surrounding both FD and FDD transceiver implementations. Section II discusses some early implementations of integrated SI cancellation circuitry for narrowband applications and highlights their limitations as applied to higher performance transceivers. The noise from the canceler will also be discussed. The challenges of linearity of FD radio design are examined

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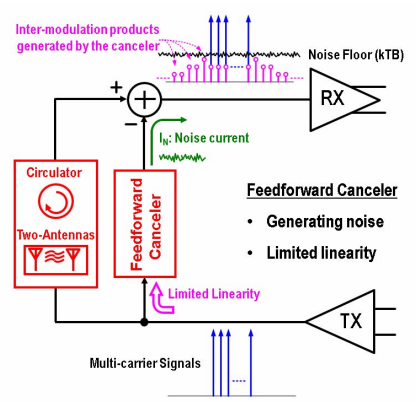


Fig. 1. Components used to improve TX-to-RX isolation. These include dedicated TX/RX antennas, a circulator with shared TX/RX antenna and feedforward cancellation paths.

further in Section III. Two high performance feedforward cancelers with deep SI cancellation over wide BW are introduced in Section IV followed by a conclusion in Section V.

II. Narrow Band Single Carrier SI Suppression Methods and Implementations

Numerous efforts have explored methods to mitigate TX leakage signals in the RX signal path for relatively narrowband signals. Research has focused on eliminating the frontend RF SAW filter and can be categorized as either attempting to perform cancellation or filtering of the TX signal through the use of either all-passive or active circuits. Feedforward cancelers [12], [13], shown in Fig. 1, sample the TX output and inject an amplitude-adjusted and phase-rotated signal into the RX signal path. Other TX leakage suppression techniques which include integrated high-Q passive filters using bond-wires [14], active bandpass sink filter [15], [16], an LMS adaptive filter [17], and a notch filter created by a frequency translational block using mixers to effectively realize a high pass filter function.

Other methods for TX leakage suppression include techniques detailed in [18]–[22]. An integrated duplexer [18], [23], antenna cancellation [19] and a mixer-first FD LNA [24] could potentially be applied for cancelling or filtering the TX SI.

There are a number of considerations which must be taken into account when implementing any TX SI canceler to improve the TX-to-RX isolation. In general, an ideal integrated TX leakage canceler would possess the following characteristics:

- Introduce minimal noise into the RX signal path, particularly if a feedforward canceler is used that has an injection point at the RX/LNA input.
- Occupy minimal silicon area.
- Perform cancellation as close to the RX input as possible to relax the required linearity performance of subsequent blocks.
- Present negligible loading (high impedance) to the TX/PA output, which minimizes any output power loss and efficiency degradation.
- Minimal sensitivity to packaging and EMI effects.

From the perspective of maximizing the TX-to-RX isolation, it is most beneficial to sample/capture the entire TX spectrum as close to the antenna as possible (PA output) which includes both the modulated signal about the carrier, as well as the noise and non-linearities generated by the PA. Likewise, the point of injection for the cancellation signal derived from the TX should be as close to the RX input as possible, to reduce the required linearity and blocking performance of the subsequent blocks in the RX chain. Therefore, if a circulator, feedforward canceler or duplex filters are used, they are best placed between the TX output and RX input, to enhance the TX-to-RX isolation in both FD and FDD radios.

A. Example All-Passive Feedforward Canceler

The placement of the proposed feedforward SI mitigation (SIM) device, relative to both the TX and RX is shown in Fig. 2. This system assumes the use of a discrete frontend duplex filter, and as such, the objective of the canceler is to significantly attenuate the leakage signal at the filter output. For this implementation, the canceler network, realized with a four-port canceler (FPC), is introduced between the TX output and RX input, thus running the TX output signal in a parallel path to an on-board FBAR duplex filter. Again, because the point of injecting a TX cancellation signal is early in the RX chain, care must be exercised to minimize any noise or nonlinearities that might be injected. The use of an all of purely passive reactive components (transformer) in the feedforward path has the advantage of minimizing the noise and any non-linearity injected by the cancellation circuitry into the RX path. An equally important feature of this canceler is to present a high-load impedance at the TX output to minimize the loading to TX.

The approach taken in the work shown in Fig. 2, utilizes components from a transformer-based RX matching network to inject the cancellation signal. A conceptual diagram of the transformer-based TX leakage canceler described in [25], [26] is shown in Fig. 2. A balun serves a dual purpose of performing a single-ended to differential conversion to increase the immunity to unwanted common-mode noise from the substrate and power supplies, as well as impedance matching at the RX input. This feedforward canceler exploits the existing transformer topology to inject a component of the cancellation signal into the transformer, by adding a second and relatively

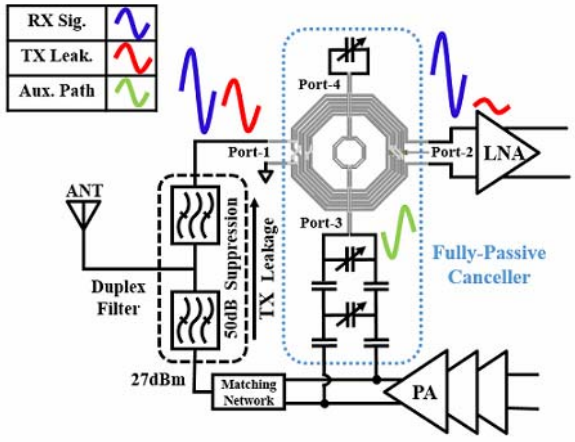
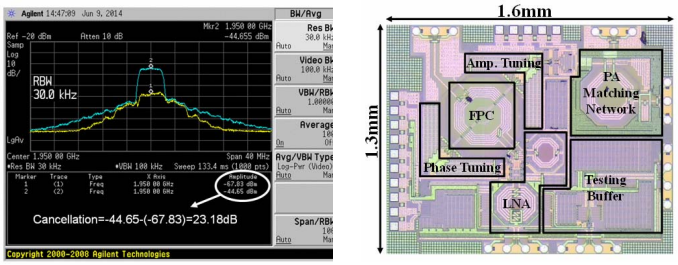


Fig. 2. An early implementation of an all-passive feedforward SI cancellation network.

small primary coil. This coil is added to the center of the transformer to couple a component of the TX signal into the RX signal path, see port-3 in Fig. 2. As such, the canceler coil becomes a component of the RX matching network with minimal additional area (almost zero). The signal received on the main primary attached to the RX input (antenna side shown as port-1) travels from port-1 to port-2 with the TX leakage signal, shown as a hybrid schematic and layout in Fig. 2. The TX signal from the canceler network is intentionally coupled into the RX with 180° phase shift, through the use of the smaller primary, shown as port-3. Since the discrete duplexer has a rejection of approximately 50dB at the TX frequency, any practical cancellation technique must accurately adjust to match the amplitude and have the opposite phase of the attenuated leakage signal. This is done with two techniques: First, port-3 and port-4 are weakly coupled with port-1 and port-2. Second, the amplitude of the coupled-TX-signal is precisely controlled by the capacitor values in the cancellation path, while the phase is modified by varying the termination reactance on port-3 and port-4 of the transformer.

While an expanded version of the measured data is included in [25], [26], some results are presented here for the purpose of discussion. A key focus of this canceler was the low noise and high linearity performance that was achieved from a purely passive feedforward network. Based on a measurement from the RX input to the LNA output, the estimated contributors to the NF were 1.5dB IL from a discrete duplex filter, an additional loss of 1-1.5dB from the FPC/RX matching network, and 2-2.5dB NF from the LNA. A total NF degradation of 0.1dB was measured as a result of enabling the TX signal path with a +30dBm output power PA.

The phase and gain settings for this 4-port canceler were set to attenuate a transmitted 3.8MHz WCDMA signal in the 2GHz band. Approximately 23dB of cancellation was observed (Fig. 3a) from just the feedforward canceler (excludes discrete frontend duplexer). Moreover, the power consumption of the 4-port canceler is negligible. This chip was implemented in a 40nm TSMC CMOS process with a total size of 500µm x 500µm (Fig. 3b). A summary of results for this chip is given in Table 1. While the performance of this feedforward canceler was excellent with respect to noise, linearity and power composition, there are significant drawbacks of using an all passive approach. First, though the work in [25], [26] minimized additional area for the passive canceler by combining the canceling coil into the RX balun (Fig. 3b), generally speaking, passive circuits, like inductors or transformers, occupy



(a) (b)

Fig. 3. (a) 4-port canceler (FPC) achieves -23dB cancellation using WCDMA modulated signal, (b) Die photo of TSMC 40nm CMOS chip, FPC shown center-left.

significantly larger areas as compared to active implementations. The second disadvantage relates to the resonant nature of this 4-port canceler which limits the cancellation BW. Moreover, these types of cancelers are only able to produce one frequency response which may (will) not track the channel response of the leakage path. Thus, to increase the cancellation BW while reducing the silicon area, alternate implementations of a feedforward canceler should be considered, mainly those that involve active circuitry instead of a purely passive resonant solution. However, the use of active circuitry which loads the TX output and supplies a cancellation signal to the LNA input must address the challenge of noise and linearity which is the subject of following sections.

B. Noise in Feedforward Cancellation Circuits

Although using purely passive-reactive cancelers may be sufficient for some narrowband applications, future FD/FDD systems will likely require cancellation bandwidths more than 10x of what can practically be achieved using purely passive solutions. For example, in evolving 5G and WiFi applications, the channel bandwidths could be up to 160MHz. Synthesizing a frequency response to match that of the leakage path likely requires the use of active circuits. A such, the challenge of noise injection and the linearity of the active canceler becomes paramount in the design.

To understand of the noise injected into the RX from the canceler, a simple model is used, see Fig. 4. The equivalent noise resistance, looking back into the canceler from the perspective of the RX signal path, at the point of injection, must be comparatively higher as compared to the antenna 50Ω impedance (or whatever impedance at the point of injection). Also, a critical aspect related to the degradation in RX NF relates to how much gain, or attention, is required in the cancelation path. Between the TX output and RX input, there is naturally a ~20dB attenuation which can be achieve by either using two antennas or a single antenna with a circulator. Thus, the upper bound of gain necessary in a feedforward canceler to match the amplitude of a leakage signal is -20dB. It is somewhat counter intuitive to note that the noise performance of the cancellation path benefits from the need for low gain. This is due to the fact that the received signal of interest never passes along the canceler signal path. The dominant noise contribution of the canceler comes from the canceler's output Gm stage which is represented as a NMOS device, see Fig. 4(a). In this example, the thermal noise of a transistor operating in saturation region [27] is given in Eq. (1),

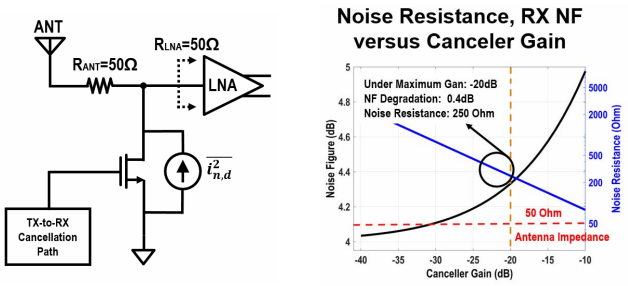
$$\overline{\iota_{n,d}{}^2} = 4kT\gamma g_m \tag{1}$$

Here, γ and g_m are the excessive noise coefficient and transconductance, respectively. Assuming the antenna and LNA are perfectly matched and have an impedance of $R_{ANT} = R_{LNA} = R = 50\,\Omega$, the Gm cell is loaded by the antenna impedance, R_{ANT} in parallel with the LNA input impedance, R_{LNA}. The voltage gain of the canceler (A) is:

$$A = g_m \cdot R/2 \tag{2}$$

The total RX NF including the contribution of the canceler is given in Eq. (3)

$$\text{NF\_Total} = 10 \cdot \log_{10}(NF\_RX + 2\gamma A) \tag{3}$$



(a) (b)

Fig. 4. Simple model to illustrate the relationship between RX NF degradation and the gain in the feedforward cancellation path.

where NF_RX is the noise figure (NF) of just the RX without any added noise from the canceler. Fig. 4(b) shows the RX NF simulation results versus the canceler gain, assuming a typical RX NF of 4dB, a noise coefficient γ of 1, and the carrier frequency of 2.4GHz. As such, the RX NF degradation due to the addition of the canceler is a function of the canceler path gain.

This is intuitively pleasing given that the g_m associated with the common source output stage of the cancellation path will increase, as the gain of this path increases, so will the drain current noise injected into the RX signal path. Under the worst case condition where the isolation between the TX and RX is only 20dB and the maximum gain of the canceler is -20dB, the NF degradation due to the cancellation path will be 0.4dB, see Fig. 4(b). This is equivalent to a noise resistance of at least 250 Ω, looking back into the canceler from the RX point of injection, which is much higher than the 50Ω impedance of the antenna. Intuitively, this is similar to the situation of minimizing the G_m of the active load current sources used in differential pair [28]. In the case of canceler and active load, the device is outside of the main signal path, requiring a minimization in the device G_m. Non-minimum length devices (>40nm) will likely be employed for G_m stage for two reasons. First, the excessive noise coefficient γ gets smaller for a longer channel-length device [27]. Second, a longer channel length leads to a higher device output impedance, which will minimize the impact on the RX input matching network.

C. *Example Compact Low Power Active Canceler*

As an example of replacing the passive components with active transistor in a feedforward canceler, the following low-energy Bluetooth FD radio is highlighted. This feedforward effectively implements a Cartesian rotator (Fig. 5) to track both the TX carrier phase and gain.

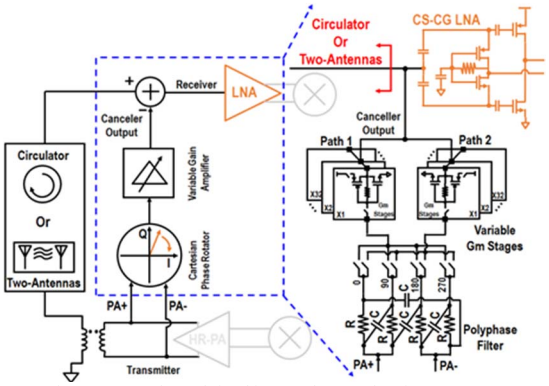
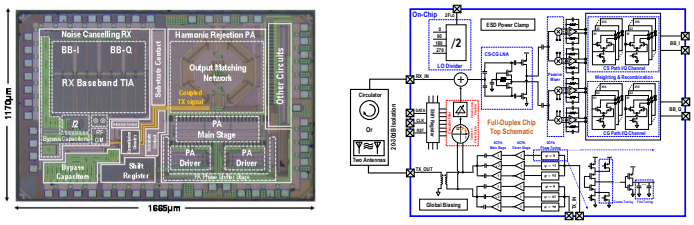


Fig. 5. Cartesian-Rotator based feedforward canceler from PA output to LNA input.



(a) (b)

Fig. 6. Bluetooth FD front-end chip (a) Die Photo, (b) Block Diagram.

This SI feedforward canceler is connected between the PA output and the LNA input which utilizes a polyphase filter (PPF) to generate roughly four equal amplitude signals with a phase difference of 0º, 90º, 180º and 270º, see Fig. 5. The canceler phase and gain tuning is performed by first selecting two of the four phases at the PPF output. These two signals which have an approximate 90º phase difference, are each weighted using variable gain transconductance stages. The two outputs are combined, to produce a vector sum which is equal in amplitude and phase to the leakage signal. This approach effectively applies a Cartesian rotator to the cancellation path by generating a vector signal copy of the TX-leakage signal.

To reduce the effect of loading on both the PA output and LNA input matching network, the canceler input and output impedances are greater than 900Ω and 500Ω, respectively. Since the frontend leakage media attenuates the SI signal by at least 20dB, any active circuitry in the cancellation path must attenuate the signal by an equal amount (20dB) to match the leakage magnitude. The canceler output is a current-mode signal generated by a set of low-power G_m stages which consume less than 0.3mA. Compared to prior transformer-based cancelers [26], this cancellation circuit requires significantly less die area. Adding active devices at the RX input usually introduces a non-negligible NF degradation. However, the noise injected into the RX path, from the canceler, is minimized by two features: 1) the cancellation path maximum gain is -20dB, 2) the required low gain of the G_m stage is exploited to increase the equivalent noise resistance (250Ω) looking into the canceler output. Therefore, the canceler contribution to the RX NF is near negligible, less than 0.6dB.

This Cartesian-based Feedforward canceler was integrated with a Harmonic-Rejection PA along with a complete receive signal path in a 40nm TSMC CMOS technology. This FD chip achieves a 30dB same-channel SI cancellation over a 4MHz BW. Although a relatively narrowband solution, this canceler occupies minimal silicon area (131μmx131μm), has a RX NF degradation of 0.6dB and consumes less than 0.25mW. A more in-depth description of this chip is given in [29] with the results summarized in Table 1, while a chip die photo and block diagram are shown in Fig. 6.

III. Linearity Issues in Post PA Interference Cancellation Circuits

Ultimately, utilizing frontend components which provide suppression of transmitted signals with a high output power PA

(24dBm) and sophisticated multi-carrier modulation methods will demand linearity performance which may be challenging to achieve using purely an electronic solution. Take a feedforward canceler as an example, see Fig. 1, the PA delivers a multi-carrier signal which is fed into the canceler and coupled to LNA input with a proper inverse response for cancellation . The canceler with limited linearity generates a bunch of inter-modulation products which is also known as spectral regrowth. The nonlinearities injected from the canceler at LNA input act as an added noise floor to the RX input that will degrade the sensitivity of the RX. For example, a PA transmits a two-tone signal at the canceler input with an output power of 24dBm (21dBm each tone). For a 20dB isolation between the PA the LNA, the canceler gain is set to be -20dB to match the SI signal at LNA input, which introduces two 1dBm-power tones at the LNA. Now, assuming a -90dBm RX noise floor at the LNA input and leaving 10dB as the margin, the third-order intermodulation products need to be as low as -100dBm. This makes the required input IP3 of the canceler to be 71.5dBm (101/2+21dBm) which is unachievable if purely an electronic solution is used.

While significant prior work has performed the non-linear models of components at the output of the a PA for a variety of elements [30], [31], this analysis attempts to simplify the linearity challenge for the CMOS technology, by reducing the problem to a high-output power signal driving a simple switch, or even a junction drain capacitance.

When a switch is biased in a triode region (ON state, V_{GS}=V_{DD}), a large signal swing at a drain/source node modulates the on-resistance r_{on} which produces nonlinearity. However, even if the switch is in the OFF state (V_{GS}=0), the large signal swing also modulates reverse-biased junction capacitances of the transistor which contributes nonlinear currents flowing into the signal path.

Here we first analyze the nonlinear behavior of a simple reverse-biased diode. The junction capacitance of a diode, C_j, is expressed as:

$$C_j = A\frac{C_{j0}}{\left(1+\frac{V_R}{V_j}\right)^{m_j}} \tag{4}$$

where A is the area of the junction, C_{j0} is the junction capacitance at zero bias, V_R is the reverse-biased voltage, V_j is the junction built-in potential, and m_j is the bottom junction capacitance grading coefficient. To derive the linearity of a reverse-biased diode, a simple circuit is used that includes a reverse-biased diode and a linear capacitor in parallel, Fig. 7(a). C_j is the junction capacitance of the diode and C_L is a linear capacitance from signal routings and other parasitic. In this setup, the DC content of V_R is 0V while an AC two-tone signal, $A\sin\omega_1 + A\sin\omega_2$ is applied to V_{ac}. The IIP3 can thus be derived as [32]:

$$A_{IP3} = 2\times\sqrt{\frac{C_j + C_L}{\frac{C_j}{1+\frac{V_R}{V_j}}\frac{m_j(m_j+1)}{{V_j}^2}}} \tag{5}$$

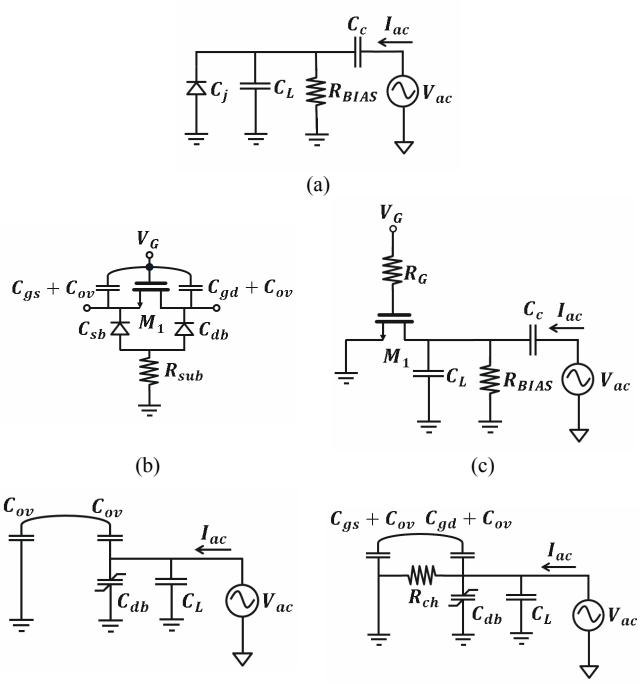


Fig. 7. (a) A test circuit for a simple diode; (b) Capacitances in a NMOS transistor; (c) A test circuit for a NMOS transistor as a switch; (d) The equivalent circuit when the switch is OFF; (e) The equivalent circuit when the switch is ON.

Eq. (5) shows that a reverse-biased junction capacitor contributes to nonlinearity.

Now consider a NMOS switch which be modeled by several capacitances and diodes, as shown in Fig. 7(b). C_{sb} and C_{db} are the junction capacitances. C_{gs}, C_{gd}, and C_{ov} are the capacitances formed between gate and drain/source. R_{sub} is the substrate resistance which is assumed to be zero in this analysis. A simple circuit is used to examine the linearity of a NMOS switch, see Fig. 7(c). V_G sets the ON/OFF state for transistor M_1 through resistor R_G, while the resistor R_{BIAS} pulls the drain node to ground, which again makes the reverse-biased voltage of the drain diode to be 0V. C_C and C_L are linear ac-couple capacitor and linear parasitic capacitance from the of signal routing parasitic, respectively.

When the switch is OFF, effectively C_{gs}=C_{gd}=0. The equivalent circuit is simplified as shown in Fig. 7(d). The nonlinear capacitance C_{db} is composed of three parts: bottom, oxide- and gate-edge sidewall junction capacitances, which is given as [33]:

$$C_{db} = A_d\frac{C_{j0}}{\left(1+\frac{V_R}{V_j}\right)^{m_j}} + (P_d - W)\frac{C_{jsw0}}{\left(1+\frac{V_R}{V_{jsw}}\right)^{m_{jsw}}} + W\frac{C_{jswg0}}{\left(1+\frac{V_R}{V_{jswg}}\right)^{m_{jswg}}} \tag{6}$$

where A_d is the area of drain, P_d is the periphery of drain, C_{jsw0} and C_{jswg0} are the oxide- and gate-edge sidewall junction capacitance per length, V_{jsw} and V_{jswg} are the oxide- and gate-edge sidewall built-in potential, m_{jsw} and m_{jswg} are the oxide- and

$$A_{IP3} = 2 \times \sqrt{\frac{C_{db} + C_L}{C_j \frac{m_j(m_j+1)}{V_j^2} + C_{jsw} \frac{m_{jsw}(m_{jsw}+1)}{V_{jswg}^2} + C_{jswg} \frac{m_{jswg}(m_{jswg}+1)}{V_{jswg}^2}}} \quad (7)$$

$$A_{IP3} = \sqrt[4]{\frac{\left(\mu_0 C_{ox}(V_{GS} - V_T)\left(\frac{W}{L}\right)\right)^2 + \omega^2 (C_{db} + C_L)^2}{\left(\mu_0 C_{ox}\left(\frac{W}{L}\right)\right)^2 \left(\frac{3}{8LE_c}\right)^2 + \left(\frac{C_j}{4}\frac{m_j(m_j+1)}{V_j^2} + \frac{C_{jsw}}{4}\frac{m_{jsw}(m_{jsw}+1)}{V_{jsw}^2} + \frac{C_{jswg}}{4}\frac{m_{jswg}(m_{jswg}+1)}{V_{jsw}^2}\right)^2}} \quad (8)$$

gate-edge side wall junction capacitance grading coefficients. When $V_{ac}=A \sin \omega_1 + A \sin \omega_2$, the IIP3 is obtained as Eq. (7). In this particular circuit, the linearity is determined by the ratio between the linear capacitance C_L and the nonlinear capacitance C_{db}. There are not many things can do to improve the linearity except for reducing the transistor size, thus lowering the nonlinear current generated from the junction capacitances.

On the other hand, when switch is ON, the equivalent circuit is shown in Fig. 7(e), where R_{ch} is the nonlinear channel resistance. The IIP3 of the circuit is derived as Eq. (8), where E_C is the critical field strength (V/m).

The above test circuits are calculated and simulated using TSMC 40nm CMOS process with C_L=500fF and two-tone signals at 2.4 and 2.401GHz. Fig. 8(a) shows the simulated results of VIP3 for a diode junction capacitance as shown in Fig. 7(a). The results show consistency between Spice simulation and the calculation. For a diode size of 200μm×0.04μm, which the junction capacitance is 10.7fF, Eq. (5) gives us a VIP3 of 23dBV or 33dBm when the diode is in parallel with a 50Ω impedance. On the other hand, for an OFF-state NMOS switch of the same 200μm×0.04μm size, the nonlinear capacitance is 76fF, resulting in a VIP3 of 13dBV, as shown in Fig. 8(b). In both the case of a diode and an OFF NMOS switch, the linearity drops as the diode/switch size increases, because the nonlinear AC portion of the total current I_{ac} increases.

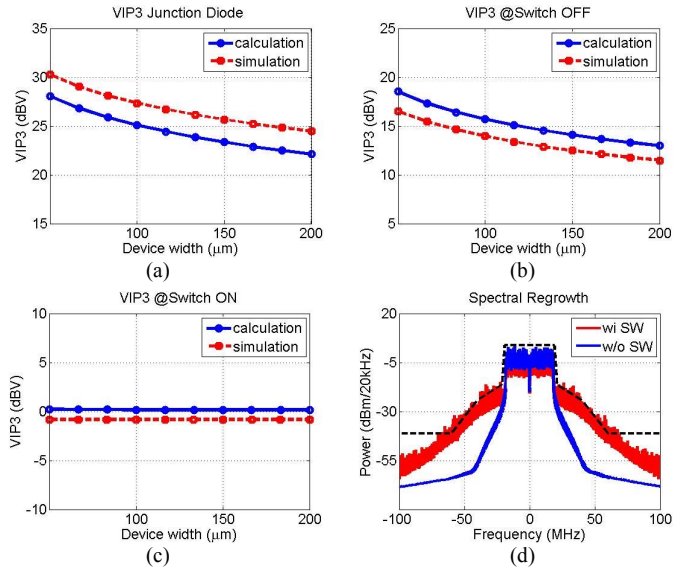


Fig. 8. The calculation and Spice simulation results of IP3: (a) Diode junction capacitance, (b) NMOS switch is OFF, (c) NMOS switch is ON; and (d) The spectral regrowth due to limited switch linearity.

When the switch is on (Fig. 7e), the I_{ac} is almost equal to the nonlinear current generated by R_{ch} because the on-resistance is low. The VIP3 is 0dBV for different width as shown in Fig. 8(c).

The insufficient linearity of an interface circuitry at TX output causes several problems. One of them is the spectral regrowth. As an example in WiFi with a 40MHz OFDM signal, the TX emission mask fails when an ideal PA delivers 29dBm output power through a 35dBm IIP3 switch, see Fig. 8(d). As mentioned in Section II, in FD applications, the insufficient linearity of a TX-RX interface circuit creates intermodulation products that not only increase the RX noise floor but also limit the maximum achievable SI cancellation from the feedforward cancelers.

A commonly used technique to improve the linearity of the MOS switches is by adding linear resistors/capacitors to build a voltage divider to reduce the voltage swing seen at drain/source nodes of the MOS switches [34]. Another method is to form a current divider to reduce the nonlinear portion of the total signal current [35]. Nonetheless, these methods still have limitations that make the TX-RX interface circuit implementation with high linearity remain extremely challenging. In fact, for high power output applications, an electronic solution to implement the circulator may not be possible, leaving the solution to the domain of other materials such as [36], [37].

IV. Broad Channel Bandwidth TX SI Cancellation

The design of a high-performance wideband SI canceler is challenging due to fact that there are multiple time delay paths

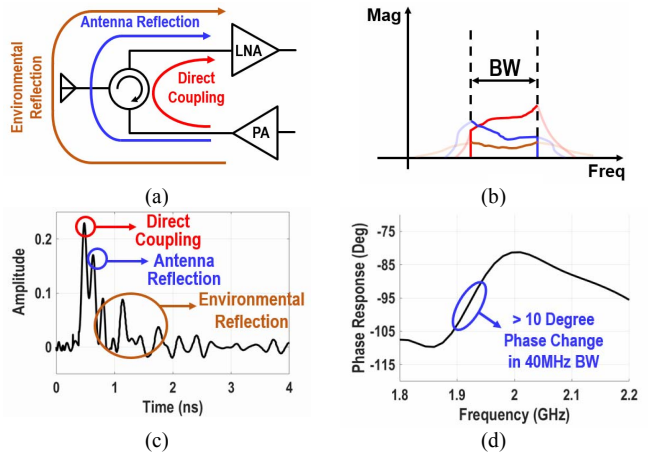
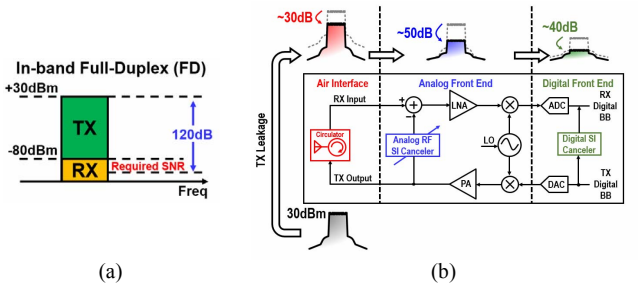


Fig. 9. Channel response of the leakage path (a) Multiple time delay paths of the leakage signal coupled from PA output to LNA input, (b) Frequency response for each time delay versions of the leakage signal, (c) Impulse response of a discrete circulator from Meca Electronics, (d) Phase response of the measured discrete circulator.

of the SI signal, over the channel BW of interest. A transceiver ntend with a circulator and a single TX/RX shared antenna is used to illustrate this concept, Fig. 9. The SI is a combination of several leakage paths (Fig. 9a) which include: 1) a direct-coupling path through the circulator, chip and board substrate, 2) reflection from the antenna due to the imperfect matching between the antenna and RX, and 3) a combination of other environmental reflections from nearby objects (e.g. human ear, metal objects, etc). Each of the SI leakage paths will have a different frequency response and transfer function, Fig. 9(b). If it is assumed that each leakage path is linear time-invariant (LTI), the overall leakage channel response can be modeled as a combination of the frequency response of each leakage path. To better understand the existence of multiple time-delayed coupling paths between the TX and RX, measurements were made of a commonly found discrete circulator (Meca Electronics #CS-1.950) using a network analyzer and the results of which are shown in Fig. 9(c) and (d). The measured phase response of the circulator from the TX to the RX port shows a significant change (10 degrees) over a BW of 40MHz due to the multiple time-delayed coupling paths, see Fig. 9(d). As such, to realize a wideband suppression of the TX-to-RX SI, the canceler must provide an inverse channel response of all the summed leakage paths.

Several recent research efforts attempt to achieve wideband and high SI cancellation using a single feedforward path [38] or a single point of injection [39]. In [38], a 2nd order G_m-C N-path filter was used to perform frequency domain equalization. However, a high-frequency multiphase clock network must be distributed to a set of switches, which likely dissipate considerable power. An alternative method synthesizes an inverse leakage signal at the LNA input using a current DAC and up-conversion mixer [40]. However, for applications requiring a high RX sensitivity, the DAC quantization noise will likely degrade the RX sensitivity. Thus, it is challenging to achieve sufficient SI suppression using a single feedforward path for a wideband TX signal, in situations where a high-power PA operates simultaneously with a high sensitivity RX. Moreover, the cancellation DAC at the RX input cannot capture the broadband noise and nonlinearities produced by the TX. Generally speaking, any on-chip single-component cancellation circuit will be challenged to reliably achieve more than 50dB suppression/cancellation. Examples might include single-sideband mixers [41], filters and harmonic rejection mixers [42], [43].

The remainder of this paper explores a SI cancelling architecture that overcomes those aforementioned challenges by



(a) (b)

Fig. 10. SI cancellation in FD communication (a) SI cancellation requirement in a FD radio with TX output power of 27dBm and RX required sensitivity of -80dBm, (b) SI cancellation distributed in the RX chain.

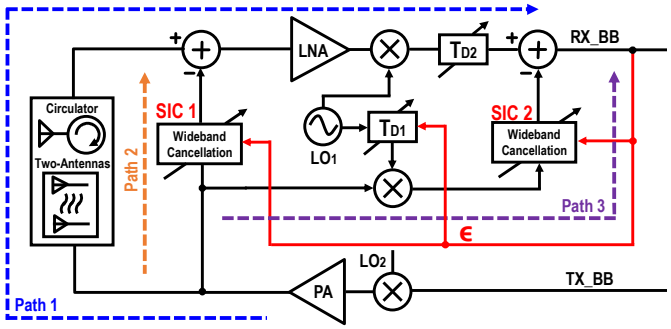


Fig. 11. Dual-injection path self-interference canceling architecture.

performing SI cancellation at multiple points in the RX [44], [45], [46]. This is followed by an expanded description of the prototype chip, which was first given in [19].

A. A Dual-Injection Point Feedforward Canceler

To achieve both broad BW and deep SI suppression for evolving 5G standards, filtering and cancellation techniques must be capable of tracking the TX SI channel response produced by multiple leakage paths. As an example, in some cellular mobile radios, the transmitter delivers a 30dBm output power and receiver has a sensitivity requirement of -80dBm. For a modulation scheme requiring a 10dB SNR, a SI cancellation of 120dB is needed, Fig. 10(a). To achieve such a high SI suppression, distributing multiple suppression techniques along the receiver chain seems reasonable, see Fig. 10(b) for a possible distribution.

This transceiver makes the use of a dual-injection path SI cancelling architecture which allows more design freedom to achieve both a deeper attenuation of TX leakage over a broader BW, see Fig. 11. Two analog cancelers, both of which have their inputs attached to the TX output matching network, are designed to properly capture not only the TX carrier signal, but also the noise and non-linear distortion introduced by the TX.

The first RF canceler resides between the PA output and the RX LNA input, with the primary function of reducing the TX SI power sufficiently, to prevent the RX frontend from saturating. This has the effect of relaxing the required linearity for the LNA and all the subsequent RX blocks. The second baseband canceler down-converts the leakage signal using a mixer, allowing a low-frequency implementation of a more complex, higher order, and longer delayed analog cancelling filter. The baseband canceler has an added advantage of capturing and cancelling the TX leakage reciprocal mixing with the LO phase noise (PN) in the RX signal path. The combination of both cancelling filters, with their outputs injected at different points in the RX chain, provides a wideband and high SI cancellation. More details covering the design of this dual-injection point canceling architecture are discussed in the next section.

The BB canceler design uses a 14-tap adaptive filter. Each of the BB TTD blocks are similar to [47] and has a simulated 10ns time delay. The mixers used in the RX signal chain and BB canceler paths (path 3) utilize the same LO signal (LO_1), but have a delay mismatch between them. Thus, a variable delay (T_{D1}) in the LO output that supplies the path 3 mixer, compensates for the path 1-3 delay mismatch (see Fig. 12).

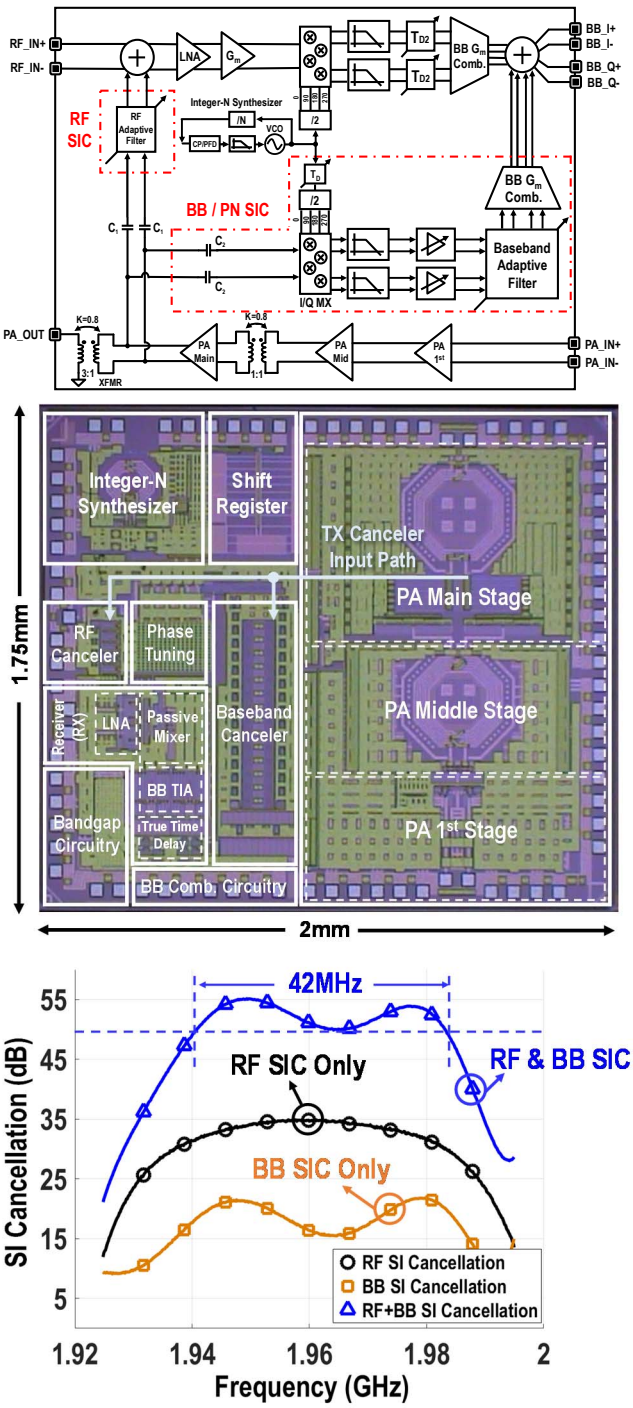


Fig. 12. Dual-injection path FD canceler block diagram (top), die photo (center), and measured SI suppression (bottom).

Combining the BB canceler and T_{D1} allows suppression of both the TX SI and RX LO sidebands.

This dual-path FD architecture has a measured SI suppression of 50dB over a 42MHz BW. Moreover, the reciprocal mixing of the TX SI in the receive path is suppressed by more than 10dB. A more through description of this chip is given in [44], while a summary of data related to this chip is present in Table 1. A block diagram, chip photo and measured SI Cancellation is presented in Fig. 12.

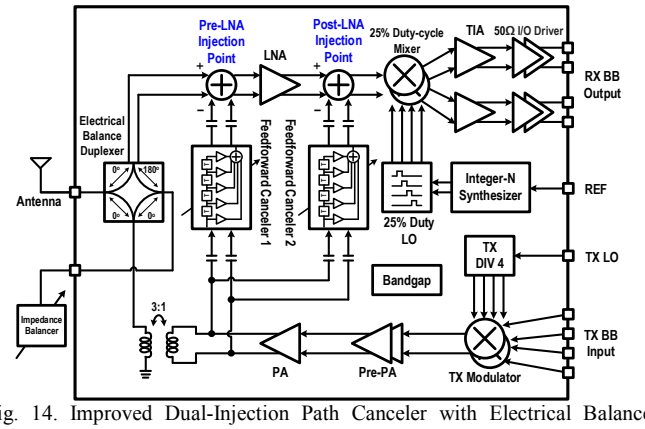


Fig. 14. Improved Dual-Injection Path Canceler with Electrical Balance Duplexer to allow both FD and FDD operation.

B. Dual-Path Canceler with Electrical Balance Duplexer (EBD) for FD and FDD operations

The aforementioned dual-injection path FD chip is able to achieve some level of transmitter PN suppression by time matching the baseband cancellation and RX paths. However, this approach relies on a high correlation in the PN between the local oscillators (LO) used by the RX mixers and baseband cancellation path mixers. As such, if the transmit carrier frequency is different than the receiver carrier frequency as in FDD systems, the TX PN skirts will no longer be suppressed in this approach. Thus, the last transceiver presented attempts to provide TX SI cancellation when the radio is operating in both FD and FDD mode.

In contrast to the previously described dual-injection path canceler, this radio implements three components (versus two) along the RX signal chain, each contributing to TX SI cancellation, these include an integrated electrical balance duplexer (EBD) between the TX, RX and antenna ports, in addition to a new dual-point injection feedforward canceler between the TX and RX, see Fig. 14.

The two points of injection for these feedforward cancelers, which are along the receiver chain of this dual-path architecture,

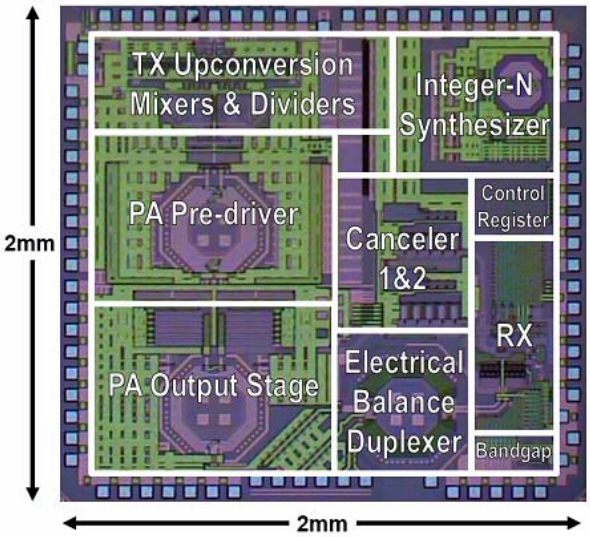


Fig. 13. Die photo of improved dual-injection path radio with EBD implemented in a 40nm TSMC CMOS process.

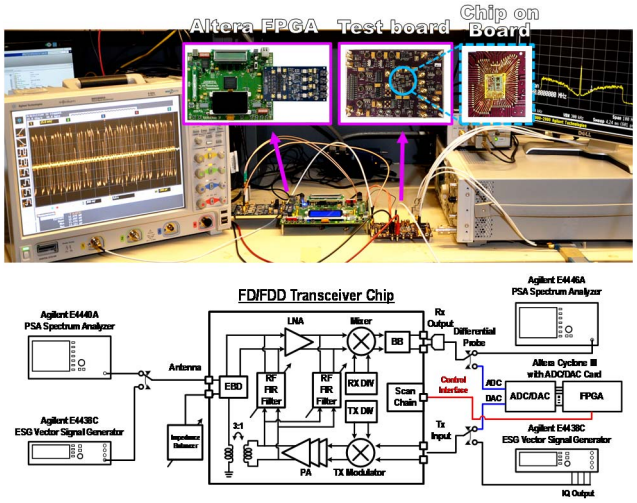


Fig. 15. Test setup which includes a FPGA board to emulate the digital baseband and perform real-time calibration.

are at the LNA input (similar to [44]), and at the LNA - RX downconversion mixers interface, Fig. 14. This obviates the need for the complex I/Q auxiliary downconversion mixers and the analog FIR filters as in [44]. Moreover, the second cancellation path has now been moved to earlier in the RX chain, thus reducing the linearity demand on the RX downconversion mixers and filters in the analog baseband. There is also an advantage as a far lower fractional-BW is required in the 2nd cancellation path, as compared to [44] which is 100%. Further benefits of this dual-path architecture relate to the method for TX broadband and PN suppression in the receiver. Unlike the work in [44], which only performs suppression of the TX reciprocal mixing products when both the TX and RX utilize the same carrier frequency, the pre- and post-LNA cancellation

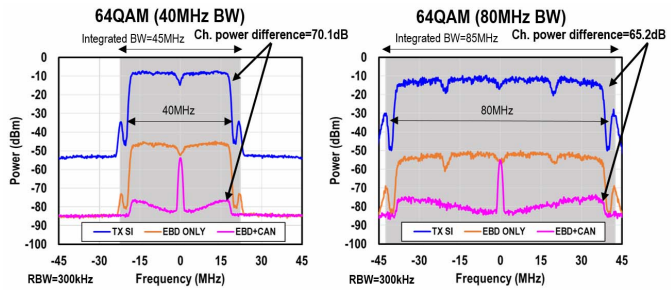


Fig. 16. Measured SI cancellation using IEEE 802.11 (OFDM multicarrier) sample packets with different bandwidths.

networks in this work can be set to suppress the TX carrier and/or noise when in FDD mode, independent of the RX and TX carrier frequencies.

The TX chain is composed of an upconversion mixer with LO dividers/drivers and a class AB power amplifier. The RX signal path includes a transconductance (Gm) LNA, a passive mixer driven by 25% duty-cycle LO, followed by a transimpedance amplifier. An integer-N synthesizer is implemented to provide the LO signals for the RX. Both the integrated EBD and a transformer at the PA output, eliminate the need for off-chip RF components including a circulator and RF baluns.

This transceiver employs an EBD and two low-power, compact, and wideband cancelers to achieve high SI cancellation (Fig. 14). The EBD achieves a high TX-to-RX isolation (~39dB) over a wide BW (200MHz) [30]. The inputs of both cancelers are connected to the PA output matching network, to capture the TX carrier signal, along with the PN and harmonics generated by the TX BB nonlinearities. A combination of the EBD and the two-path feedforward canceler

Table 1: Comparison of recently published Full Duplex transceivers and components, including circulators.

		S. Ramakrishnan RFIC' 2017 [39]	J. Zhou ISSCC' 2015 [37]	N. Reiskarimian ISSCC' 2017 [30]	B. Liempd TMTT' 2017 [34]	I. Fabiano TMTT' 2017 [23]	V. Broek JSSC' 2015 [45]	T. Zhang JSSC' 2015 [25]	T. Zhang ESSCIRC' 2017 [28]	T. Zhang ISSCC' 2017 [43]	K. Chu ISSCC' 2018 [44]
Architecture		VM-downmixer	Frequency Domain Equalization	Duplexing LNA	EBD + SAW Filter	EBD + Rx	SIC VM-downmixer + Mixer-first RX	Transformer Coupling	Poly-phase Filter + Active Gm Stage	Dual-path + Adaptive Filter	EBD + Double-RF Adaptive Filter
Technology		65nm	65nm	65nm	0.18um SOI	28nm	65nm	40 nm	40 nm	40 nm	40 nm
Frequency Range (GHz)		0.15 - 3.5	0.8 - 1.4	0.61 - 0.975	0.7 - 1.0	1.7 - 2.1	0.15 - 3.5	1.8 - 2.4	2.4	1.7 - 2.2	1.6 - 1.9
TX SI	TX_{out}-to-RX_{in} Iso. (dB)	N/A External Circulator	30-50 External Circulator Two-antenna	40[e] On-chip Circulator	50 On-chip EBD	40 On-chip EBD	25 Two-antenna	50 External Duplex Filter	20-30 External Circulator Two-antenna	30-35 External Circulator	39[a] On-chip EBD
	Total On-chip SIC Depth (dB) / BW (MHz)	64 / 20	20 / 25 (15)[h]	40 / 20	50 / 10 (SAW) 50 / 2 (EBD)	45 / 14	21 / 16	20 / 3.84	30 / 4	50 / 42	72.8 / 20[h] 70.1 / 40[c] 65.2 / 80[d]
RX Gain (dB)		35	27 - 42	28	7.5	35	24	18	45	36	42
Noise Figure (dB)		3.6	4.8	6.3	7.6	6.7	10.3 - 12.3	5	4.5	4	8.0 (EBD 5.6)
SIC NF Degradation (dB)		3.4[g]	1.1---1.5 (0.9-1.2)[h]	1.7	N/A	N/A	4	0.1	0.6	1.5	1.6
Canceller Area (mm^2)		N/A	N/A	N/A	N/A	N/A	N/A	~ 0	0.015	0.349 (RF+BB)	0.12 (RF*2)
SI Circuitry Power (mW)		N/A	44 - 91[i]	36[f]	0 (passive)	0 (passive)	1 - 10	0 (passive)	0.25	11.5 (RF+BB)	14.3 (RF*2)
Canceller IIP3 (dBm)		N/A	N/A	N/A	N/A	N/A	21.5[i]	N/A	15	36 (RF) / 34.5 (BB)	N/A
TX-ANT Path IIP3 (dBm)		N/A	N/A	30	58	50	N/A	N/A	N/A	N/A	N/A
Max TX Operating Power (dBm)		17	N/A	8	24	N/A	3.6	30	0	15	10
TX SI to RX LO Suppression (dB)		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	10	11
Integrated TX Upconversion Path		No	No	No	No	No	No	No	No	No	Yes
Integrated PA		Yes	No	No	No	No	Yes	No	Yes	Yes	Yes
Integrated PLL		No	No	No	No	No	No	No	No	Yes	Yes
Active Area (mm^2)		6.25	4.8	1.5	6.62	0.72	2	2.08	1.93	3.5	4

[a] Measured with on-chip test structure. [b] Measured channel power difference with 20MHz 64QAM and 22MHz integration BW. [c] Measured channel power difference with 40MHz 64QAM and 45MHz integration BW. [d] Measured channel power difference with 80MHz 64QAM and 85MHz integration BW. [e] Averaged over 20MHz. [f] Antenna interface. [g] Calculated by the difference between system NF and RX NF. [h] Measurement with an antenna pair, 15MHz BW, 0.9-1.2dB NF deg. is with one filter, 25MHz, 1.1-1.5dB NF deg. is with two filters. [i] power including 0-47mW Gm cells and 44mW LO for one buffer.

in this work, achieves more than >70dB cancellation over 40MHz (Fig. 16).

A 2-to-4 turn ratio EBD provides both a single-ended-to-differential conversion and the LNA noise matching (Fig. 14). The LNA is implemented with a current-reuse Gm stage, which provides a current-mode output to drive the passive downconversion mixers. Both PMOS and NMOS tail currents are utilized in the LNA to provide a first-order rejection of any common-mode signals generated by the EBD [30]. A 1-to-3 transformer is placed between EBD and PA, to translate the 50Ω impedance of the antenna down to 6Ω, which is the r_{opt} for the PA output.

This transceiver chip was fabricated in TSMC 6L 40nm LP CMOS process with a die size of $4mm^2$ and consumes 106mW (w/o PA). The EBD occupies an area of $0.23mm^2$ while both RF cancelers occupy an area of $0.12mm^2$ (Fig. 13). An Altera Cyclone III FPGA with 14bit ADC/DACs operating at 100MHz is used to emulate the digital BB and close the filter adaptation loop (Fig. 15). The FPGA finds optimal codes for the canceler weights in real time with a gradient descent algorithm. The on-chip self-interference cancellation is tested by applying a 20/40/80MHz OFDM multicarrier 64QAM modulated signal, and a measured channel power difference of 72.8/70.1/65.2dB (maximum 77.6dB from a single-tone sweep) is obtained with an integration BW of 22/45/85MHz, respectively (Fig. 16). A more through description of this chip is given in [45], while the key data of this chip is summarized in Table 1.

V. Conclusion

This paper presented an overview of numerous methods for transmitter self-interference cancellation towards FD and FDD integrated radios. At present, the field appears very promising with respect to achieving performance which would allow full duplex operation for commercial standards-based radios. Several groups around the world have demonstrated SI cancellation well above 50dB. While the implementation of a circulator for high TX output power applications appears challenging due to the extreme demand on linearity, other non-electronic solutions appear promising, possibly enabling a complete radio solution using a multi-chip module (MCM). Overall, the field is promising with many novel solutions yet to come.

VI. Acknowledgements

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