9.7 A Broadband and Deep-TX Self-Interference Cancellation Technique for Full-Duplex and Frequency-Domain-Duplex Transceiver Applications

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Full-Duplex (FD) radios, capable of simultaneously transmitting and receiving on the same frequency, have evolved as one method to address future demand for higher data-rates. Although recent highly integrated full-duplex radios [1-4] show promise towards improving spectral efficiency by >1.9× [5], mitigating transmitter (TX) self-interference (SI) for broad-bandwidth signals remains a major challenge, particularly for longer range transceivers requiring a high-output-power PA. This paper describes a CMOS transceiver with a deep TX SI cancellation performance over a very wideband (65dBc/80MHz and 70dBc/40MHz).

Achieving sufficient TX SI cancellation depth and bandwidth for envisioned 5th-Generation standards using a single component is quite challenging. However, cascading several SI cancellation techniques as the signal passes down the receiver chain appears promising to achieve high TX SI attenuation as was done with a two-point injection architecture in [3]. This approach utilized two feedforward cancelers, where both inputs are supplied by the TX output, with a high-frequency multitap adaptive FIR filter supplying a cancellation signal to the LNA input, while the second cancellation path frequency-translated the signal to baseband, where a complex analog adaptive I/Q filter further suppressed the TX SI [3]. However, the BB I/Q filters require many taps and occupy significant silicon area as compared to the equivalent RF filter implementation. In addition, calibrating both complex filters is challenging and any residual imbalance between the I and Q paths limits the cancellation performance. In contrast, this radio implements three components (versus two) along the RX signal chain, each contributing to TX SI cancellation. These include an integrated electrical balance duplexer (EBD) between the TX, RX and antenna ports, in addition to a new dual-point injection feedforward canceler between the TX and RX, see Fig. 9.7.1.

The two points of injection for these feedforward cancelers, which are along the receiver chain of this dual-path architecture, are at the LNA input (similar to [3]), and at the LNA -RX downconversion mixers interface (Fig. 9.7.1). This obviates the need for the complex I/Q auxiliary downconversion mixers and the analog FIR filters as in [3]. Moreover, the second cancellation path has now been moved to earlier in the RX chain, thus reducing the linearity demand on the RX downconversion mixers and filters in the analog baseband. There is also an advantage as a far lower fractional-BW is required in the 2nd cancellation path, as compared to [3] which is 100%. Further benefits of this dual-path architecture relate to the method for TX broadband and phase-noise (PN) suppression in the receiver. Unlike the work in [3], which only performs suppression of the TX reciprocal mixing products when both the TX and RX utilize the same carrier frequency, the pre- and post-LNA cancellation networks in this work can be set to suppress the TX carrier and/or noise when in FDD mode, independent of the RX and TX carrier frequencies, Fig. 9.7.2.

The TX chain is composed of an upconversion mixer with LO dividers/drivers and a Class-AB power amplifier. The RX signal path includes a transconductance (Gm) LNA, a passive mixer driven by a 25% duty-cycle LO, followed by a transimpedance amplifier. An integer-N synthesizer is implemented to provide the LO signals for the RX. Both the integrated EBD and a transformer at the PA output eliminate the need for off-chip RF components, including a circulator and RF baluns.

This transceiver employs an EBD and two low-power, compact, and wideband cancelers to achieve high SI cancellation (Fig. 9.7.2). The EBD achieves a high TX-to-RX isolation (~39dB) over a wide bandwidth (200MHz) [6]. The inputs of both cancelers are connected to the PA output matching network to capture the TX carrier signal, along with the phase noise and harmonics generated by the TX BB nonlinearities. A combination of the EBD and the two-path feedforward canceler in this work achieves more than 70dB cancellation over 40MHz (Fig. 9.7.5).

A 2-to-4 turns ratio EBD provides both a single-ended-to-differential conversion and the LNA noise matching (Fig. 9.7.3). The LNA is implemented with a current-reuse Gm stage, which provides a current-mode output to drive the passive downconversion mixers. Both PMOS and NMOS tail currents are utilized in the LNA to provide a first-order rejection of any common-mode signals generated by the EBD [6]. A 1-to-3 transformer is placed between EBD and PA, to translate the 50Ω impedance of the antenna down to 6Ω, which is the r_{opt} for the PA output.

Each RF canceler consists of a 5-tap FIR filter to emulate the inverse response of multiple TX leakage paths [3], see Fig. 9.7.3, where each tap includes an 8b (signed-magnitude) variable-G_m amplifier and a push-pull interstage buffer to drive an RC-CR allpass filter with a measured time delay of 50.9ps (Fig. 9.7.5). The push-pull buffer improves the canceler IIP3 by 3dB as compared to [3]. Both RF cancelers supply a current output signal which is summed with a current-mode signal in the RX path. Each canceler presents a high impedance at both the input (~3kΩ) and output (~1kΩ) to prevent loading the PA output and LNA input/output. To further improve the canceler linearity, an attenuator is placed prior to both cancelers' inputs. The simulated IIP3 of the canceler is +40dBm; a direct measurement of the canceler IIP3 is not possible as both the TX and RX paths are integrated from baseband to the antenna port on the TX side, and from the EBD input to the RX baseband. Also, for the sake of clarity, the IIP3 simulation was performed by placing the PA output r_{opt} (6Ω differential resistance) at the canceler input, which is significantly lower than the real part resistance looking into just the canceler itself (~3kΩ). This simulation approach most accurately reflects the voltage levels experienced at the canceler input when the PA is at maximum output power.

This transceiver chip was fabricated in TSMC's 6L 40nm LP CMOS process with a die size of 4mm^2 and consumes 106mW (w/o PA). The EBD occupies an area of 0.23mm^2 while both RF cancelers occupy an area of 0.12mm^2. An Altera Cyclone III FPGA with 14b ADC/DACs operating at 100MHz is used to emulate the digital BB and close the filter adaptation loop (Fig. 9.7.4). The FPGA finds optimal codes for the canceler weights in real time with a gradient descent algorithm. The EBD was characterized using an on-chip test structure and has a measured TX-to-RX isolation of 39dB over 200MHz. The RX operates from 1.6GHz to 1.9GHz with a measured gain of 42dB and a total noise figure (NF) of 8.09dB, 5.6dB of which was contributed by the measured passive loss of the EBD. The PA has a measured output P_{-1dB}/P_{sat} of 10.6dBm/12.5dBm. The measured locking range of the integer-N synthesizer is 3.52 to 4.28GHz while consuming 10.4mW with a PN of -117dBc/Hz @1MHz offset.

The on-chip self-interference cancellation was tested by applying a 20/40/80MHz OFDM multicarrier 64-QAM modulated signal, and a measured channel power difference of 72.8/70.1/65.2dB (maximum 77.6dB from a single-tone sweep) was obtained with an integration bandwidth of 22/45/85MHz, respectively (Fig. 9.7.6). The noise figure degradation due to the TX leakage signal dropped from 8dB to 1.6dB after turning on both RF cancelers. TX SI reciprocal mixing with the RX LO phase noise was also significantly reduced by 11dB (Fig. 9.7.5), because all cancellation occurs prior to the RX mixers.

A tabular performance comparison is given in Fig. 9.7.6, and the die micrograph is presented in Fig. 9.7.7. A complete transceiver system with the entire analog TX upconversion and RX downconversion paths demonstrates the feasibility for FD radios with more than 72.8/70.1/65.2dB on-chip SI cancellation over 20/40/80MHz bandwidths, respectively. This was achieved by cascading three TX-to-RX isolation blocks along the receiver signal chain.

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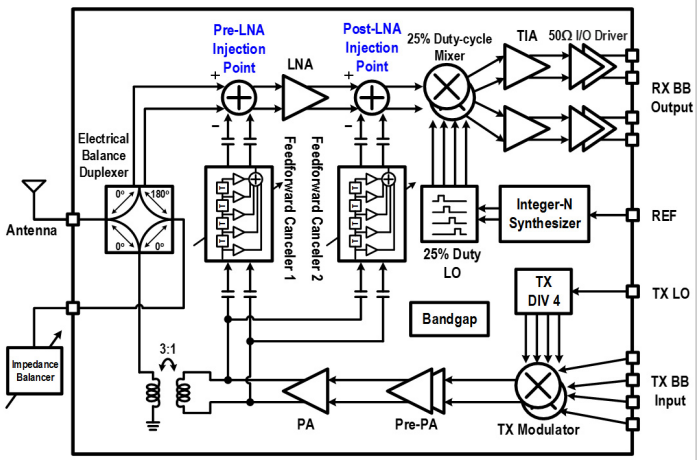

Figure 9.7.1: Block-level diagram of FD/FDD transceiver architecture.

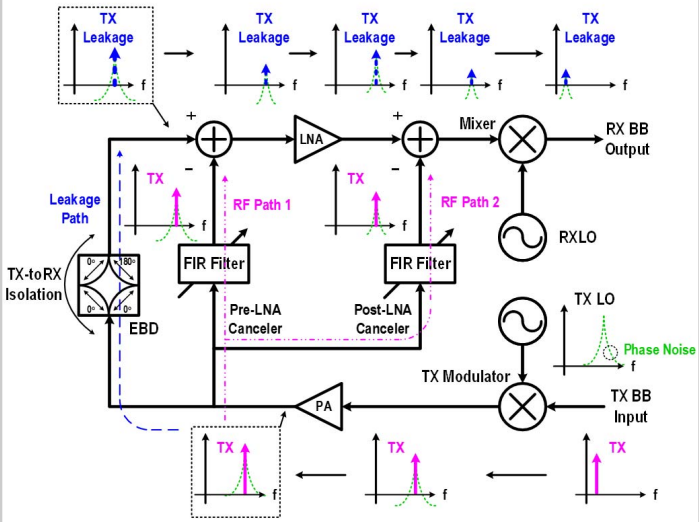

Figure 9.7.2: Conceptual diagram of TX self-interference suppression as signal passes from the transmitter through the receiver.

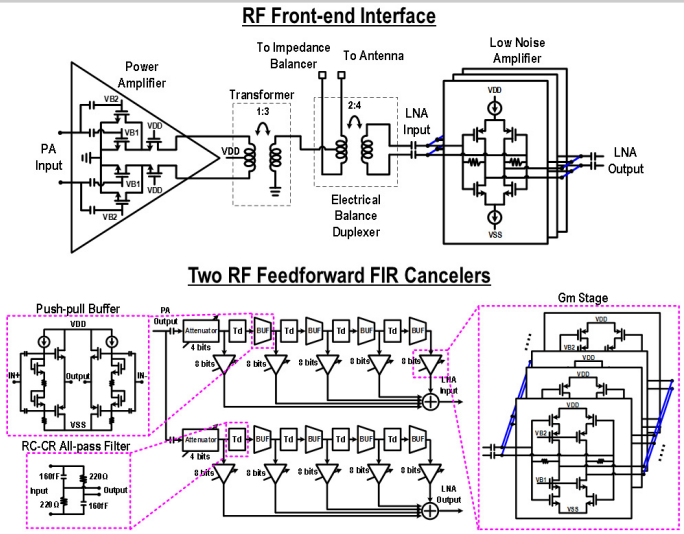

Figure 9.7.3: Detailed circuit diagram of: 1) RF front-end interface, 2) RF cancelers.

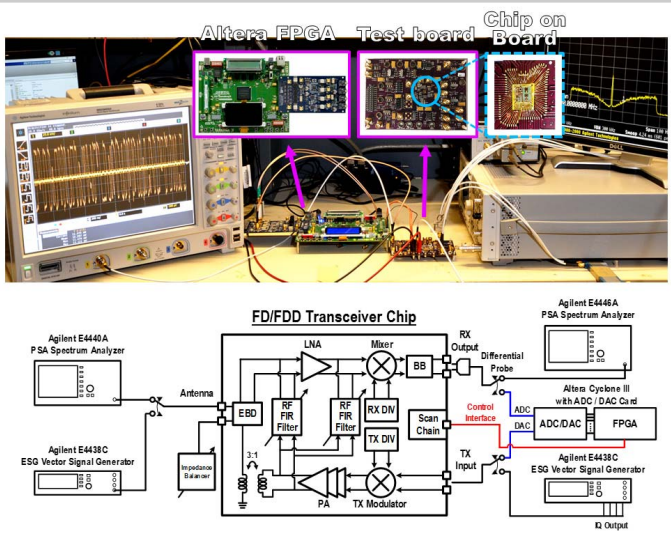

Figure 9.7.4: Lab bench setup allowing various modes of testing. Chip testboard and Altera Cyclone III FPGA board shown above.

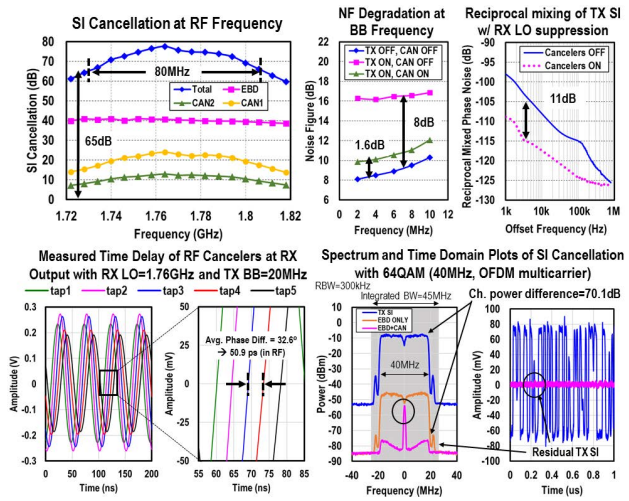

Figure 9.7.5: Measurement results of TX SI mitigation: SI cancellation with CW signal, NF and reciprocal mixing, tap delay of cancelers, and SI cancellation with OFDM signal.

		RFIC' 2017 [1]	ISSCC' 2017 [2]	ISSCC' 2017 [3]	TMTT' 2017 [4]	This Work
Architecture		Replica Cancellation DAC	N-Path-Filter-Based Circulator	Dual-Path + Adaptive Filter	EBD + SAW Filter	EBD + Double-RF Adaptive Filter
Technology		65nm	65nm	40nm	0.18μm SOI	40nm
Frequency Range (GHz)		1-2	0.61-0.975	1.7-2.2	0.7-1.0	1.6-1.9
TX SI	TX_{out}-to-RX_{in} Iso. (dB)	N/A External Circulator	40[e] On-Chip Circulator	N/A External Circulator	50 On-Chip EBD	39[e] On-Chip EBD
	Total On-Chip SIC Depth (dB) / BW (MHz)	64 / 20	40 / 20	50 / 42	50 / 10 (SAW) 50 / 2 (EBD)	72.8 / 20[b] 70.1 / 40[c] 65.2 / 80[d]
RX Gain (dB)		35	28	36	8.8	42
Noise Figure (dB)		3.6	6.3	4	7.6	8.1 (5.6dB from EBD)
SIC NF Degradation (dB)		3.4[g]	1.7	1.5	N/A	1.6
Canceler Area (mm^2)		N/A	N/A	0.349 (RF+BB)	N/A	0.12 (RF*2)
SI Circuitry Power (mW)		N/A	N/A	36[f] 11.5 (RF+BB)	0 (passive)	14.3 (RF*2)
TX SI to RX LO Suppression (dB)		N/A	N/A	10	N/A	11
Integrated TX Upconversion Path		No	No	No	No	Yes
Integrated PA		Yes	No	Yes	No	Yes
Integrated PLL		No	No	Yes	No	Yes
Active Area (mm^2)		6.25	0.94	3.5	6.62	4

[a] Measured with on-chip test structure. [b] Measured channel power difference with 20MHz 64QAM and 22MHz integration BW. [c] Measured channel power difference with 40MHz 64QAM and 45MHz integration BW. [d] Measured channel power difference with 80MHz 64QAM and 85MHz integration BW. [e] Averaged over 20MHz. [f] Antenna interface. [g] Calculated by the difference between system NF and RX NF

Figure 9.7.6: Comparison table with state-of-art FD publications.

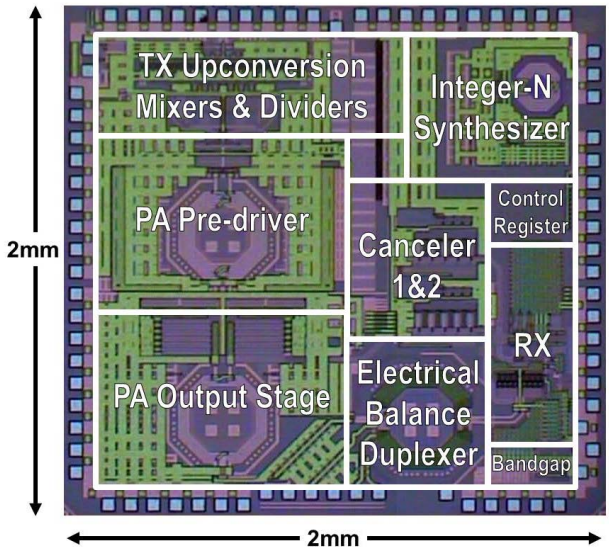

Figure 9.7.7: TSMC 6L-metal FD and FDD transceiver die micrograph.

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