18.1 A 1.7-to-2.2GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth

Tong Zhang, Ali Najafi, Chenxin Su, Jacques C. Rudell

University of Washington, Seattle, WA

Full-duplex (FD) radio communication potentially doubles the spectral efficiency in the densely occupied RF spectrum (100MHz to 5GHz). However, significant challenges remain, particularly the presence of a strong transmitter (TX) self-interference (SI) coupling to the receiver (RX). Numerous recent efforts on mitigating SI have focused on using active cancellation techniques [1-5]. However, these methods are challenged by either a degradation in noise performance [2], high power consumption [1,4], large silicon area [5], the inability to adequately cancel a high-output-power TX signal [3-4], or achieve a relatively narrow cancellation bandwidth [3,5]. Moreover, other sources of SI are presented to the RX, including the effects of 1) in-band TX thermal noise, which can exceed the RX noise floor, 2) the RX LO phase noise (PN), which reciprocally mixes with SI, further degrading the C/I ratio. This paper presents several circuit-level techniques, which contribute toward reducing the interaction between the TX and RX in FD radios.

Prior cancellation methods inject a SI cancellation signal at the RX input to relax the demand on linearity for the subsequent RX signal path (Fig. 18.1.1) [1,2,5]. This approach uses two wideband cancellation paths, one at RF (SIC1, Fig. 18.1.1), while the second one is in the RX BB (SIC2 and T_{D1}, Fig. 18.1.1). The PA output-matching network provides the input to both cancellers.

This FD system (Fig. 18.1.2) includes an integrated Class-AB PA, integer-N synthesizer running at twice the local-oscillator (LO) frequency, two LO dividers, and two SI cancellers. Detailed circuit diagrams for both the RF and BB cancellers are shown in Fig. 18.1.3. State-of-the-art cancellers [1,2,5] use calibration to tune the phase/amplitude of the cancellation path to match the TX leakage at the center frequency. This often leads to a narrowband cancellation [3,5], as the leakage path has a frequency response that rapidly deviates from the canceller response for small frequency offsets from the carrier. The proposed method to broaden the cancellation BW is best understood by analyzing the leakage signal in the time domain using an inverse Fourier transform, which reveals that there are two main leakage paths, both having strong time variance, originating from: 1) finite isolation through a circulator or two antennas, 2) signal reflection from the antenna. This FD system utilizes adaptive filters to create an inverse time-domain response of the leakage path to track a time-varying response. The proposed analog RF canceller is implemented as an analog FIR filter, where each tap includes a true-time-delay (TTD) circuit, a buffer, and a 7b variable-gain amplifier (MSB determines the polarity, while the other 6 bits control the canceller gain). The TTD block is designed as an RC-CR all-pass filter with the resistor/capacitor values of 500Ω/160fF, respectively. Each of the RF TTD blocks provides a simulated time delay of 65ps. The variable-gain amplifier is designed with a set of low-power, low-noise inverter-based Gm stages. The current output of each tap is summed and fed to the RX input. More filter taps increase the cancellation BW, but degrade the RX NF and raise the power consumption; 5-taps was found optimal to achieve a desired 40MHz cancellation BW with less than 1dB RX NF degradation.

The BB canceller design uses a 14-tap adaptive filter. Each of the BB TTD blocks is similar to [6] and has a simulated 10ns time delay. The mixers used in the RX signal chain and BB canceller paths (path 3) utilize the same LO signal (LO_1), but have a delay mismatch between them (see Fig. 18.1.1). Thus, a variable delay (T_{D1}) in the LO output that supplies the path-3 mixer, compensates for the path 1-to-3 delay mismatch. Combining the BB canceller and T_{D1} allows the suppression of both the TX SI and RX LO sidebands (see Fig. 18.1.1 and Fig. 18.1.2).

An integrated three-stage Class-AB noise-cancelling (NC) power amplifier (Fig. 18.1.2) reduces the simulated/measured PA in-band thermal-noise floor by 5dB (Fig. 18.1.4). The PA provides low noise and high gain in the first stage of amplification using a topology similar to a NC-LNA [7].

The PA has a maximum output power of +25dBm, which places a high input-referred linearity demand on the RF canceller since it is attached directly to the PA output. Thus, to improve the canceller linearity, two features are exploited: 1) additional attenuation capacitors C_1 and C_2 (Fig. 18.1.3) are added at the input of RF/BB cancellers to give 6dB and 10dB attenuation, respectively, 2) the input of both cancellers are attached to the differential low-impedance side (~9Ω) of the PA output-matching network (XFMR) to lower the maximum voltage swing (2.5V) at the canceller input (Fig. 18.1.2). The RF/BB canceller has a measured P_{-1dB} and IIP3 of 27/26.5dBm and 36/34.5dBm, respectively. C_1 and C_2 also raise the input impedance of the canceller (simulated to be 3kΩ), thus minimizing any PA-output-loading effects.

As a demonstration of this FD system, a transceiver front-end was realized in a 40nm, 6-metal-layer TSMC CMOS process with a die size of 3.5mm^2. The RF canceller occupies an area of 203μm×124μm. The measurement setup (Fig. 18.1.5) consists of an Altera Cyclone III EP3C120 Development Board that emulates a digital BB that would otherwise implement a blind-source-adaptation algorithm for both cancelling filters. The algorithm starts by adapting the 5-tap RF canceller. After the RF canceller converges, the adaption algorithm is then applied to the BB canceller. The RX operates from 1.7 to 2.2GHz with a measured gain of 36dB and a 4dB in-band NF while consuming 22mW. The NC-PA has a measured output P_{-1dB}/P_{sat} of 25.1/26.5dBm and a maximum PAE of 32%. Using a 20Mb/s QPSK modulated input signal with +25dBm PA output power, a 5.1% EVM was measured. The measured integer-N synthesizer locking range is 3.4 to 4.4GHz while consuming 10.4mW with a PN of -116dBc/Hz @1MHz offset.

All self-interference-cancellation measurements were performed using an off-chip circulator while the PA delivered +25dBm. The maximum on-chip measured SI cancellation is 55dB with greater than 50dB cancellation over a 42MHz bandwidth (Fig. 18.1.4). The combined FD front-end chip with a discrete circulator may achieve more than 80dB of SI cancellation/isolation. The RX NF measurements were performed using a desired RX signal, which is 100kHz away from the TX leakage signal, and monitoring the C/I ratio at the RX output. Before the canceller is enabled, the NF degradation is 6dB, and it drops to 1.55dB after enabling the cancellers (Fig. 18.1.4). Next, measurements were performed to see the effectiveness of the RX-LO sideband suppression on the SI signal with the BB canceller and T_d enabled/disabled; 10dB RX-LO sideband cancellation was observed (Fig. 18.1.4).

A performance comparison is given in Fig. 18.1.6, while the die micrograph is shown in Fig. 18.1.7. Measurement results demonstrate promise toward enabling highly integrated same-channel FD transceivers.

Acknowledgements:
This work was supported by NSF #1408575, CDADIC, Qualcomm, Google and Marvell. The authors acknowledged Li Lin and Visvesh Sathe.

References:

[1] J. Zhou, et al., "Reconfigurable Receiver with >20MHz Bandwidth Self-Interference Cancellation Suitable for FDD, Co-Existence and Full-Duplex Applications," *ISSCC*, pp. 342-343, Feb. 2015.
[2] D.-J. van den Broek, et al., "A Self-Interference-Cancelling Receiver for In-Band Full-Duplex Wireless with Low Distortion under Cancellation of Strong TX Leakage," *ISSCC*, pp. 344-345, Feb. 2015.
[3] D. Yang, et al., "A Wideband Highly Integrated and Widely Tunable Transceiver for In-Band Full-Duplex Communication," *IEEE JSSC*, vol. 50, no. 5, pp. 1189-1202, May 2015.
[4] J. Zhou, et al., "Receiver with Integrated Magnetic-Free N-Path-Filter-Based Non-Reciprocal Circulator and Baseband self-interference cancellation for Full-Duplex Wireless", *ISSCC*, pp. 178-179, Feb. 2016.
[5] T. Zhang, et al., " An Integrated CMOS Passive Self-Interference Mitigation Technique for FDD Radios," *IEEE JSSC*, vol. 50, no. 5, pp. 1176-1188, May 2015.
[6] S. K. Garakoui, et al., "Compact Cascadable gm-C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency," *IEEE JSSC*, vol. 50, no. 3, pp. 693-703, March 2015.
[7] F. Bruccoleri, et al., "Noise canceling in wideband CMOS LNAs," *ISSCC*, pp. 406–407, Feb. 2002.

 978-1-5090-3758-2/17/$31.00

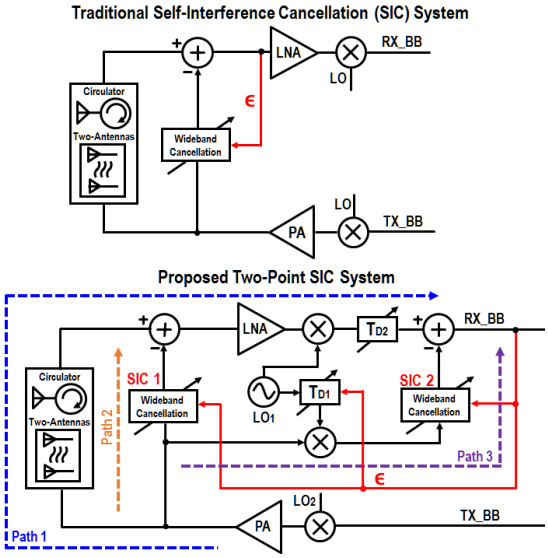

Figure 18.1.1: Conceptual diagram of the proposed full-duplex front-end.

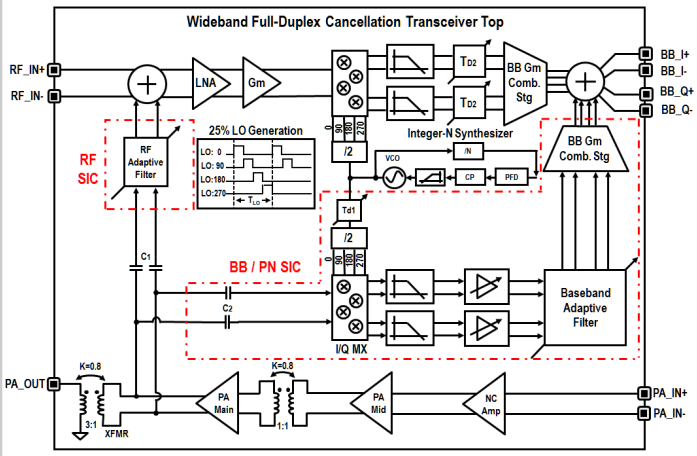

Figure 18.1.2: Detailed transceiver block diagram for the implemented full-duplex front-end.

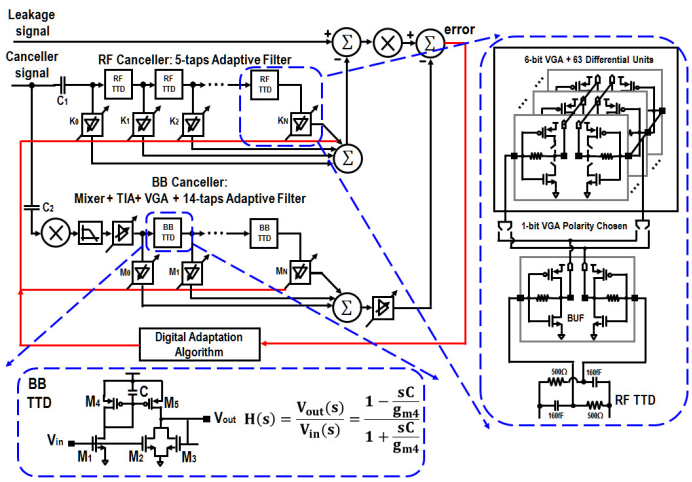

Figure 18.1.3: Detailed circuit diagram of RF/BB adaptive filter for self-interference cancellation.

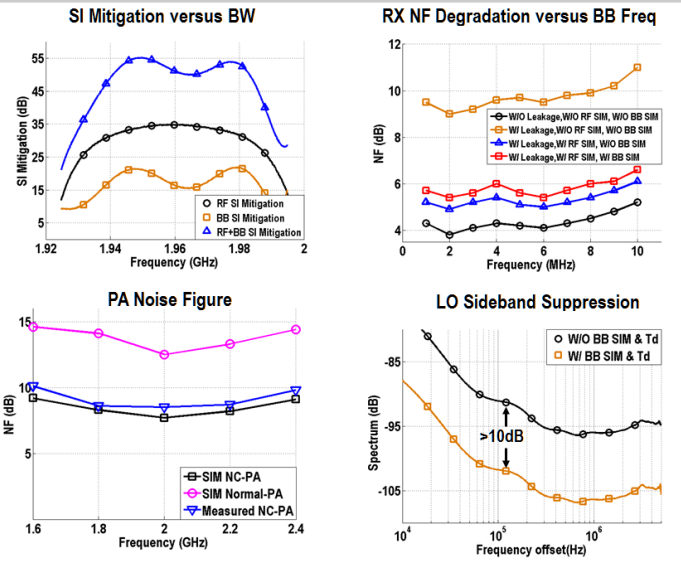

Figure 18.1.4: Measured self-interference mitigation results.

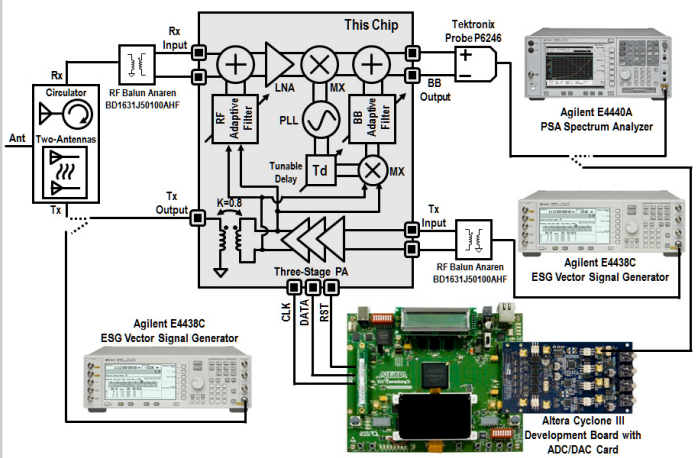

Figure 18.1.5: Chip testing measurement setup.

		ISSCC 2015 [1]	ISSCC 2015 [2]	JSSC 2015 [3]	ISSCC 2016 [4]	This Work
Architecture		Frequency Domain Equalization	Mixer-First RX+ VM-downmixer	Mixer First+ Duplexing LNA	Integrated Circulator+ BB SIC	Adaptive Filter + NC PA+ LO Sideband Suppression
Technology/VDD		65nm /?	65nm/1.2V	65nm/1.2V, 2.5V	65nm/1.3V, 2.2V	40nm /1.2, 1.8V, 2.5V
RX Frequency (GHz)		0.8-1.4	0.15-3.5	0.1-1.5	0.6-0.8	1.7-2.2
TX-to-RX Interface Isolation (dB)		30-50	N/A	N/A	N/A	30-35
Integrated Power Amplifier		No	Yes	Yes	No	Yes
Integrated PLL		No	No	No	No	Yes
TX Maximum Suppression (dB)		N/A	27	33	N/A	55[7]
Cancellation BW	Cancellation (dB)	20	27	33	42[4]	50[7]
	BW (MHz)	15 / 25[2]	16.25[2]	0.3	12[4]	42[7]
NF degradation due to leakage cancellation (dB)		0.9-1.2/1.1-1.5[8]	4-6	N/A[6]	5.9[8]	1.05 (RF)+0.5(BB)
Canceller Power Consumption (mW)		44-91[5]	N/A	N/A	30	3.5 (RF) +8 (BB)
RF Canceller Area (μm²)		N/A	N/A	N/A	N/A	203 × 124
Canceller IIP3 (dBm)		N/A	N/A	N/A	N/A	36 (RF) / 34.5 (BB)
Canceller P1dB (dBm)		N/A	N/A	N/A	N/A	27 (RF) / 26.5 (BB)
RX LO Sideband Suppression (dB)		N/A	N/A	N/A	N/A	10
RX Gain		27-42	24	33-53	42	20-36
RX Power Consumption (mW)		63-69	23-56[6]	43-56	70[6]	22
Maximum TX Output Power (dBm)		N/A	>10	N/A	N/A	25
TX PAE (%) @Maximum Power		N/A	N/A	N/A	N/A	32
TX EVM (%)		N/A	N/A	N/A	N/A	5.1
PLL Phase Noise @1MHz (dBc/Hz)		N/A	N/A	N/A	N/A	-116
Active Area (mm²)		4.8	2	1.5	1.4	3.5

[1]Measurement with an antenna pair. 15MHz BW, 0.9-1.2dB NF deg. is with one filter. 25MHz, 1.1-1.5dB NF deg. is with two filters. [2]Power including 0-47mW Gm cells and 44mW LO for one filter. [3]Half-duplex/Full-duplex mode show NF of 6.3/ 10.3-12.3dB. [4]Power including LO tree. [5]RX DSB NF is 5-8dB in Full-Duplex mode. [6]42dB cancellation 12MHz BW measured including integrated circulator, not including 43dB digital cancellation from Matlab. [7]The TDD RX NF is 5dB, NF increases to 8.4dB including the circulator and goes to 10.9dB including the baseband canceller. [8]Power including 60mW signal path and 10mW LO path at 0.7GHz. [9]The measured maximum 55dB cancellation and 50dB cancellation over 40MHz BW doesn't include the 30-35dB isolation from the discrete circulator or two-antennas.

Figure 18.1.6: Performance summary and comparison with other state-of-the-art FD publications.

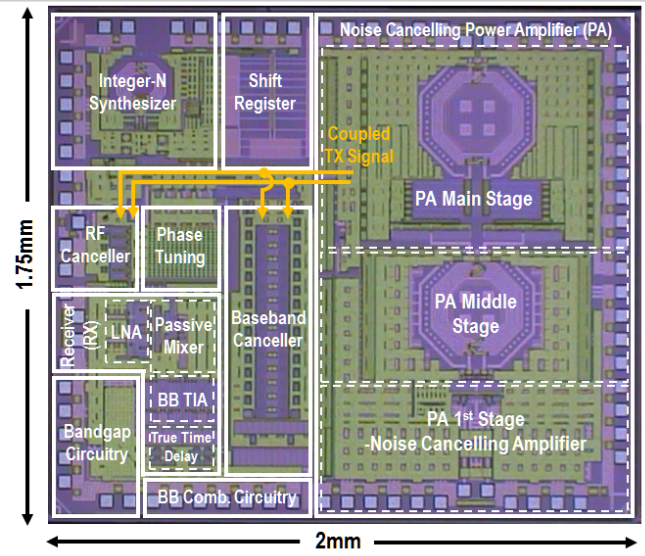

Figure 18.1.7: 40nm TSMC die micrograph.

978-1-5090-3758-2/17/$31.00 ©2017 IEEE