A High-Voltage Compliant, Electrode-Invariant Neural Stimulator Front-End in 65nm Bulk-CMOS

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***Abstract*— A high-voltage compliant, 65nm bulk-CMOS neural stimulator front-end is presented which can interface with a wide range of electrode impedances. With bulk-CMOS compatibility, the presented design can be easily integrated on the same silicon chip with other blocks needed for implantable bidirectional neural interfaces (e.g. high-density neural recording, DSP, memory, wireless interfaces). Measurements show voltage compliance exceeding +/-10V (with 1V and 2.5V devices) when driving 50µA to 2mA biphasic stimulus through resistive and capacitive electrode models. *In vivo* measurement results are provided (anesthetized rat) which demonstrate the efficacy of the integrated stimulator in bidirectional neural interface applications. The stimulator front-end active die area is 2mm^2. While delivering 2mA, 200µs pulse-width biphasic stimulus at 300Hz the chip consumes 9.33mW; stand-by power consumption is approximately 300µW.**

Keywords—Neural interfaces, electrical stimulation, high-voltage, bulk-CMOS

I. INTRODUCTION

Rapid advances in understanding brain function, neural connectivity and neural plasticity are providing opportunities to develop innovative systems to aid the diagnosis and treatment of neurological disorders. Specifically, electrical neural stimulators are being used alongside neural recording systems to enable bidirectional interactions with the nervous system and realize new neuroprostheses and rehabilitation methods. However, to make such bidirectional neural interfaces viable for future medical technologies, the implanted electronics must be robust, low power, and wireless (communication and power). Additionally, many bidirectional neural interface applications (e.g. cortico-spinal prostheses, automated seizure suppression [5], closed-loop deep-brain stimulation) require digital signal processing within the implant, as to control the stimulator in response to recorded neural activity, in real-time. System-on-Chip (SoC) integration in bulk-CMOS silicon holds promise toward realizing the aforementioned features.

A key barrier to implementing all bidirectional neural interface electronics on a single bulk-CMOS chip relates to the high voltages often required to evoke neural activity using electrical stimulation. These large voltages are the result of driving charge-balanced, biphasic stimulus current through the electrode-tissue-interface impedance (Z_E). Although advancing the state-of-the-art in energy efficiency [1, 2] and form-factor, most bulk-CMOS neural stimulators published to date have limited voltage compliance (i.e. ±VDD/2), constrained by the foundry-defined voltage-ratings of the implemented active devices (e.g. VDD = 1V) in order to prevent gate-oxide breakdown and ensure reliable performance. Yet, several bulk-CMOS stimulators have been developed with voltage compliance beyond ±VDD/2 [3, 4, 5]. However, these specialized front-end designs either still restrictively limit the overall stimulator compliance (i.e. < ±VDD), have performance limitations in terms of driving stimulus through electrodes with varied frequency-dependent impedance characteristics (discussed in [6]), and/or place the front-end design burden on high-performance/specialized analog circuits (e.g. floating current-DACs) which may be difficult to implement across advanced CMOS technologies.

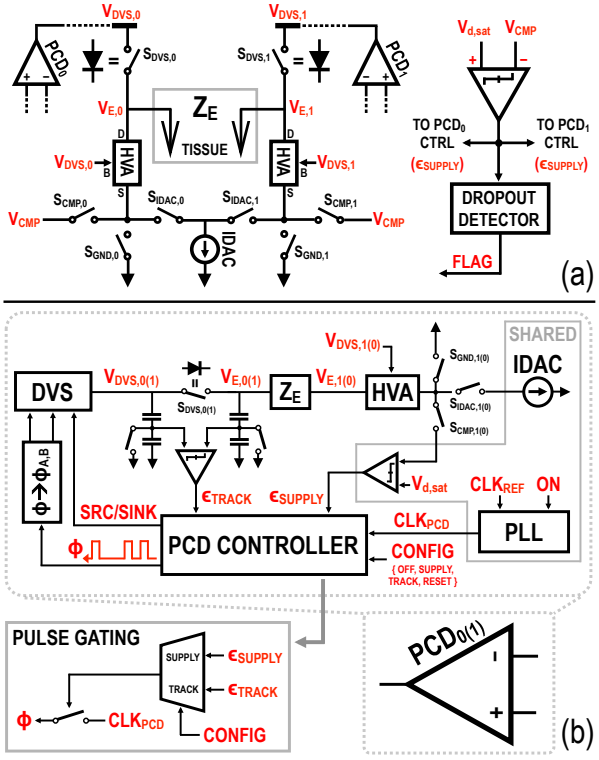

Fig. 1. Overview of proposed neural stimulator (a) H-bridge-based front-end interfaces with two electrodes (0 & 1); fictional op-amps model the behavior of two, multi-purpose positive-current drivers (PCDs); (b) $PCD_{0(1)}$ block-diagram; pulse-gating of high-frequency clock within PCD is used to regulate a switch-capacitor dynamic power supply (DVS).

Thus, this work seeks to realize a high-voltage, bulk-CMOS stimulator front-end with: 1) voltage compliance de-coupled from the VDD-rating of the implementing transistors; 2) the ability to drive charge-balanced, current-regulated stimulus through a wide range of Z_E, from resistive to capacitive (i.e. "electrode-invariant" performance); and 3) a

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design which is scalable across nm-scale CMOS technologies, leveraging the transistor as a switch as much as possible.

II. System Overview

The proposed high-voltage stimulator front-end is based on a sink-regulated H-bridge (Fig. 1a), which is digitally cycled through different states to deliver biphasic, constant-current stimulus (Fig. 2a). Both phases of the stimulus current are regulated by a single, low-voltage current-DAC (IDAC), which can safely interface with the stimulation electrodes using specialized high-voltage adapter (HVA) circuits. Two dynamic voltage supplies (DVSs) are controlled within separate positive-current driver (PCD) sub-systems (Fig. 1b) to perform two functions: 1) to SUPPLY stimulus current while dynamically generating a 0-to-V_{MAX} voltage that keeps the IDAC from dropping-out (i.e. keeps IDAC devices in saturation) and 2) to subsequently TRACK a discharging electrode voltage back down to low voltages, as to keep the attached HVA properly biased and the switch to the electrode (a diode) off (Fig. 2c). To account for "capacitive-looking" electrodes, the front-end uses the balancing stimulus to discharge Z_E, which may hold a high voltage after the leading stimulus pulse is delivered (State 4 in Fig. 2); only after a low-voltage comparator (CMP) detects Z_E to be discharged is a DVS used to deliver the remaining balancing stimulus current.

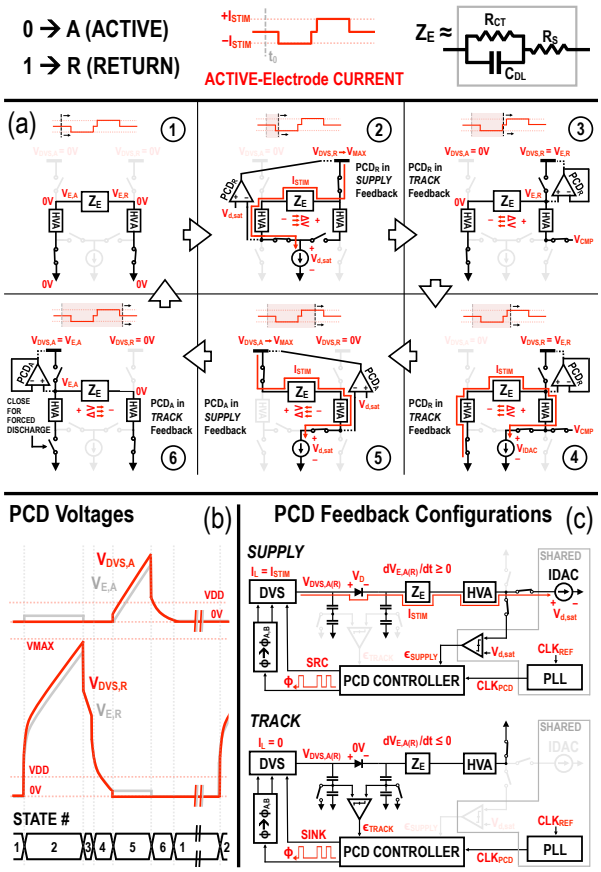
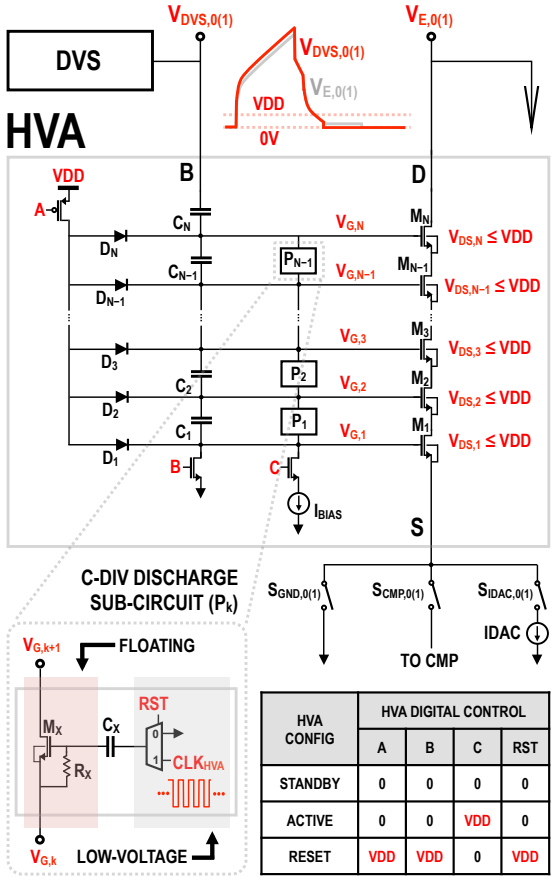


Fig. 2. Transient operation of stimulator front-end: (a) front-end "state-cycle" producing biphasic stimulus delivery; (b) illustrated electrode and DVS voltages during stimulus delivery; (c) PCD in SUPPLY feedback used to actively supply stimulus current and PCD in TRACK feedback used to safely discharge DVS voltage as the electrode voltage falls.



HVA CONFIG	HVA DIGITAL CONTROL			
	A	B	C	RST
STANDBY	0	0	0	0
ACTIVE	0	0	VDD	0
RESET	VDD	VDD	0	VDD

Fig. 3. High-voltage adapter (HVA) circuit schematic and control summary; when ACTIVE, a C-DIV safely distributes DVS voltage (which closely tracks electrode voltage seen by HVA) across gates of M_1 through M_N.

III. Dynamic Voltage Supply (DVS) Circuit

Each DVS is a multi-stage, switched-capacitor power converter, terminated by a large capacitor (C_{OUT}). A single-stage of a DVS is a modified voltage-doubler, employing two "pumping capacitors" (C_{PUMP}) to either source (SRC) or SINK switched-capacitor current (with equal drive strength) to and from the output, respectively (for $V_{OUT} \geq V_{IN}$) [6]. In a PCD (Section II), 1-bit error generated by a low-voltage CMP is used to gate a high-frequency clock (CLK_{PCD}) into the DVS switching signal input (Φ), with the resulting unidirectional feedback (i.e. on/off regulation) ensuring loop stability. The maximum N-stage DVS output voltage (V_{MAX}) is limited by the reverse-breakdown voltage of the n-well/substrate junction ($\approx$ 12V for the CMOS process used in this work) [6]; this barrier ultimately limits the compliance of the proposed stimulator, instead of individual device voltage limits. A more detailed discussion of the DVS circuit can be found in [6].

IV. High-Voltage Adapter (HVA) Circuit

A high-voltage adapter (HVA) circuit (Fig. 3) employs a cascode of equally-sized deep-n-well NMOS devices to provide a safe conduction pathway between an electrode (which may be at high voltages) and low-voltage circuits (e.g. CMP, IDAC). The HVA uses a capacitive divider (C-DIV) to implement a device-protecting gate-biasing function, which

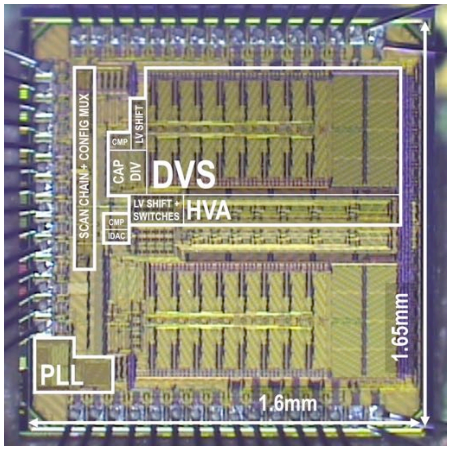


Fig. 4. Annotated photo of the 9-metal TSMC 65nm CMOS (GP) chip.

ensures that when large electrode voltages are generated, each transistor in the HVA cascode never experiences terminal-to-terminal voltage exceeding the device VDD-rating. Overall, this approach is similar to C-DIV biasing schemes utilized in stack power-amplifiers for RF and mm-Wave transmitters.

When a HVA is ACTIVE (i.e. stimulus is being delivered), the bottom of the C-DIV is kept at V_{ON} = VDD – V_{D1} via I_{BIAS}, limiting the voltage at the effective "source" of the HVA to $V_{ON} - V_{GS,1} <$ VDD. Meanwhile, the top of the C-DIV is biased by the DVS on the same side of the H-bridge as the HVA; accordingly, when large electrode voltage variations occur, the electrode and biasing DVS voltages will be approximately equal via PCD feedback operation (Section II).

The C-DIV distributes the DVS output voltage among the gates of a HVA cascode according to Eq. 1; this gate-biasing function protects the HVA devices from voltage overstress, as long as Eq. 2 and Eq. 3 are satisfied (where VDD is the device voltage-rating, N is the number of HVA "stages", and k is the device index). If Eq. 2 is satisfied then $V_{G,k+1} - V_{G,k} \leq$ VDD, and if the lower bound of Eq. 3 is satisfied, then as the DVS and electrode voltages rise and fall during stimulus delivery, $V_{GS,k+1} \geq V_{GS,k}$; these two conditions together ensure V_{DS} reliability (i.e. $V_{DS,k} \leq$ VDD). V_{GS} reliability (i.e. $V_{GS,k} \leq$ VDD) is maintained by the upper bound of Eq. 3 (along with setting V_{ON}, which limits the maximum drain current of the HVA cascode, sufficiently low). To implement Eq. 1, C_1 through C_{N-1} are sized for equal division, and C_N is sized so that Eq. 3 is satisfied considering worst-case error between DVS and electrode voltage during stimulus delivery.

$$V_{G,k} = V_{ON} + \alpha\left(\frac{k-1}{N-1}\right)V_E \tag{1}$$

$$V_E \leq (N-1)VDD/\alpha \tag{2}$$

$$\frac{N-1}{N} \leq \alpha < \frac{(N-1)VDD}{V_{ON}+(N-2)VDD} \tag{3}$$

The low-duty cycle of neural stimulation (typically << 50%) is leveraged to RESET the HVA between stimulus events, during which the DVS and electrode voltages are known to be 0V (i.e. State 1 in Fig. 2). To quickly RESET the HVA, VDD and I_{BIAS} are disconnected, the bottom-plate of C_1 is grounded, and pulses are AC-coupled to the gates of the M_X devices (Fig. 3) to discharge C_1 through C_{N-1}. A HVA can be placed in STANDBY by disconnecting I_{BIAS}; this configuration is useful in keeping an electrode connected to ground during the long intervals between stimulus events (while the HVA consumes no power).

V. Implementation & Measurements

The stimulator front-end was fabricated in the 9-metal, TSMC 65nm GP CMOS process. ±11V to ±10V compliance was measured when delivering biphasic stimulus current ranging from 50µA to 2mA in amplitude, respectively.

A. Chip Implemeantion and Overview

An annotated chip die photo is shown in Fig. 4; the active chip area is ≈ 2mm^2. The DVS design uses 8-stages and a 2.5V VDD, with C_{PUMP} and C_{OUT} set to 13.1pF and 180pF, respectively. The maximum frequency of CLK_{PCD} is 8×13.56MHz but lower multiples of 13.56MHz (i.e. x4, x2, and x1) can be used based on the stimulus amplitude setting. The HVA employs 7-stages, with C_1 through C_7 set to ensure the terminal-to-terminal voltages of each cascoded device stay within ±2.5V during high-voltage stimulation. The chip uses 3

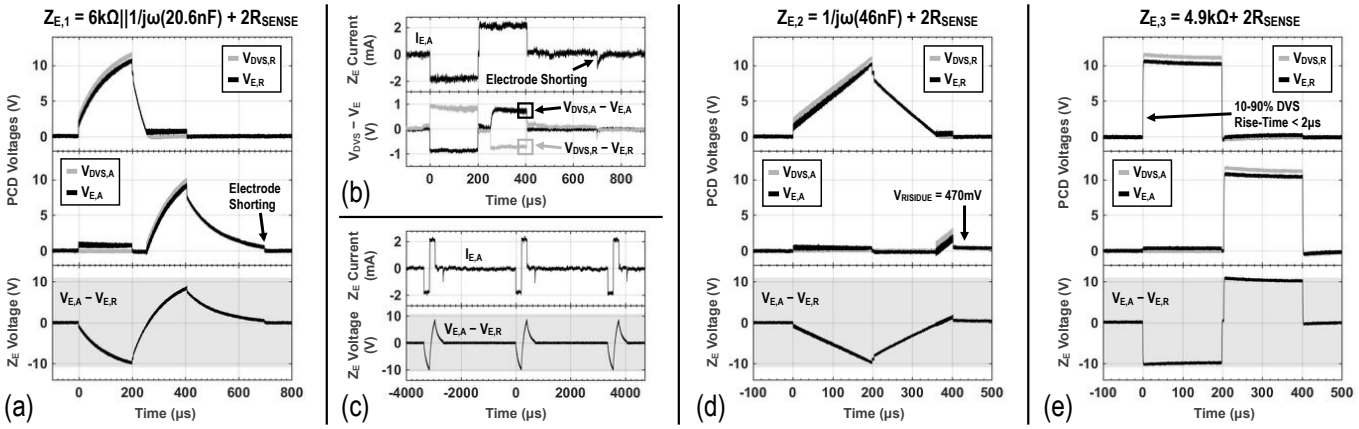


Fig. 5. Measured front-end signals during high-voltage, 2mA, 200µs pulse-width biphasic stimulus delivery to RC-modeled Z_E (R_{SENSE} = 200Ω current sense resistor); (a) DVS and electrode voltages for parallel-RC $Z_{E,1}$; (b) active electrode current and DVS-electrode difference voltage during $Z_{E,1}$ stimulation; (c) 300Hz stimulus pulse delivery to $Z_{E,1}$ (d) DVS and electrode voltages for capacitive $Z_{E,2}$; (e) DVS and electrode voltages for resistive $Z_{E,3}$.

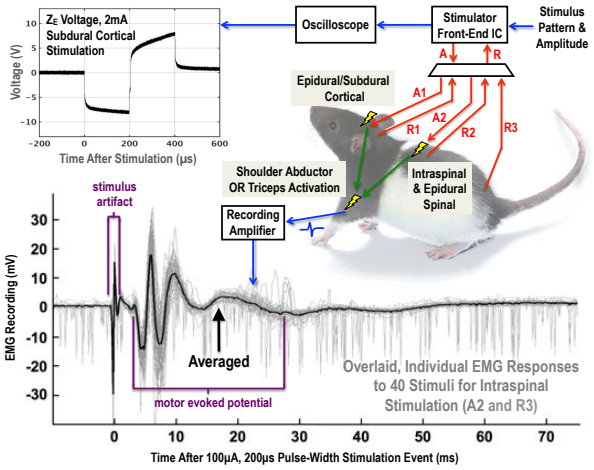


Fig. 6. Fabricated stimulator chip producing motor evoked potentials in an anesthetized rat. Electrodes: A1 is silver ball electrode at forelimb area of motor cortex, R1 is skull-screw return, A2 and R2 are 50µm Pt/Ir wires at cervical spinal cord, R3 is stainless steel dorsal return.

clocked-comparators (CMPs), each having the same design and a maximum sampling rate of 8×13.56MHz. Each PCD has a dedicated CMP for TRACK-feedback error detection, and the third CMP is used for IDAC dropout detection and shared by both PCDs for SUPPLY-feedback error detection. The low-voltage, binary-weighted IDAC has a 10µA LSB and features a 2.5V-tolerant active-cascode buffer. An on-chip phase-locked loop (PLL) takes a 13.56MHz input (ISM band) from off-chip and generates the high-frequency clocks used by the CMPs, DVSs, and HVAs. An off-chip micro-controller generates a 200kHz system clock and a 4-bit bus which encodes the "state" of the front-end; this bus is input to a large multiplexing structure, which then forwards the correct configuration codes (all scanned into the chip) to the front-end blocks, digitally guiding the chip through each state of stimulus delivery.

B. Benchtop Stimulator Front-End Measurements

Fig. 5 provides the measured PCD voltages and Z_E current during high-voltage, 2mA stimulation with varied Z_E. The residual voltage measured after 2mA stimulus is delivered to the capacitive $Z_{E,2}$ (for which the front-end functions the most asymmetrically) corresponds to 22nC of charge-mismatch (Fig. 5d). When stimulating the purely resistive $Z_{E,3}$ (Fig. 5e) at a high rate (300Hz) the chip consumes 9.33mW (nearly all drawn from the 2.5V supply); as Z_E becomes more capacitive, this power draw reduces since a larger fraction of the balancing stimulus is not actively supplied by a DVS. The stand-by power consumption of the chip is measured at 304µW (leakage, system clocking, comparator biasing, op-amp biasing in IDAC, and charge-pump/VCO biasing in PLL); the only stand-by power consumption from the high-voltage front-end circuits (DVSs and HVAs) is a single, 2µA HVA bias current.

C. In Vivo Measurements

The *in vivo* efficacy of the chip was demonstrated by producing motor evoked potentials and overt movement in the triceps and shoulder abductor of an anesthetized rat (Fig. 6) through spinal stimulation (intraspinal, epidural) and cortical stimulation (epidural, subdural); four applications relevant to bidirectional neural interface research and development.

VI. Conclusion

A comparison to other high-voltage bulk-CMOS stimulators is provided in Table I. With the designs of the DVS and HVA de-coupling compliance from transistor VDD-ratings, this work achieves state-of-the-art voltage compliance. The larger area compared to [4] and [5] is due to the area-dominant DVSs used to drive higher stimulus currents and voltages. And although presented in a specific 65nm CMOS process, this stimulator is easily scalable to other process nodes since it allows for the insertion of almost any IDAC, PLL, and CMP design, and it requires only two specialized circuits, with HVA operation relying on a capacitive divider and DVS operation leveraging transistors as switches. Overall, this work demonstrates the possibility of bidirectional neural interface SoC integration in low-voltage, bulk-CMOS technologies.

TABLE I. PERFORMANCE COMPARISON

System	[3]	[4]	[5]	**This Work**
Stimulus Regulation	Biphasic Arbitrary Current	Biphasic Constant Current	Biphasic Constant Current	Biphasic Constant Current
Topology	Ground-Return	Differential	H-Bridge	H-Bridge
Process	65nm CMOS	65nm CMOS	0.18µm CMOS	65nm CMOS
Device Rating / Compliance	1.2V, 2.5V / ±2.4V	1.2V, 2.5V / ±6V	1.8V, 3.3V / ±9V	1V, 2.5V / > ±10V*
Electrode Invariant	R → YES C → YES	R → ?** C → YES	R → YES C → NO**	R → YES C → YES
Charge-Balancing Technique	Digital Cal.	Electrode Short w/ Off-Chip Series Caps	N.A.	Electrode Short w/ Off-Chip Series Caps
Max Amp	50µA	450µA***	30µA	2mA
Electrodes / Stimulators	513 / 512	16 / 2	2 / 1	2 / 1
Stimulator Active Area	0.0169mm^2 /stimulator	0.385mm^2 + 0.0675mm^2 /stimulator	≈ 0.6mm^2	2mm^2

*±10V at 2mA stimulus, ±11V at 50µA stimulus
**Not Demonstrated
***Demonstrated up to 150µA

Acknowledgment

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