

An Ultra-Wideband IF Millimeter-Wave Receiver With a 20 GHz Channel Bandwidth Using Gain-Equalized Transformers

Venumadhav Bhagavatula, *Member, IEEE*, Tong Zhang, *Student Member, IEEE*, Apsara Ravish Suvarna, and Jacques Christophe Rudell, *Senior Member, IEEE*

Abstract—This paper presents a CMOS millimeter-wave (mm-wave) receiver designed to meet the challenges in low-power, ultra-broadband, phased-array systems with a large number of array elements. This receiver employs a high intermediate-frequency (IF) heterodyne architecture to reduce the frequency and power consumption associated with distributing a local oscillator (LO). The receiver operates over a bandwidth of 51–71 GHz, while maintaining 20 GHz of bandwidth along the signal chain of the entire mm-wave front end, through a high-IF stage, and to the baseband output. To maintain a high fractional bandwidth (fBW) throughout the signal chain, this receiver employs multiple *gain-equalized transformers*. Receiver measurements show an overall flat bandwidth response of 20 GHz, with a total gain of 20 dB, a minimum double-sideband noise figure of 7.8 dB, and an input 1 dB compression power of -24 dBm while consuming 115 mW from a 1.1 V supply. The test chip, implemented in a six-metal layer 40 nm CMOS process, occupies an area (including pads) of 1.2 mm^2 .

Index Terms—Millimeter-wave integrated circuits, phased-arrays, receivers, RLC circuits, wideband.

I. INTRODUCTION

APPLICATIONS for single-chip CMOS electronics in the millimeter-wave (mm-wave) and terahertz spectrum promise to provide antenna, circuit, device, and system engineers with exciting opportunities for innovation. A couple of decades ago, the *radio frequency* (RF) band between 500 MHz and 10 GHz was considered “high” frequency for CMOS-based integrated circuits. However, advances in device fabrication and continued scaling of the minimum feature size have extended the maximum operating frequency of a single CMOS transistor in excess of several hundred gigahertz. Much of the initial commercial impetus for mm-wave CMOS was provided by the “60 GHz” standards (e.g., IEEE 802.11ad), which promised

Manuscript received May 15, 2015; revised August 14, 2015 and November 08, 2015; accepted November 13, 2015. Date of publication January 14, 2016; date of current version January 29, 2016. This paper was approved by Associate Editor Jan Craninckx. This work was supported by Grants from CDADIC and Qualcomm.

V. Bhagavatula is with Samsung Semiconductors Inc., San Jose, CA 95134 USA.

T. Zhang, A. R. Suvarna, and J. C. Rudell are with the Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA (e-mail: bvnu@uw.edu; togzhang@uw.edu; apsara@uw.edu; jcrudell@uw.edu).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2015.2504411

short-range high-speed communication with data rates exceeding 6–7 Gb/s. Starting with prototypes of mm-wave CMOS low-noise amplifiers (LNAs) and mixers [1]–[3], researchers have now demonstrated fully integrated mm-wave frequency synthesizers [4] and transceivers [5]–[8]. However, numerous challenges such as high-power consumption, large silicon area and bandwidth limitations, impede mass consumer deployment of mm-wave CMOS transceivers.

Extending the bandwidth of mm-wave transceivers, the primary focus of this paper, has gained recent interest in several publications [9], [10]. To achieve wideband signal amplification, this paper explores a technique to intentionally introduce electric coupling between magnetically coupled resonant tanks (transformers), succinctly referred to as *gain-equalized transformers*. In the discussion on bandwidth of a circuit, this paper will use the definition of fractional bandwidth (fBW) to mean the channel bandwidth/carrier frequency $\times 100$.

The prototype receiver described in this work targets the mm-wave frequency range of 50–70 GHz, as shown in Fig. 1. It is important to note that although the input frequency band has an overlap with the 60 GHz standard, the choice of this band was based on more practical considerations relating to the available measurement equipment in the lab, i.e., this receiver was not designed to meet the 60 GHz standard specifications. 60 GHz transceivers use narrow-band circuit techniques due to fBW requirements of less than 15%. In contrast, the ultra-wideband receiver described in this paper has a baseband bandwidth of 9 GHz (LSB) and 11 GHz (USB), approximately nine times larger than state-of-the-art 60 GHz systems.

To counter the high propagation-loss at mm-wave frequencies, multi-element phased-array transceivers have been proposed in prior-art [9]. Moreover, trends on the application level demand long-distance point-to-point mm-wave solutions with more directionality, necessitating a phased-array with large number of array elements. In such a scenario, the high power consumption in the on-chip local-oscillator (LO) distribution network motivates research to reduce this component of power consumption. In the lower frequency RF band direct conversion has evolved as the architecture of choice for highly integrated low-power systems, where the LO drives only a *single* set of quadrature mixers. In mm-wave band transceivers, such as an N -element direct conversion phased-array transceiver, the LO distribution power associated with driving N quadrature mixers could be equivalent, if not more than the signal path power. In contrast, a heterodyne architecture allows the

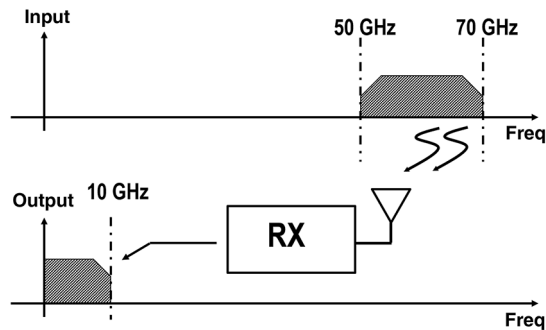


Fig. 1. Millimeter-wave spectrum targeted for this receiver.

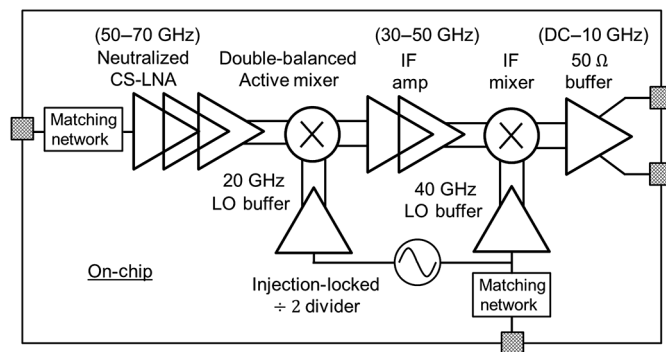


Fig. 2. Block diagram of the ultra-wideband mm-wave receiver.

flexibility of significantly reducing the frequency of the LO distributed throughout an N -element array, which reduces the power consumption associated with LO distribution. However, this reintroduces the need for a wideband and low-power intermediate-frequency (IF) stage which utilizes minimum silicon area.

This paper is organized as follows. Section II describes the receiver architecture along with the main bandwidth bottlenecks in the signal path. The design of a gain-equalized transformer is described in Section III. Circuit implementation details associated with this heterodyne receiver are discussed in Section IV. Experimental results from a prototype test-chip and comparison with other prior-art high fBW receivers are presented in Sections V and VI, respectively. Finally, this paper concludes with some summary comments in Section VII.

II. RECEIVER ARCHITECTURE

The block diagram of the receiver is shown in Fig. 2. The signal-path implemented on-chip includes a single-ended mm-wave input, an on-chip transformer-based matching network, a three-stage differential LNA, a double-balanced mm-wave active-mixer, a two-stage IF-amplifier, and an IF-mixer. The LO-path implemented on-chip includes an injection-locked divide-by-2 circuit and LO buffers.

The first mixer is driven by a 20 GHz LO, while the second mixer utilizes a 40 GHz LO. When the receiver is extended to phased-array systems, the single-phase differential 20 GHz LO will be distributed across the chip, while the quadrature 40 GHz LO feeds only a single set of I/Q mixers. While a heterodyne receiver has the advantage of scaling down the LO frequency for the first set of mm-wave mixers, a new challenge

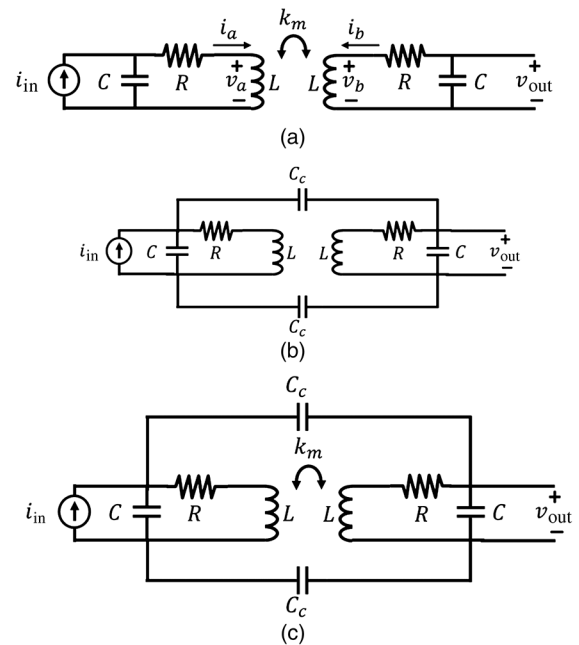


Fig. 3. (a) Magnetically coupled resonant tanks. (b) Electrically coupled resonant tanks. (c) Electrically and magnetically coupled resonant tanks.

is introduced at the IF stage for ultra-wideband systems. With an input signal bandwidth of 20 GHz, the front-end requires an fBW of at least 33%. However, when this 20 GHz signal is frequency-translated to an IF centered at 40 GHz, the IF amplifiers would require a fBW of 50%. This challenge provides an interesting opportunity for innovation to realize a very broadband multiresonant response.

A parallel R-L-C circuit is a common resonant-load employed in traditional narrow-band amplifier design. However, to extend a similar structure for wideband circuit design is challenging as the only variable available to the designer is to reduce the quality factor (Q) of the resonant-tank. Distributed amplification is another popular approach for wideband design. Fractional bandwidths exceeding 75% have been achieved using a distributed-amplifier (DA)-based band-pass amplifiers [14]; however, the band-pass filters require an input/output termination impedance of 50Ω to allow a practical, small area solution. Thus, DAs are suboptimal for use as an IF-stage in a heterodyne receiver. For the wideband mm-wave receiver described in this paper, multiple stages both at the front-end and IF must be presented with a wide bandwidth load. Higher order load networks using coupled resonant-tanks can provide a wideband frequency response; the details of using a combination of magnetic and electric coupling to realize a “gain-equalized” transformer are described in the following section.

III. GAIN-EQUALIZED TRANSFORMERS

Three mechanisms for coupling tuned resonant tanks—magnetic, electric, and combination of magnetic and electric—are shown in Fig. 3. For each structure, the parameter of interest is the trans-resistance Z , where Z is the ratio of the output voltage (v_{out}) to the input current (i_{in}).

TABLE I
PARAMETER VALUES IN CANONICAL EXPRESSIONS FOR MAGNETIC,
ELECTRICAL, AND MAGNETIC + ELECTRICAL COUPLING

	Magnetic coupling	Electrical coupling	Magnetic + electrical coupling
ω_{n1}	$\frac{1}{\sqrt{L(1-k_m)C}}$	$\frac{1}{\sqrt{LC}}$	$\frac{1}{\sqrt{LC}} \frac{1}{\sqrt{1+k_m}}$
ω_{n2}	$\frac{1}{\sqrt{L(1+k_m)C}}$	$\frac{1}{\sqrt{L(C+C_c)}}$	$\frac{1}{\sqrt{LC}} \sqrt{\frac{1-k_c}{1-k_m}}$
Q_1	$\frac{1}{R} \sqrt{\frac{L(1-k_m)}{C}}$	$\frac{1}{R} \sqrt{\frac{L}{C}}$	$\frac{1}{R} \sqrt{\frac{L(1+k_m)}{C}}$
Q_2	$\frac{1}{R} \sqrt{\frac{L(1+k_m)}{C}}$	$\frac{1}{R} \sqrt{\frac{L}{C+C_c}}$	$\frac{1}{R} \sqrt{\frac{L(1-k_m)}{C+C_c}}$

A. Magnetically Coupled Resonant Tanks

The circuit diagram of two magnetically coupled resonant tanks is shown in Fig. 3(a). The finite Q of the inductor is modeled by a series resistance R . Using node-analysis, the trans-resistance can be shown as

$$|Z_{MC}(s)| = \frac{v_{out}}{i_{in}} = \frac{sk_m L}{\{1 + sCR + s^2LC(1 - k_m)\}\{1 + sCR + s^2LC(1 + k_m)\}} \quad (1)$$

Equation (1) can also be expressed in the canonical form (2), where the variable values are shown in Table I:

$$Z_{MC}(s) = sLk_m \left\{ \frac{Q\omega_n \frac{\omega_{n1}}{Q_1}}{\omega_{n1}^2 + s\frac{\omega_{n1}}{Q_1} + s^2} \right\} \left\{ \frac{Q\omega_n \frac{\omega_{n2}}{Q_2}}{\omega_{n2}^2 + s\frac{\omega_{n2}}{Q_2} + s^2} \right\} \quad (2)$$

The two magnetically coupled second-order tanks (each with a self-resonant frequency ω_n and Q) exhibit a trans-resistance with two natural resonant frequency peaks, at ω_{n1} and ω_{n2} . Assuming $Q > 5$, and $k_m > 0.6$, it can be shown that $Z_{MC}(s)$ simplifies to

$$|Z_{MC}(j\omega)_{\omega=\omega_{n1}, \omega_{n2}}| = \frac{1}{2} \frac{L(1 \pm k_m)}{CR} \quad (3)$$

While the transresistance of magnetically coupled tanks at the natural resonance frequencies can be mathematically derived, a more intuitive interpretation follows by considering the terms Q_1 and Q_2 . Due to the magnetic coupling, the effective inductance at ω_{n1} changes from L to $L(1 - k_m)$. Therefore, effective Q of the inductor changes to

$$|Q_L|_{\omega=\omega_{n1}} = \frac{\omega_{n1}L(1 - k_m)}{R} = \frac{1}{R} \sqrt{\frac{L(1 - k_m)}{C}} = Q_1 \quad (4)$$

The equivalent parallel load resistance due to a single LC tank at the frequency ω_{n1} can be computed using the standard series-to-parallel impedance transformation

$$R_{LC} = (1 + Q_1^2) R \approx Q_1^2 R \quad (5)$$

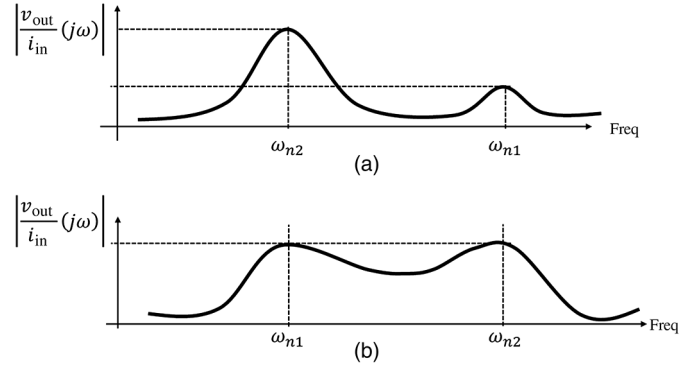


Fig. 4. (a) Trans-resistance of a magnetically coupled (MC) and electrically coupled (CC) resonant tank. (b) Trans-resistance of a gain-equalized transformer.

Finally, since there are two resonant tanks, the effective trans-resistance is the parallel combination of two resistors of value R_{LC} which gives

$$|Z_{MC}(j\omega)_{\omega=\omega_{n1}}| = \frac{1}{2} Q_1^2 R \quad (6)$$

The trans-resistance obtained by the intuitive approach (6) agrees well with (3).

Peak splitting in magnetically coupled resonant tanks is achieved by increasing the mutual-inductance or magnetic-coupling coefficient (k_m) between the resonant tanks. However, from (3), $|Z_{MC}(j\omega)_{\omega=\omega_{n1}}|$ and $|Z_{MC}(j\omega)_{\omega=\omega_{n2}}|$ are only equal if $k_m = 0$. Thus, as shown in Fig. 4(a), *peak-splitting* based solely on magnetic coupling exhibits an inherent amplitude mismatch.

B. Electrically Coupled Resonant Tanks

The trans-resistance of electrically coupled resonant-tanks, shown in Fig. 3(b), is given by

$$|Z_{CC}(s)| = \frac{1}{2} \frac{sC_c(sL + R)^2}{\{s^2L(C_c + C) + sR(C_c + C) + 1\}\{s^2LC + sRC + 1\}} \quad (7)$$

The values of ω_{n1} , ω_{n2} , Q_1 , and Q_2 from the equivalent canonical form are given in Table I. The spacing between the two resonant peaks can be increased by increasing the value of the coupling capacitance C_c . In contrast to magnetically coupled resonant tanks where the location of both poles ω_{n1} and ω_{n2} changes, electric-coupling only moves the location of one pole ω_{n2} , while ω_{n1} remains fixed. However, it is interesting to note that in terms of the parameters Q_1 and Q_2 , the expressions for the trans-resistance of electrically coupled and magnetically coupled tanks are identical:

$$|Z_{CC}(j\omega)_{\omega=\omega_{n2}}| = \frac{1}{2} Q_2^2 R = \frac{1}{2} \frac{1}{R} \frac{L}{C + C_c} \quad (8)$$

$$|Z_{CC}(j\omega)_{\omega=\omega_{n1}}| = \frac{1}{2} Q_1^2 R = \frac{1}{2} \frac{1}{R} \frac{L}{C} \quad (9)$$

From (8) and (9), *peak-splitting* based solely on electric-coupling also exhibits amplitude mismatch.

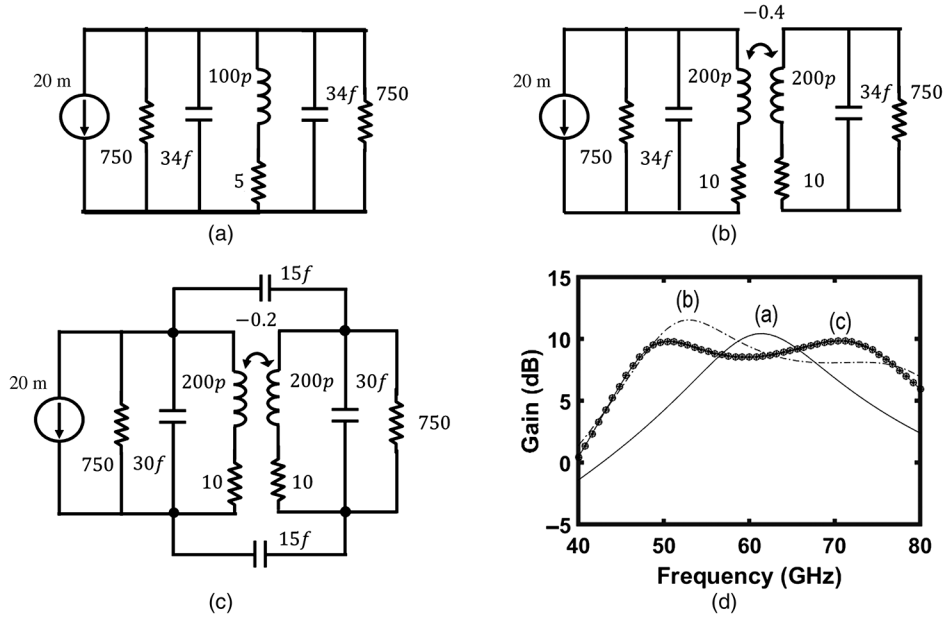


Fig. 5. (a) LC load. (b) Magnetically coupled transformer. (c) Gain-equalized transformer. (d) Comparison of the trans-resistance of circuits a, b, c.

C. Electrically and Magnetically Coupled Resonant Tanks

The amplitude mismatch in magnetically/electrically coupled resonant tanks relates to the dependence on a single coupling variable, k_m (magnetic-coupling coefficient) or k_c (electric-coupling coefficient), where

$$k_c = \frac{C_c}{C_c + C_2}. \quad (10)$$

Unequal peaks were identified as a problem for resonant-mode-switching-voltage-controlled oscillators by Li *et al.* [15]. To overcome this limitation, they proposed to introduce a capacitance across the windings of a transformer. The resulting structure, shown in Fig. 3(c), has two independent design parameters, k_m and k_c , and a trans-resistance $Z_{MC-CC}(s)$, defined in (11).

It can be observed that in the two limiting cases $k_m = 0$ and $C_c = 0$, $Z_{MC-CC}(s)$ simplifies to $Z_{MC}(s)$ and $Z_{CC}(s)$, respectively. Equation (11) can be expressed in the canonical form (12) with the values provided in Table I [(11) and (12) are shown at the bottom of the page].

Similar to magnetically coupled, and electrically coupled resonant tanks discussed in previous sections, the trans-resistance of resonant-tanks with both magnetic *and* electric-coupling at the natural resonant frequencies ω_{n1} and ω_{n2} can be described by

$$|Z(j\omega)_{\omega=\omega_{n1}}| = \frac{1}{2} Q_1^2 R = \frac{1}{2} \frac{L}{R} \frac{L(1-k_m)}{C+C_c} \quad (13)$$

$$|Z(j\omega)_{\omega=\omega_{n2}}| = \frac{1}{2} Q_1^2 R = \frac{1}{2} \frac{L}{R} \frac{L(1+k_m)}{C}. \quad (14)$$

From (13) and (14), the upper and lower resonant peaks will be equal (hence the name *gain-equalized* transformer) if

$$k_c = -2k_m / (1 - k_m). \quad (15)$$

Equation (15) is a key result. For a given magnetically coupled tank, the idea is to introduce a capacitor C_c such that (15) is satisfied. The expected trans-resistance is shown in Fig. 4(b). An important point to note is that k_c (defined in (11)) is bound between 0 and 1. Therefore, in order to satisfy (15), k_m has to be negative. In other terms, the cross-coupling capacitor must be connected across the transformer terminals with negative magnetic-coupling coefficient.

D. Design Example

To provide further insight into the design of gain-equalized transformers, consider the three circuits in Fig. 5(a)–(c). For ease of elucidation, the Z_{OUT} of the driver stage and Z_{IN} of the load stage have been assumed to be 750Ω with a capacitance of approximately 30 fF . The goal is to design a wideband resonant load for the amplifier to operate at 60 GHz , where the metric of comparison is trans-resistance.

The design of the shunt-LC load is straightforward. To resonate the 60 fF capacitance on the output node at 60 GHz , an

$$Z_{MC-CC}(s) = \frac{s \frac{C_c}{2} \{sL(1-k_m) + R\} \{sL(1+k_m) + R\} + sLk_m}{[s^2L(C_c + C)(1-k_m) + s(C_c + C)R + 1][s^2LC(1+k_m) + sCR + 1]} \quad (11)$$

$$Z_{MC-CC}(s) = \omega_{n1}^2 \omega_{n2}^2 \frac{s \frac{C_c}{2} \{sL(1-k_m) + R\} \{sL(1+k_m) + R\} + sLk_m}{[s^2 + s \frac{\omega_{n1}}{Q_1} + \omega_{n1}^2][s^2 + s \frac{\omega_{n2}}{Q_2} + \omega_{n2}^2]} \quad (12)$$

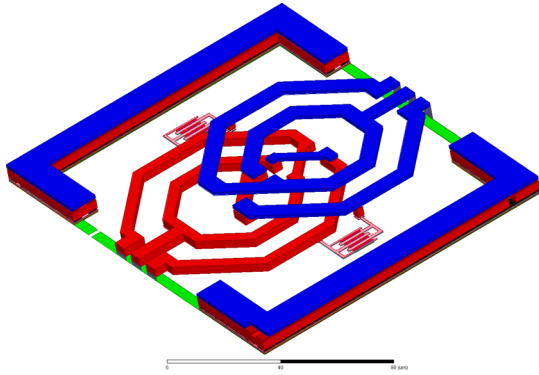


Fig. 6. Layout used to model one of the gain-equalized transformer in HFSS.

inductance of approximately 100 pH is required. Assuming a Q of 7.5, the resulting trans-resistance is plotted as a function of frequency in Fig. 5(d). An increase in the bandwidth (and reduction in trans-resistance) can be obtained by reducing Q of the LC load. Next, to widen the bandwidth, consider magnetically coupled resonant tanks in Fig. 5(b). The total output capacitance is split into two equal components of 30 fF each, and therefore, each inductor can be doubled to 200 pH. For a fair comparison, the inductor Q is kept the same. As k_m increases, the location of the poles at ω_{n1} and ω_{n2} will follow the results described in Table I. From the frequency response with $k_m = 0.4$, shown in Fig. 5(d), one observes that the amplitude mismatch in the resonant peaks limits the 3 dB bandwidth of the overall frequency response.

To equalize the first and second peaks, electric-coupling is introduced between the magnetically coupled resonant tanks. For a fair comparison between the circuits in Fig. 5, inductors of equal value and Q have been utilized. Moreover, to ensure the resonant peaks occur at same frequency for circuit-b, $k_m = -0.2$. From (15), it follows that for gain-equalization, $k_c = 1/3$ is required. The trans-resistance, or effectively the gain of each circuit, is plotted in Fig. 5(d). The gain-equalized transformer has equal trans-resistance at the even- and odd-order resonant peaks and therefore achieves a trans-resistance bandwidth of the 33 GHz.

To further illustrate the procedure to design wideband amplifiers using the gain-equalized transformers, consider the model of the gain-equalized transformer shown in Fig. 6. To create a reference design, the model is first simplified by removing the coupling capacitors. An electromagnetic (EM) simulation is performed to generate the transformer's S -parameters. Based on the S -parameters, the lumped element model shown in Fig. 3(a) is extracted to estimate C and k_m . Coefficient k_c can be calculated from (15). Based on the additional capacitance required to tune the transformer for the correct operating frequency, k_c can be used to estimate the coupling capacitor from (10). Finally, the coupling capacitors are added to the EM model, and the S -parameters are again generated. With all conditions being equal, the frequency response of a mm-wave amplifier loaded with the 1) normal transformer and 2) gain-equalized transformer is plotted in Fig. 7. The observation can be made that equalizing the gain of the even and odd-order peaks in the load results in an increase in the 3 dB bandwidth of the amplifier.

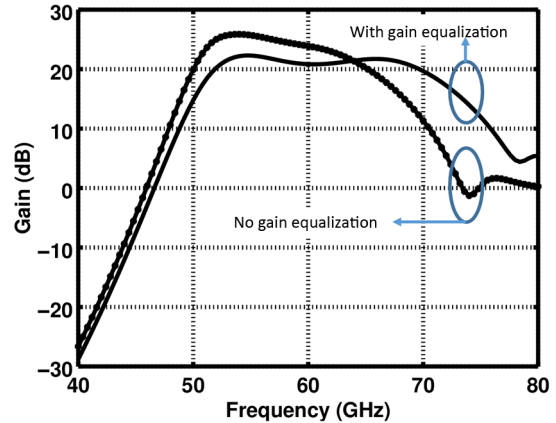


Fig. 7. Gain versus frequency plot of the mm-wave LNA with and without gain-equalization on the transformer load.

E. Physical Implementation

The primary and secondary windings of the transformer are designed in the top two metal layers. The mutual magnetic coupling between the windings of the lateral transformer is controlled by varying the degree of overlap. The cross-coupling capacitors are implemented using metal-oxide-metal (MOM) capacitors. To minimize the impact of process variation, minimum-sized capacitors were not used. In addition, each capacitor is surrounded by floating dummy capacitors to minimize abrupt metal density variation in the vicinity of the desired cross-coupling capacitors. The cross-coupling capacitors were included in the EM model to improve the simulation accuracy.

F. Limitations

In the proposed gain-equalized transformer, there is a trade-off between 3 dB bandwidth and pass-band droop. In order to increase the bandwidth (for a fixed center-frequency), the spacing between the even- and odd-order resonance frequency is made larger to increase the magnetic or capacitive coupling between the resonant tanks. If Q of the tank is fixed, then as the even- and odd-order resonance frequencies move apart, the droop increases.

IV. RECEIVER CIRCUIT DESIGN

An on-chip transformer-based balun was used to interface the single-ended antenna with a differential LNA input. The on-chip balun has a turns-ratio of 1:2 and provides a wide-band impedance match with 6 dB of passive voltage gain. The balun was simulated along with the input probe pads in a single EM model (Fig. 8). The schematic for the three-stage LNA is shown in Fig. 9(a). The first stage of the LNA is realized as a common-source topology instead of a cascode topology to mitigate the effects of noise-figure degradation due to the cascode transistor. To improve the reverse isolation, the LNA second and third stages employ cross-coupled transistors for C_{GD} neutralization. Each stage of the LNA is loaded with gain-equalized transformers ($k_m = -0.16$ and $k_c = 0.28$). The LNA achieves a gain of 18 dB while consuming 35 mA of current.

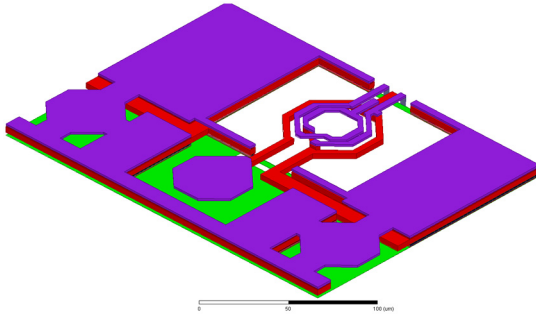


Fig. 8. HFSS model with the GSG pad and the input balun.

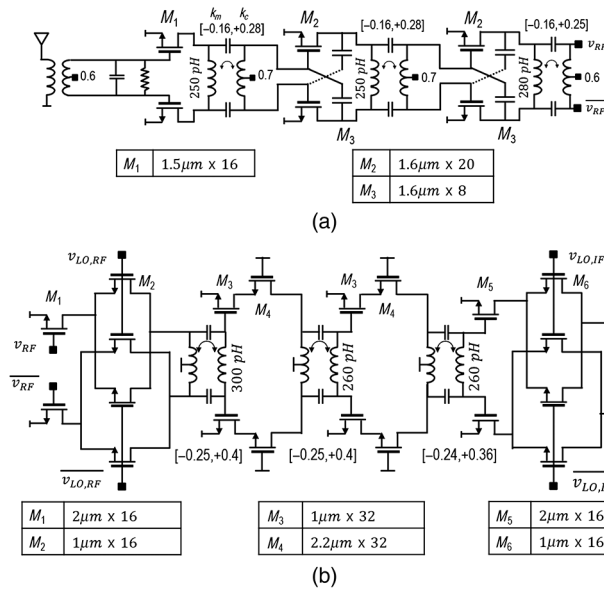


Fig. 9. Schematic diagram of (a) three-stage LNA and (b) mm-wave mixer, two-stage IF-amplifier, and IF-mixer.

The schematic of the mm-wave mixer, IF-amplifier, and IF-mixer is shown in Fig. 9(b). In the 60 GHz standard, the mm-wave signal is composed of four channels of equal bandwidth. Therefore, in a fixed IF architecture, as the signal progresses from RF to IF, the absolute bandwidth of the signal reduces. In contrast, in the ultra-broadband RFIC described in this work, the goal is to downconvert the entire mm-wave bandwidth to baseband. As a result of the absolute signal bandwidth remaining fixed while the center-frequency reduces, the fBW of the amplifiers increases from 29% at RF to 43% at IF. Higher fBWs necessitates a lower loaded-Q in the IF-amplifier compared to the LNA. Therefore, for the same current consumption, the gain of the LNA is higher than the IF-amplifier.

The LNA drives a double-balanced active mixer, which converts the 51–71 GHz mm-wave signal to an IF of 31–51 GHz using a 40 GHz LO. The mixer has a conversion loss of 3 dB while consuming 12 mA of current. Compared to the LNA, a higher degree of peak-splitting is required to maintain a high fBW through the IF-stage. As a result, the gain-equalized transformers in the IF stage have coupling coefficients of $k_m = -0.24$ and $k_c = 0.38$. The IFA consists of a two-stage cascode amplifier and provides 5 dB of gain to compensate for the loss of the mm-wave mixer. The IFA drives a single-phase

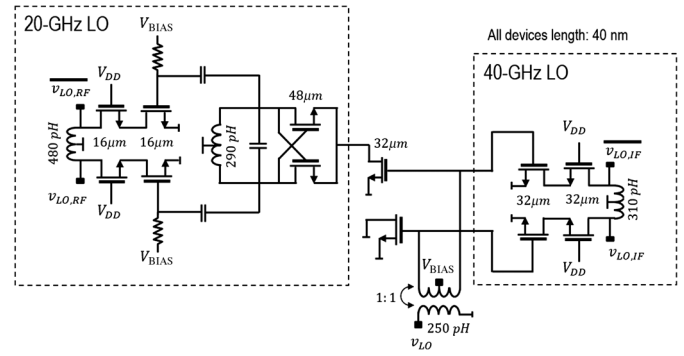


Fig. 10. Schematic of the LO distribution network for both sets of mixers.

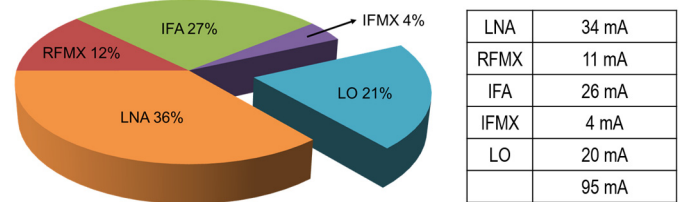


Fig. 11. Power breakdown for the different circuit blocks.

IF mixer. For a complete transceiver solution, a quadrature IF downconversion system is essential. However, the purpose of this implementation was to demonstrate high fBWs, and only one mixer of the I/Q downconverter was realized.

The schematic of the LO distribution network is shown in Fig. 10. The 40 GHz LO for the IF-mixer was generated by an off-chip signal generator that drives an on-chip balun. The IF-mixer is driven by a cascode LO-buffer. The LO for the mm-wave mixer is generated using an LC injection-locked divider. A 20 GHz cascode buffer isolates the mm-wave mixer from the injection-locked divider.

A breakdown of power consumption for the various receiver blocks is shown in Fig. 11; note, the percentage power consumption of the LO driver for the prototype receiver (one element of the phased-array) is comparable to the power of the IFA. If the receiver utilizes an N-element phased-array receiver with LO phase-shifting/IF signal-combining, the IFA power is fixed while the LO-power scales up by N^2 . The equal power consumption of the IF-amp and the LO in the single-element receiver is predictive of the overall power consumption of a phased-array system, i.e., as the number of elements increases so does the LO power. Eventually with enough elements, the LO power consumption will dominate the total receiver power. Therefore, architectures which focus on minimizing the LO-distribution power are crucial for future phased-array mm-wave transceivers.

Finally, it is important to note that approximating a true-time delay (required for coherent signal combining) with a phase-shift is valid only when the received signal has a small fBW. The techniques proposed in this paper deal with ultra-wide bandwidth signals. Therefore, to extend this work toward a complete phased-array implementation, a thorough study of the impact of the phase-shift approximation on the received signal EVM [12] is required.

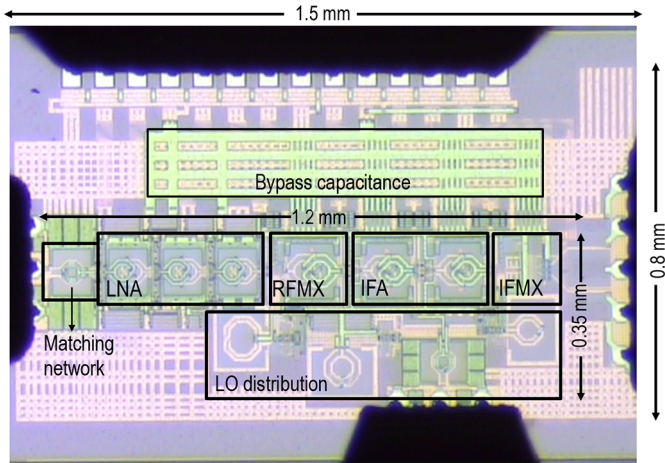
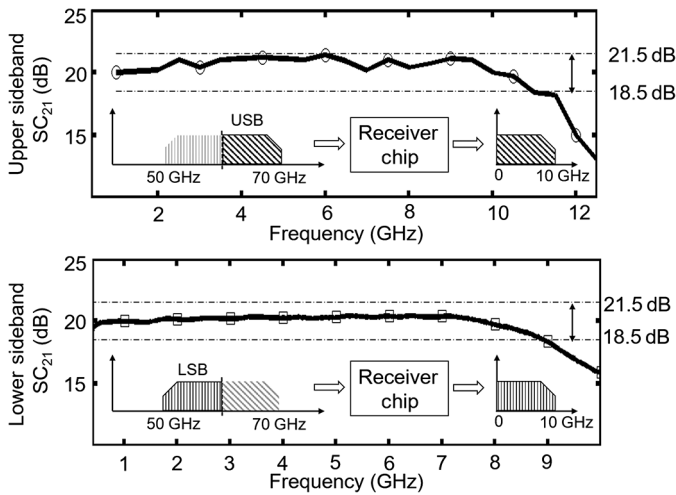


Fig. 12. Die micrograph of the mm-wave CMOS receiver.


 Fig. 13. Receiver frequency response measured at the baseband output. Referred to the receiver front-end, a gain of 20 ± 1.5 dB is maintained across a 51–71 GHz bandwidth.

V. MEASUREMENT RESULTS

A die photograph of the prototype mm-wave receiver chip fabricated in a 40 nm CMOS process is shown in Fig. 12. The metal stack consists of a six standard metal layers, one ultrathick metal (UTM) layer, and one aluminum passivation (AP) layer. The entire chip, including the mm-wave wafer-probe pads, occupies an area of $0.8 \text{ mm} \times 1.5 \text{ mm}$. The core receiver area, including the signal-path and LO-path, is $0.35 \text{ mm} \times 1.2 \text{ mm}$ only.

The measured channel frequency response of the entire receiver at the baseband output is shown in Fig. 13. The mm-wave input spectrum is broken down into two components: an upper-sideband (USB) extending from 60 to 70 GHz, and the lower-sideband (LSB) from 60 to 50 GHz. At the output of the receiver, both sidebands are downconverted to the same baseband frequency (0–10 GHz). In the USB, the receiver achieves a nominal power gain of 20 dB over a frequency range of 60–71 GHz. In the LSB, the receiver achieves a nominal power gain of 20 dB with ± 1.5 dB of gain variation over a

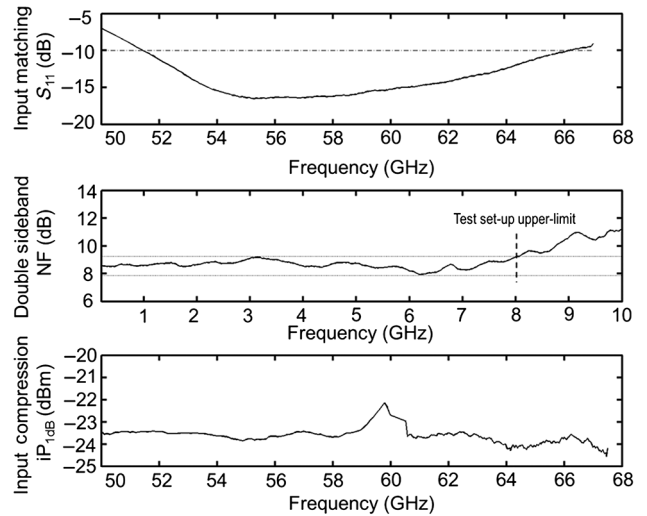


Fig. 14. Measured input matching, noise-figure, and input compression point.

frequency range of 51–60 GHz. The effective mm-wave bandwidth of the receiver is from 51 to 71 GHz. In the passband, the frequency response of the multistage receiver is flat and now shows indication of ripples due to the staggered resonant peaking of multiple gain-equalized transformers used along the signal path. The minimum DSB noise-figure of the entire receive-chain is 7.8 dB. The DSB-NF remains less than 9.3 dB up to a frequency of 8 GHz. The noise-figure degradation at frequencies greater than 8 GHz is attributed to the upper frequency limit of the noise-figure measurement setup.

The receiver achieves an input-referred 1 dB compression-point of -24 dBm and is plotted versus frequency in Fig. 14. The simulated group-delay across the entire receiver chain varies from 250 to 100 ps. The entire chip consumes 104 mW from a 1.1 V supply; this includes the power of the signal-path and the LO distribution path. As mentioned previously, the prototype receiver presented in this paper does not contain an I/Q IF-mixer. Based on the power breakdown in Fig. 11, an additional 10 mW of power consumption was added to our measured results to account for the extra quadrature-mixer that would otherwise be needed in a full system. The reported power per unit bandwidth is 115 mW/21 GHz or 5.5 pW/Hz.

VI. COMPARISON WITH PRIOR-ART

This mm-wave receiver utilizes multiple instances of gain-equalized transformers, where the resonant-peaks of the mm-wave front-end and IF-stage are staggered and tuned to achieve a flat frequency response from the LNA input to the baseband output. While the application of capacitive cross-coupling in a transformer has previously been applied for a resonant-mode switching-based oscillator design [15], this is the first use of this technique for bandwidth extension in the signal path.

Innovative circuits and architectures aimed at capturing wide bandwidths in the mm-wave spectrum have received considerable interest over the past decade. The performance of this prototype receiver is compared to other state-of-the-art implementations in technologies such as SiGe, BiCMOS, SOI, and standard CMOS in Table II. As described previously, direct

TABLE II
COMPARISON WITH STATE-OF-THE-ART WIDEBAND RECEIVERS

	[9]	[16]	[17]	[18]	This work
Tech	45-nm SOI-CMOS	130nm SiGe-BiCMOS	65nm CMOS	180nm BiCMOS	40-nm CMOS
BEOL	NA	6-metal, 2 UTM	7-metal, 2 UTM, 1 Al	6-metal, 1 Al	6-metal, 1 UTM, 1 Al
Architecture	Heterodyne	Direct conversion	Sliding IF heterodyne	Direct conversion	Heterodyne
F_{LO-RF}, F_{LO-IF} (GHz)	NA	76, x	37.3–42.9 18.6–21.9	NA	20, 40
RF-BW (GHz)	45–66	70–80	53–66	75–95	51–71
IF-BW (GHz)	1.2	x	4.5 ⁺	x	31–51
BB-BW (GHz)	NA	6	1.2 ⁺	~ 8	11 (USB) 9 (LSB)
Power (mW) output buffer power not included	30 (per element)	180 ^{1a}	61 ^{2a}	250 ³	115 ⁵
Gain (dB)	26.2	50	35.5 (voltage-gain)	37	20
NF (dB)	> 5.5	< 7	5.6–6.5	< 7	< 9.3
iP1dB (dBm)	–27	–51	–39	–35	–24
Group delay (ps)	NA	< 9ps (sim) BB amp only	NA	NA	100–250 (sim)
VDD(V)	1.1	1.5,2.5,3.3	1–1.2	2.5	1.1
Area (mm ²) (including pads)	0.8	2.1 mm ²	2.6 mm ²	3.4 ⁴	1.2
FoM = $\frac{\text{Power}}{2 * \text{BB-BW}}$ (pW/Hz)	25	15	25.4	15.6	5.5

⁺Target IF-BW listed in [17], BB-BW estimate based on the 60 GHz standard specifications.

¹Estimated power of LNA, IQ-Mixer, baseband, $\frac{1}{2}$ clock-tree based on this table [16].

²Estimated power of RX-front end, VCO, VCO buffers based on this table [17].

³Estimated per channel power based on Table I [18].

⁴Area of the entire four-element phase-array chip.

⁵Added 10 mW to the measured power consumption to account for Q-mixer.

conversion as well as heterodyne architectures have been explored. The receivers reported in [9], [16]–[18] have front-end circuits with fBW of 13%, 21%, 23%, and 38%, respectively. Among all the receivers, the prototype IC described in this section has the highest baseband bandwidth, 11 GHz in the USB, and 9 GHz in the LSB. It would be fair to note that the ultra-wideband operation comes at the expense of the noise-figure, e.g., the NF is degraded by 2.8 dB with respect to [17].

The figure-of-merit used for comparison with other reported receivers is power consumption per unit Hertz. Power efficiency is a strong function of the metal stack available in the process. Therefore, the metal stack available in each process has been included in Table II. This receiver consumes 115 mW of power from a 1.1 V supply, while providing a flat conversion-gain over an effective baseband bandwidth of $(11 + 9)/2$ or 10 GHz. The receiver FoM of 5.5 pW/Hz is the lowest among all the compared systems.

VII. CONCLUSION

This paper presents the design of an ultra-broadband heterodyne receiver intended for use in low-power phased-array systems which contain a large number of elements. The device

occupies 1.2 mm² and exploits the properties of gain-equalized transformers throughout the signal path to achieve an overall flat in-band gain response of 20 dB across a 20 GHz bandwidth. The receiver has a DSB NF of 7.8 dB and an input-referred $P_{-1\text{dB}}$ of –24 dBm, while consuming 115 mW off a 1.1 V supply.

ACKNOWLEDGMENT

The authors would like to thank D. J. Allstot, R. Brockenbrough, M. Wiklund, and E. Lin for their technical advice.

REFERENCES

- [1] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Broderson, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.
- [2] S. Emami, C. H. Doan, A. M. Niknejad, and R. W. Broderson, "A 60-GHz down-converting CMOS single-gate mixer," in *IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, 2005, pp. 163–166.
- [3] A. Natarajan, S. Nicolson, M.-D. Tsai, and B. Floyd, "A 60-GHz variable-gain LNA in 65 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2008, pp. 117–120.

- [4] J. Lee, M. Liu, and H. Wang, "A 75-GHz phase-locked loop in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1414–1426, Jun. 2008.
- [5] B. Razavi, "A 60 GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.
- [6] B. Afshar and A. M. Niknejad, "A robust 24 mW 60 GHz receiver in 90 nm standard CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2008, pp. 182–183.
- [7] E. Laskin *et al.*, "Nanoscale CMOS transceiver design in the 90-170-GHz range," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3477–3490, Dec. 2009.
- [8] K. Okada *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK direct-conversion transceiver for IEEE 802.15.3c," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec. 2011.
- [9] S. Kundu and J. Paramesh, "A compact, supply-voltage scalable 45–66 GHz baseband-combining CMOS phased-array receiver," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 527–542, Feb. 2015.
- [10] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 GHz wideband QPSK receiver in 65 nm CMOS," in *IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, 2014, pp. 357–360.
- [11] H. T. Friss and C. B. Feldman, "A multiple unit steerable antenna for short-wave reception," *Proc. Inst. Radio Eng.*, vol. 25, pp. 841–717, Jul. 1937.
- [12] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver-LO phase-shifting approach," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 614–626, Feb. 2005.
- [13] D. Parker and D. C. Zimmermann, "Phased arrays—Part 1: Theory and architectures," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 678–687, Mar. 2002.
- [14] V. Bhagavatula, M. Taghivand, and J. C. Rudell, "A compact 77% fractional bandwidth CMOS band-pass distributed amplifier with mirror-symmetric Norton transforms," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1085–1093, May 2015.
- [15] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, Jun. 2012.
- [16] I. Sarkas *et al.*, "An 18-Gb/s, direct QPSK modulation SiGe BiCMOS transceiver for last mile links in the 70–80 GHz band," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1968–1980, Oct. 2010.
- [17] F. Vecchi *et al.*, "A wideband receiver for multi-Gbit/s communications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, Mar. 2011.
- [18] S. Shahramian, Y. Baeyens, N. Kaneda, and Y.-K. Chen "A 70–100 GHz direct-conversion transmitter and receiver phased array chipset demonstrating 10 Gb/s wireless link," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1113–1125, May 2013.



Venumadhav Bhagavatula (S'11–M'15) received the B.E. degree in electronics and communication from the University of Delhi, New Delhi, India, the M.Tech. degree in electronic design technology from the Indian Institute of Science, Bangalore, India, and the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2005, 2007, and 2013, respectively.

Since 2014, he has been with the Modem Laboratory, Samsung Semiconductors Inc., San Jose, CA, USA. His research interests include RF/mm-

wave, and low-power mixed-signal circuits.

Dr. Bhagavatula was the recipient of the CEDT Design Medal from the Indian Institute of Science (2007), and the Analog Devices Outstanding Student Designer Award (2012). He was a corecipient of the Best Student Paper Award at the RFIC 2014.



Tong Zhang (S'12) received the B.S. degree from Southeast University, Nanjing, China and the M.S. degree from the University of Washington, Seattle, WA, USA, in 2011 and 2014, respectively, both in electrical engineering. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Washington.

From July 2013 to March 2014, he was an Intern with Qualcomm Atheros, San Jose, CA, USA, working on developing new techniques for wideband IQ generation. From April 2015 to July 2015, he was an

Intern with Google, Mountain View, CA, USA, for analog circuit design. His research interests include self-interference mitigation systems and millimeter-wave transceivers.

Mr. Zhang was the recipient of the Analog Device Outstanding Student Designer Award in 2015.



Apsara Ravish Suvarna received the B.E. degree in electronic and communication from the National Institute of Technology Karnataka, Surathkal, India, and the M.S. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2006 and 2013, respectively.

From 2006 to 2010, she was an Analog Designer with the Power Management Group, Cosmic Circuits Pvt. Ltd., Bangalore, India, where she worked on low-drop out regulators, bandgap references and power-on-reset circuits. From 2013 to 2015, she worked as an RFIC Designer with the Cellular Transceiver Group, Qualcomm, San Diego, CA, USA. Since 2015, she has been with the Wireless-RF Solutions Group, Maxim Integrated Products, Inc., San Jose, CA, USA. Her research interests include RF circuit and system design, and low-power mixed-signal circuits.



Jacques Christophe Rudell (S'96–M'00–SM'09) received the B.S. degree from the University of Michigan, Ann Arbor, MI, USA, in 1989 and the M.S. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA, all in electrical engineering, in 1994, 2000 respectively.

After completing his degrees, he worked for several years as an RF IC Designer with Berkana Wireless (now Qualcomm), San Diego, CA, USA, and Intel Corporation, Santa Clara, CA, USA.

In January 2009, he joined the Faculty with the University of Washington, Seattle, WA, USA, as an Assistant Professor of Electrical Engineering. His research interests include topics in RF and mm-wave integrated circuits design for communication systems, in addition to biomedical electronics for imaging and neural interface applications.

Dr. Rudell is an active member at the Center for Sensorimotor Neural Engineering (CSNE), an NSF Engineering Research Center (ERC) based at the University of Washington. He served on the ISSCC Technical Program Committee (2003–2010), and on the MTT-IMS Radio Frequency Integrated Circuits (RFIC) Symposium Steering Committee (2002–2013), where he was the 2013 General Chair. He served as an Associate Editor for the *IEEE JOURNAL OF SOLID-STATE CIRCUITS* (2009–2015). He was the recipient the Demetri Angelakos Memorial Achievement Award, the 2008 ISSCC Best Evening Session Award, and the 2015 NSF CAREER Award. He has twice been corecipient of the Best Paper Awards at the IEEE International Solid-State Circuits Conference, the first of which was the 1998 Jack Kilby Award, followed by the 2001 Lewis Winner Award. He was also a corecipient of the 2011 and 2014 RFIC Symposium Best Student Paper Award.