A 55-70GHz Two-Stage Tunable Polyphase Filter with Feedback Control for Quadrature Generation with <2° and <0.32dB Phase/Amplitude Imbalance in 28nm CMOS Process

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***Abstract*— An integrated two-stage polyphase filters (PPFs) with feedback control is proposed for local oscillator (LO) quadrature generation at millimeter-wave band frequencies. The PPFs second stage utilizes triode-region NMOS transistors to implement variable resistors which are accurately controlled to minimize any IQ mismatch. A prototype quadrature signal generator for use in a homodyne 60GHz receiver is integrated in 28nm LP CMOS process. A worst-case measured phase and amplitude imbalance of 2° and 0.32dB across a frequency range of 55-70GHz is reported. The core IQ generator size is 20μm x 40μm while consuming 81μW, which includes 9μW for the feedback control loop and 40μA from 1.8V supply for the opamp. The input impedance is simulated to be 150Ω in parallel with 18fF.**

Keywords—Quadrature generation, Feedback control, Polyphase Filter(PPF), Millimeter wave integrated circuits, CMOS process.

I. INTRODUCTION

The evolution of smart phone and notebook computers continue to drive demand for higher data rates in the associated transceivers. Standards in the mmWave band, such as 60GHz, will eventually address the demand for increased connectivity by offering as much as 7GHz of worldwide unlicensed bandwidth. At lower frequencies (<10GHz), the popularity of the direct-conversion (zero-IF) architecture is due to the simplicity of the transceiver signal path and ease of integration. However, utilizing direct-conversion for mmWave receivers requires the generation of a highly amplitude/phase accurate IQ local oscillator (LO) to drive the mixers. The realization of a high accuracy mmWave IQ generator is one of the most challenging aspects of mmWave transceiver design. This is due to the extreme sensitivity of quadrature generation to mismatch at frequencies above 60 GHz. Fig.1 illustrates the issues of phase imbalance as a function of frequency for a given mismatch induced time delay error. A constant time delay mismatch of ΔT is dependent on the mismatch in device geometry and is relatively independent of frequency. A mismatch induced I/Q delay error of ΔT at a 100GHz will generate 10x higher phase mismatch as compared to an LO output running at 10GHz [1] assuming the same relative mismatch and delay error; this is illustrated in Fig.1.

Ideally, the LO I/Q signals should be equal in amplitude and 90° out of phase over the frequency band of interest to minimize the impact on EVM and bit error rate. Three methods commonly employed to generate LO I/Q signals include: (1) quadrature voltage control oscillators (QVCO), (2) divide-by-two circuits with a VCO running at twice the LO frequency, (3) polyphase filters (PPFs). Other methods, which are more often used for mmWave band applications include differential branch-line directional couplers [2], distributed microstrip shunt-stubs [3] and quadrature all-pass filters [4].

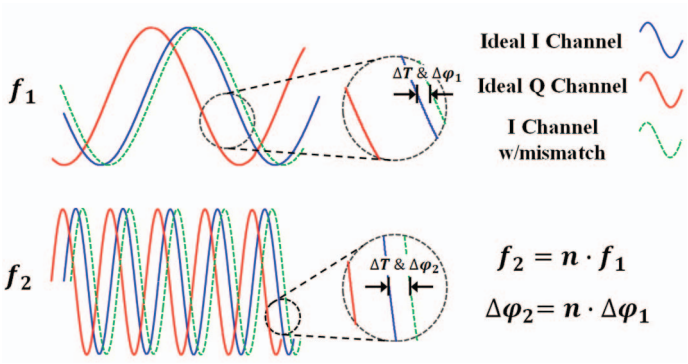

Fig.1 Illustration of phase imbalance at low and high frequency due to a mismatch induced timing error.

QVCOs use two cross-coupled oscillators that inherently produce a 90° phase difference between their outputs. Trade-offs exist with QVCOs between the coupling strength, I/Q phase accuracy, tuning range, and the phase noise (PN) performance. In addition, these oscillators typically have a lower tuning range and worse PN as compared to a conventional oscillator [5]. Injection locked QVCOs at 60GHz achieve good PN performance, but at the expense of a lower locking range [6]. Divide-by-two circuits generate I/Q signals for a VCO running at twice the desired LO frequency, however

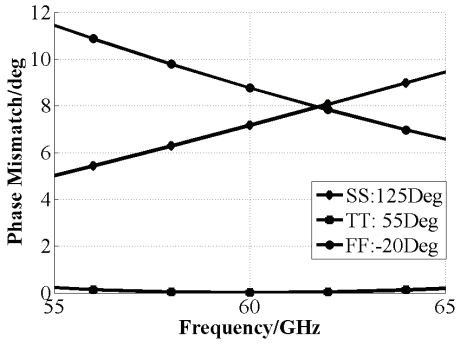

Fig. 2 Phase mismatch in two-stage PPFs plotted for several process and temperature corners

the VCO is required to operate at double the carrier frequency (ex: 120GHz for a 60GHz transceiver), which severely degrades the PN performance, lowers the tuning range, and increases the power consumption due to the low quality factor of the passive components [7]. Transmission line based methods mentioned in [2-4] often require significant silicon area to realize mmWave IQ generation and worse IQ mismatch.

PPFs are able to generate broadband precision quadrature LO signals with fractional bandwidths greater than 30% by cascading numerous stages. However, the fundamental insertion loss of the PPF limits the number of stages, hence restricting its use to narrow-band systems. Furthermore, the IQ balance of a PPF is dependent on the RC product, which may vary by as much as 30% over process and temperature. The phase mismatch of a typical two-stage PPF over process and temperature vs. frequency is shown in Fig.2. The PPFs were sized to operate at 60GHz in the TT corner 55 ˚C and the phase mismatch is simulated to be less than 0.5˚ over a bandwidth of 7GHz. However, at the corner of SS 125 ˚C or FF -20 ˚C, the phase mismatch goes beyond 8˚ due to a shift in the resistor/capacitors values, see Fig.2. This phase variation will severely degrade the EVM performance of a 60GHz system without calibration [8]. Introducing additional stages in the PPF will improve the IQ balance, however this increases the insertion loss by approximately 3dB for each additional stage, thus requiring more buffer stages between the PPF and mixer LO input. These buffers would also contribute additional IQ phase mismatch while consuming more power. Therefore, all the aforementioned solutions present a set of performance tradeoffs.

An ideal integrated quadrature generator would have the following characteristics:

- Perform precision quadrature balance while utilizing minimal silicon area.
- Minimal insertion loss and power consumption.
- Present a large input impedance, to relax the loading effects on the previous stage (could be the VCO).
- Minimize the sensitivity to process, voltage and temperature (PVT) variations.

The remainder of this paper describes a generic technique which embodies these ideal characteristics.

II. Proposed PPF Quadrature Generator

Fig.3 illustrates the proposed quadrature generation method which is based on a calibrated two-stage PPFs. In the proposed technique, the second stage resistors are replaced with transistors that operate in the triode-region. This allows modulation of the channel resistance to realize a variable resistor. A feedback network drives the gate voltage of the transistors and sets the channel resistance based on the process corner and temperature information. A 2k Ohm poly-resistor R_s is added in series with each gate, which couples the large LO input signal from the drain/source to the gate, to maintain a constant V_{GS} and hence a relatively fixed channel resistance.

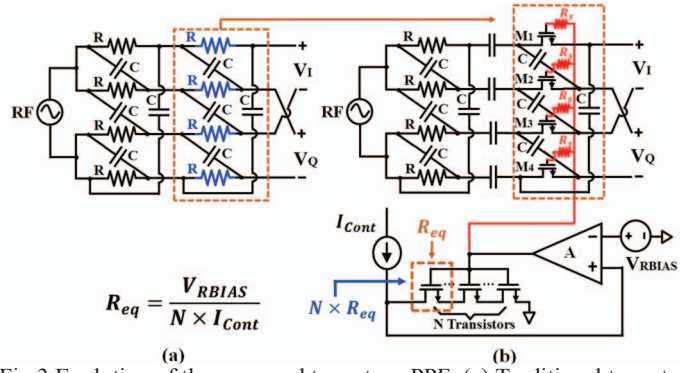

Fig.3 Evolution of the proposed two-stage PPF. (a) Traditional two-stage PPF (b) Two-stage PPF with feedback-controlled triode region transistors

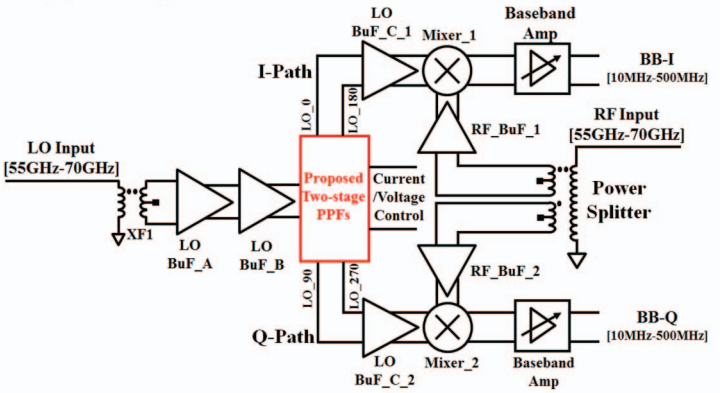

Fig.4 Block Diagram of the proposed system for IQ imbalance measurement

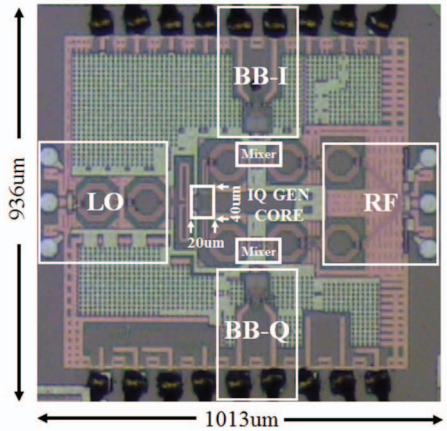

Fig. 5 28nm CMOS Quadrature Generator Chip Micrograph

The feedback network includes an operational amplifier, multiple replica transistors, a control voltage and current. Assuming each transistor has the same channel resistance, cascoding multiple (N) transistors reduces the power consumption of the feedback circuity by a factor of N. Also, with the same desired value of resistance, lowering the control voltage by 2x will result in a 4x power savings. The proposed circuit utilizes three cascoded transistors and the bias voltage is set to 100mV to minimize the power consumption.

With the feedback loop closed, the equivalent resistance in the PPF is set by the voltage V_{RBIAS} and the control current I_{Cont}.

$$R_{eq} = \frac{V_{RBIAS}}{N \times I_{Cont}}$$

Beyond minimizing the IQ phase/amplitude errors of the PFFs, there are two other essential features: 1) minimizing the insertion loss of the PPFs, 2) minimizing the loading of the components driving the IQ gen (either buffers or a VCO) which implies as high an input impedance as possible. Both the PPFs insertion loss and input impedance, influence the required number of buffer stages and ultimately the power consumption of the overall solution including the VCO, PPF, and buffers. The input impedance of the proposed QG is determined by the channel resistance of the triode-region devices and capacitors. In the extracted simulation, the proposed QG introduces 3.5dB insertion loss and presents an input impedance of 150 Ohm in parallel with 18fF.

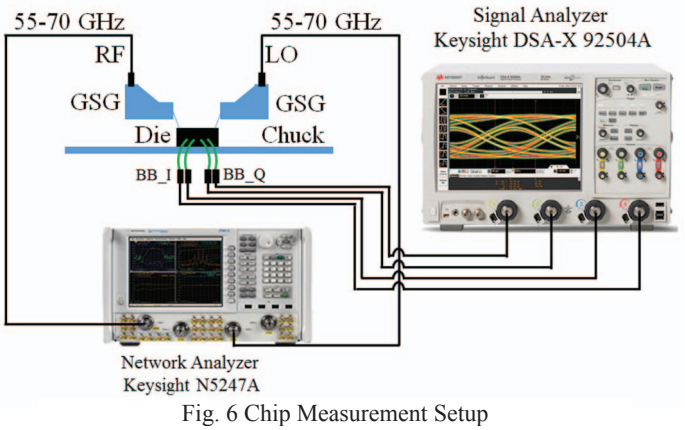

Fig. 6 Chip Measurement Setup

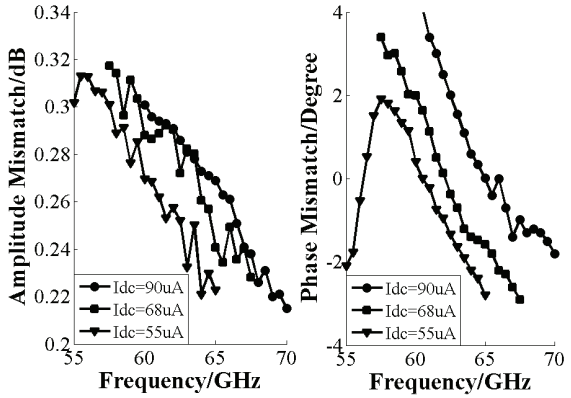

Fig. 7 Measured Amplitude/Phase mismatch of the proposed tunable IQ generator vs frequency for several values of I_{cont}.

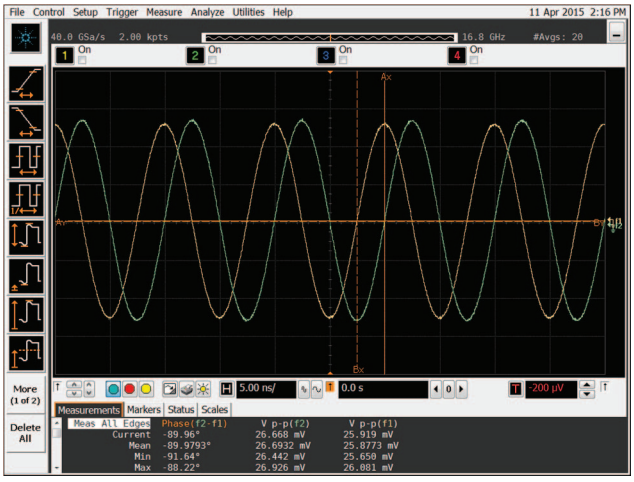

Fig. 8 Baseband quadrature output waveforms measured using oscilloscope. f_{RF} = 65GHz, f_{LO} = 64.9GHz, f_{IF} = 100MHz, V_{RBIAS} =100mV, I_{Cont}=90µA.

III. CIRCUIT IMPLEMENTATION

Two methods are commonly used to measure and characterize the quadrature imbalance. The first approach measures the IQ phase imbalance directly at the carrier frequency (mmWave band) using high-frequency probes. However, the measurement accuracy becomes limited by the phase mismatch introduced by the probes, the differential balance of the input signal and high frequency Short-Open-Load-Termination calibration error. The second approach first down-converts the LO where an accurate IQ imbalance measurement may take place at a much lower frequency. However, the down-converter design mandates the use of large device sizes (long-channel length devices) in the amplifiers, mixers and buffers to minimize any mismatch introduced by the test circuitry. The method of down-converting the LO before measurement was used to acquire the reported data.

Two down-conversion mixers with linear buffers, as shown in Fig.4, were used to measure the quadrature phase and gain accuracy. A single-to-differential (STD) power-splitter is used to generate two differential 55GHz-to-70GHz signals. An STD balun (XF1, see Fig.4) generates the differential signals for the input of proposed QG. To improve the differential balance of the input LO signal, two sets of buffers (BuF_A and BuF_B) are added between the STD and proposed QG. Another set of linear buffers (BuF_C_1 and BuF_C_2) are added after the QG to improve the voltage swing before driving the passive mixer (Mixer_1 and Mixer_2). Baseband linear amplifiers are connected after the mixers and drive a 50 Ohm port impedance on board with a simulated 3dB bandwidth of 10MHz-500MHz. Monte Carlo simulations have been done to show the worst case IQ amplitude/phase mismatch introduced by the buffers, amplifiers and mixers is 0.1dB/0.2°, respectively, which is minimal compared to the mismatches caused by the QG. In addition, any unexpected phase imbalance introduced by the test circuitry can be compensated for by the proposed PPFs.

IV. MEASUREMENT RESULTS

This chip was fabricated in a 28nm CMOS process with 1 UTM layer, 7-metal stack and occupies 0.936mm x 1.013mm including bond pads. The core two-stage PPFs with feedback control is compact and occupies an area of less than 20µm x 40µm. The die is assembled with the testboard using chip-on-board packaging. A die photo is shown in Fig.5. An L-compensated layout for the PPFs [9] is employed to further improve the quadrature balance.

This chip was characterized using Cascade 12000AP Summit on-wafer probe station. Measurements were performed mainly using an Agilent N5247A PNA-X network analyzer and Agilent 25GHz bandwidth DSA-X 92504A signal analyzer.

Table I. Comparison Table

	JSSC '05 [2]	JSSC '09 [3]	TMTT '12 [4]	This Work
Architecture	Branch Line Coupler	Distributed Microstrip Shunt-Stubs	Quadrature All-Pass Filter	Two-Stage Polyphase with FB Control
Freq (GHz)	57-64	55-65	55-78.5	55-70
Phase Mis (º)	<15	<5	<9.5	<2
Amp Mis (dB)	<1	<1.5	<0.5	<0.32
IL (dB)	-x-	2.5/4	>3dB$^{\lozenge}$	3.5dB[1b]
Input Impedance	-x-	-x-	40 Ohm // -x-	150 Ohm // 18fF[1a]
Area (um^2)	-x-	-x-	-x-	20×40[2a]
Power	0	0	0	5.5-9μW[2b]
Process	0.12um SiGe	90nm CMOS	0.13um SiGe	28nm CMOS

[1a]Extracted simulation results. [1b] Extracted simulation results with real loading from the following buffer stage.

$^{\lozenge}$Calculated from the ideal amplitude response of QAF with $\frac{R_S}{R} = 1$.

[2a] Area doesn't include the operational amplifier. [2b] Power consumption includes feedback circuity only, the opamp adds 40uA from a 1.8V supply.

The measurement setup is shown in Fig.6. In the measurements, 55-70GHz RF/LO signals were provided by an Agilent network analyzer N5247A and performed using on-wafer probing. Baseband output and DC signals were assembled with the board using chip-on-board packaging. The Agilent 25GHz bandwidth DSA-X 92504A signal analyzer was connected to the baseband output and measured the IQ imbalance in both the time and frequency domains.

The measurement results for the proposed quadrature generator are shown in Fig. 7. Both the phase and gain error over frequency are plotted for several values of control current from 55μA to 90μA. The proposed mmWave quadrature generation circuit maintains less than 0.32dB gain imbalance and 2° phase imbalance over a 7GHz bandwidth. The measured center frequency can be tuned across a frequency range of 55GHz to 70GHz.

A screen capture from an oscilloscope is shown in Fig.8 for an IQ signal. This measurement was taken with f_{RF}=65GHz, f_{LO}=64.9GHz and the control voltage/current are 100mV/90uA, respectively.

The proposed quadrature generators consumes 55-90μA for the control current of the feedback circuitry. Since the control voltage for the feedback circuitry is only 100mV, the actual power consumption introduced by the feedback circuitry is less than 9μW. The operational amplifier dissipates an additional 40μA from a 1.8V supply.

V. Conclusions

A feedback-controlled PPFs based method is proposed for high frequency accurate IQ generation. A prototype chip is designed with a measured IQ imbalance of less than 2° and 0.32dB over a 7GHz bandwidth centered from 55GHz to 70GHz. A detailed circuit performance/comparison is shown in Table I. To the author's knowledge, this technique reports the best phase and amplitude matched IQ generation method for mmWave (60GHz applications) reported to date with minimum silicon area.

Acknowledgment

This work was supported by Qualcomm Inc. The authors gratefully acknowledge the assistance of M. Ghahramani, C. Marcu, E. Lin, A. Keerti, R. Brockenbrough and B. Kim.

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