A Compact 77% Fractional Bandwidth CMOS Band-Pass Distributed Amplifier With Mirror-Symmetric Norton Transforms

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***Abstract*—This paper presents the design of a high fractional-bandwidth millimeter-wave band-pass distributed amplifier (BPDA) implemented in a 40 nm (LP) CMOS process. A high-order load impedance with multiple resonant elements is often used to realize wideband amplifiers. However, these implementations require the use of numerous inductors which occupy a prohibitively large amount of silicon area. A mirror-symmetric Norton transformation technique which reduces inductor component values for a wideband amplifier, allowing an area-efficient layout, is described in this paper. The BPDA consumes 34 mW while providing a power-gain of 7 dB from 24-to-54 GHz with less than 2 dB in-band gain-variation. The BPDA has a measured 77% fractional bandwidth, a +11 dBm in-band IIP3, and an in-band noise-figure less than 6.2 dB, while occupying an area of 0.15 mm^2.**

***Index Terms*—Band-pass filters, coplanar waveguide, distributed amplifier, millimeter-wave circuits, Norton transform.**

I. Introduction

OVER the past decade, the minimum feature size of silicon CMOS technologies have become nano-scale in dimension. Correspondingly, the unity power-gain frequency (f_{max}) of these devices have exceeded several hundred giga-hertz. Integrated systems designed in these advanced CMOS process nodes are capable of operating in the 'millimeter-wave' (mm-wave) band to address a broad range of applications, from passive imaging [1] to a wide variety of communication systems with data rates up to 100 Gb/s [2]. The opportunity to exploit the under-utilized mm-wave spectrum has opened the door to a variety of applications, including automotive radar at 22–29/77 GHz [3], [4], the newly standardized 60 GHz band at 57–64 GHz [5], along with the spectrum between 71–76 GHz and 81–86 GHz [6] (with no channelization restriction) for last-mile, and point-to-point wireless communication. However, effectively utilizing this spectrum requires power and area optimized circuit techniques to implement highly-integrated low cost silicon solutions capable of operating on ultra-wideband signals with high fractional bandwidths (fBW = absolute bandwidth/center-frequency).

A key challenge associated with high fBW integrated mm-wave systems is the silicon area occupied by the numerous resonant elements needed to realize a broadband response. Practical amplifiers are fundamentally bound by a finite gain-bandwidth product. Doubling the width of the device to increase the transconductance is accompanied with a proportional increase in the gate-to-source and drain-to-bulk capacitance and therefore, a decrease in bandwidth. Moreover, since these capacitances are inherent to the physical structure of the device, they cannot be eliminated. Circuit designers circumvent this problem by 'tuning' the load at the frequency of operation. The simplest solution is to add an inductor to resonate with the device/parasitic capacitor, resulting in a second order RLC load, which is extensively utilized for high-gain narrow-band amplifier designs at both RF and millimeter-wave frequencies. For wideband designs, multiple inductor solutions (higher order loads) such as inductive-peaking based bandwidth extension [7], transformer-feedback [8], T-match based matching networks [9], and LC ladder filter based approaches [10], [11] have been proposed in prior-art. All these solutions attempt to find an optimal (with respect to minimizing inductor value and area) topology to resonate the device capacitance across the widest bandwidth possible, with minimum in-band gain variation. However, since on-chip inductors occupy a large amount of silicon-area, the solution space is ultimately constrained by the number of inductors that can be practically integrated on-chip.

An alternate approach, extensively applied in wireline and optical applications [12], [13], is to achieve a wideband design through the use of a distributed amplifier (DA). Originally described in a patent disclosure in 1938 [14], the DA has been implemented using a variety of technologies, including vacuum-tube [15], bipolar, BiCMOS, GaAs, and CMOS [16]. Not surprisingly, a DA was one of the earliest reported millimeter-wave CMOS circuits [12]. However, two major barriers limit practical integrated implementations of the traditional low-pass DAs (LPDA) in wireless transceivers. First, the LPDA has a low-pass filter response. For most radio transceiver applications, selectivity is important in eliminating out-of-band interference

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along the signal chain, thus requiring components along the signal chain with a band-pass, rather than low-pass frequency response. The second, and more important constraint, is the large area associated with multiple on-chip spiral-inductors or transmission-lines. As a result, to date, relatively little exploration has been conducted on extending distributed amplification techniques to realize a band-pass frequency response. Discrete-component implementations of band-pass distributed amplifiers (BPDA) were first described in [17] and [18]. More recently, a SiGe-BiCMOS DA [19] employed a high-pass filter topology to reduce the number of inductors. In this paper, we explore techniques which allow practical fully-integrated, compact BPDAs for very wideband signal amplification.

This paper begins in Section II by describing the limitations of the canonical BPDA structure. In Section III, a design methodology which applies dual mirror-symmetric Norton transformations to realize a significantly more compact form of a BPDA is given. A detailed description of a prototype BPDA test-chip implemented in a 40 nm CMOS process is presented in Section IV, and, measured results and a comparison with prior-art are given in Section V.

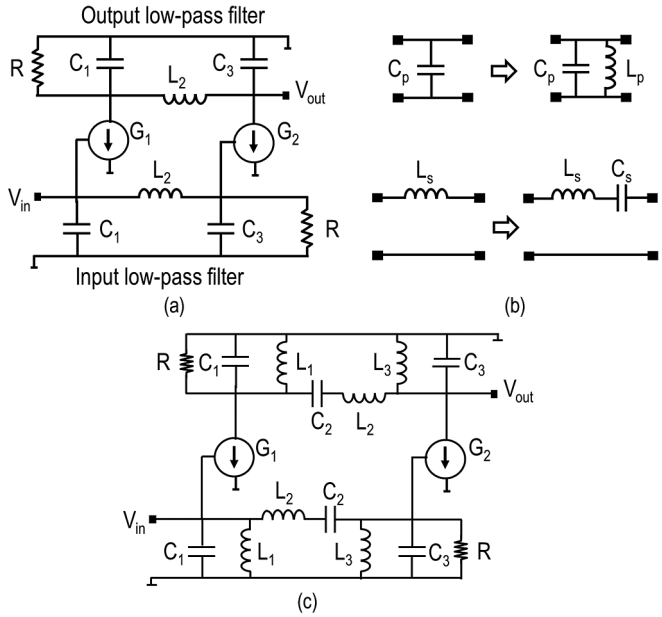

Fig. 1. (a) Canonical form of the LPDA (b) low-pass to band-pass filter transformation (c) canonical form of the BPDA.

II. Canonical Form of the BPDA

A simplified model of a two-stage LPDA is shown in Fig. 1(a). The LPDA is comprised of two gain-cells—ideal voltage-controlled current-sources (transconductance) G_1 and G_2. To simplify the notation, we assume that $G_1(G_2)$ has an equal input/output capacitance $C_1(C_3)$. The input/output capacitances are absorbed in the L-C low-pass ladder filters at the input and output nodes, respectively. In a BPDA, each low-pass filter (LPF) of the LPDA is replaced by a band-pass filter (BPF). A BPF can be derived from an LPF by replacing each series inductor, L, with a series L-C circuit, and likewise substituting a shunt L-C for each shunt capacitor, C; the filter transformation is shown in Fig. 1(b). The resulting canonical form of the BPDA is shown in Fig. 1(c). A major disadvantage of a BPDA as compared to the LPDA, is the increase in the number of inductors; this can be greater than a factor of 2. This increase in the number of inductors in the canonical BPDA would appear antithetical to the goal of realizing a compact DA. However, as will be described later, the addition of the two shunt inductors in the BDPA can be exploited when Norton Transformations are applied. A more subtle, but equally important, drawback in the canonical BPDA relates to the scaling of the inductive components (L_1, L_2, and L_3) as a function of bandwidth (BW) and center frequency (ω_c). These drawbacks are illustrated in the LPDA and BPDA design process that follows.

For the sake of simplicity, we again return to the third-order LPDA of Fig. 1(a). A series inductor, L_2, separates the capacitances of the gain-cells G_1 and G_2, to form two low-pass C-L-C filters, one at that input and the other at the output of the LPDA. The bandwidth of the DA is determined by determined by the bandwidth of the C-L-C network which forms the synthetic transmission line. Fortunately, a well-documented [20] algorithmic approach to select component values for the desired bandwidth and transfer function exists. As an example, a filter-coefficient table which may be used to obtain component values for a Butterworth filter response is shown in Table I. Here, K corresponds to the order of the filter, and g_k is a normalized constant which relates filter component values to the desired frequency response. Using Fig. 1(a) as a reference, for $N = 3$, the filter coefficients $g_1 = 1$, $g_2 = 2$, and $g_3 = 1$ map to C_1, L_2, and C_3, respectively. The coefficient values are normalized to a unit termination impedance and a unit bandwidth. To design a filter with a termination impedance of 50-ohms and a bandwidth, BW, the component values are:

$$R_1 = g_1 * Z_0 \tag{1}$$

$$C_1 = \frac{g_1}{BW * Z_0} \tag{2}$$

$$L_2 = \frac{g_2 * Z_0}{BW} \tag{3}$$

$$C_3 = \frac{g_3}{BW * Z_0} \tag{4}$$

$$R_4 = g_4 * Z_0. \tag{5}$$

From (3), one observes that as the desired BW of the filter increases, the value of inductor L_2 decreases. Therefore, assuming the inductors dominate the area, as the BW of the LPDA increases, the area of the circuit decreases.

Also, from (2) and (4), one notes that as the BW rises, the capacitors C_1 and C_2 decline in value. As described previously, the basic idea of distributed-amplification is to absorb the input and output capacitances of the gain cell into the low-pass C-L-C filter. Assuming a gain-cell implemented using either MOS or BJT devices, and a constant bias voltage, the input/output capacitance is directly proportional to the transconductance of the device. Thus, an increase in BW translates into smaller transistors and a lower gain from the LPDA.

The canonical BPDA, shown in Fig. 1(c), consists of capacitors (C_1, C_2, C_3) and inductors (L_1, L_2, L_3). Components

TABLE I
ELEMENT VALUES FOR MAXIMALLY FLAT LOW-PASS FILTER PROTOTYPE ($g_0 = 1, \omega_C = 1$, K = 1 TO 8)

K	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8	g_9
1	2.0000	1.0000							
2	1.4142	1.4142	1.0000						
3	1.0000	2.0000	1.0000	1.0000					
4	0.7654	1.8478	1.8478	0.7654	1.0000				
5	0.6180	1.6180	2.0000	1.6180	0.6180	1.0000			
6	0.5176	1.4142	1.9318	1.9318	1.4142	0.5176	1.0000		
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450	1.0000	
8	0.3902	1.1111	1.6629	1.9615	1.9615	1.6629	1.1111	0.3902	1.0000

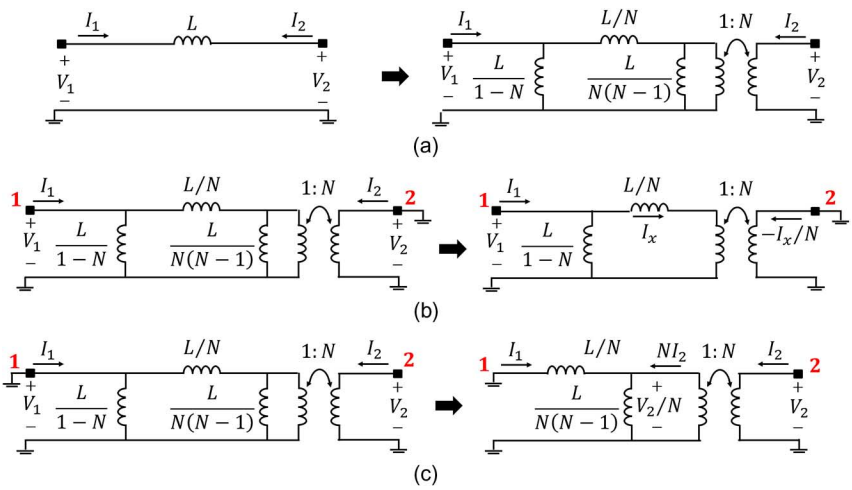

Fig. 2. (a) Norton transformation of a series floating inductor; (b) equivalent circuit for $y_{11B} = I_1/V_1$ and $y_{21B} = I_2/V_1$; (c) equivalent circuit for $y_{12B} = I_1/V_2$ and $y_{22B} = I_2/V_2$.

values for C_1, L_2, and C_3 are governed by (2) to (4). Similar to an LPDA, C_1, L_2, and C_3 scale down as bandwidth is increased. However, it is also important to note, from (2), that L_2 is independent of ω_c. Therefore, even if an increase in the center-frequency of the BPDA were desired, L_2 will remain the same. This is problematic for BPDAs with a high center frequency relative to the self-resonance frequency (SRF) of L_2.

The three additional components of the BPDA (L_1, C_2, L_3) are related to the BW, ω_c and termination impedance by

$$L_1 = \frac{g_1 * BW * Z_0}{\omega_c^2} \tag{6}$$

$$C_2 = \frac{BW}{g_2 * \omega_c^2 * Z_0} \tag{7}$$

$$L_3 = \frac{g_3 * BW * Z_0}{\omega_c^2}. \tag{8}$$

From (9), the shunt inductance L_1 is inversely proportional to $1/\omega_c^2$, but directly proportional to the target BW. Thus, for a given center-frequency, the L_1 operates closer to its SRF as the BW increases; further necessitating techniques to reduce the value and area, which to first order increases the SRF of any inductor used in a wideband amplifier.

In summary, at millimeter-wave frequencies, the SRF of the inductors $L_{1,2,3}$ ultimately limits the achievable ω_c and the BW for a BPDA implementation. The next section proposes Norton transformation techniques to address the aforementioned limitations by substantially reducing the value of the series inductances used in BPDAs.

III. NORTON TRANSFORMATION

A Norton transform (NT) [21], [22], illustrated in Fig. 2(a), replaces a reactive element, such as an inductor L, with an equivalent circuit using components $L/(1-N)$, L/N, $L/\{N(N-1)\}$ and a transformer with a turns ratio of $1{:}N$.

A. An Electrical Equivalence of Norton Transforms

A proof of electrical equivalence between the two circuits in Fig. 2(a) can be obtained by using any set of two-port parameters such as an impedance [Z], or admittance matrix [Y]. For the nominal case of a series floating inductor, the Y-parameters are given by

$$Y_A = \frac{1}{j\omega L}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}. \tag{9}$$

For the NT equivalent circuit (shown on the right of Fig. 2(a)), the two-port Y-parameters y_{11B} and y_{21B} are calculated with port-2 shorted to ground. Therefore, the simplified model in Fig. 2(b) can be used. Similarly, for calculating y_{12B} and y_{22B}, the NT circuit reduces to the form shown in Fig. 2(c).

In Fig. 2(b), with port-2 shorted to ground, the inductor $L/[N(1-N)]$ is effectively shorted. Therefore, the input impedance of port-1 is described by

$$\frac{V_1}{I_1} = j\omega\frac{L}{N} \| j\omega\frac{L}{1-N} = j\omega L \tag{10}$$

$$\Rightarrow y_{11B} = \frac{1}{j\omega L}. \tag{11}$$

From Fig. 2(b), and (9), the short-circuit transconductance is

$$I_2 = -\frac{1}{N}I_x = -\frac{1}{N}\left\{\frac{L/1-N}{L/1-N+L/N}I_1\right\}$$

$$= -\frac{1}{N}N\frac{V_1}{j\omega L} = -\frac{V_1}{j\omega L} \tag{12}$$

$$\Rightarrow y_{12B} = -\frac{1}{j\omega L}. \tag{13}$$

In a similar fashion, y_{12B} and y_{22B} can be derived from the simplified circuit in Fig. 2(c). In this case, port-1 is shorted to ground, thus effectively eliminating the shunt-inductor $L/(1-N)$ from the circuit.

$$I_1 = -\left\{\frac{L/N(1-N)}{L/N(1-N)+L/N}\right\}NI_2 = N^2I_2 \tag{14}$$

$$y_{21B} = -\frac{1}{j\omega L}. \tag{15}$$

Similarly,

$$y_{22B} = +\frac{1}{j\omega L}. \tag{16}$$

Finally, from (10)–(15), the y-parameters of the transformed circuit are

$$Y_B = \frac{1}{j\omega L}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} = Y_A. \tag{17}$$

Equation (16) has been derived assuming X is an inductor; however, NTs can be applied to capacitors as well.

For the case of NTs applied to replace a single floating inductor, the resulting inductors decrease in value with an increase in the transformer turns ratio N. However, it is important to note that for N $>$ 1, the component $L/(1-N)$ is negative. Also, at first glance, the number of components (additional inductors and a transformer) increases when applying a Norton transform to replace a single inductor, posing a further challenge with respect to integrating the DA. However, although the number of inductors increases using NT, the total value of inductance decreases substantially, as compared to a single floating inductor. An example of applying NT to reduce component values was reported in [23], where the matching network of a CMOS power amplifier was realized with a combination of capacitor- and inductor-based NTs to lower the aggregate component values. For the BPDA reported in this work, inductor-only, dual mirror-symmetric Norton transforms were applied with the explicit goal of scaling down the size of the inductors to facilitate the integration of the entire DA in silicon.

B. Dual Mirror Symmetric Norton Transform Applied to BPDA

The BPDA consists of two band-pass filters of the form shown in Fig. 3(a). For a wideband BPDA design, the series floating inductor L_2 is typically the inductor requiring the largest value and occupying the most silicon area. Therefore, reducing the value of this component is of primary concern. If an NT is applied on L_2, the procedure to reduce the total value of inductance in a BPDA is outlined below:

- Step 1) Inductor L_2 is split into two equal-valued series inductors and placed symmetrically about capacitance C_2, as shown in Fig. 3(b). Each $L_2/2$ inductor is further split into two inductances, L_1 and $L_x = L_2/2 - L_1$. Note, this technique can only be employed when the $L_2/2 > L_1$, which typically holds for high fractional-bandwidth BPDAs.
- Step 2) Apply NT with $N = 2$ on each of the series inductors labeled L_1 in Fig. 3(b). The transformation results in a net negative inductance, $-L_1$, in parallel with the shunt inductor L_1. Note that $L_1 // -L_1$ is an open circuit, effectively eliminating both inductors. The band-pass filter, after applying NTs, is shown in Fig. 3(c). Next, the two residual 1:2 transformers labeled T_1 and T_2, are exploited to further reduce the inductor values.
- Step 3) From Step 1, there are three components (one capacitor C_2 and two inductors L_x) in the series signal path. As shown in Fig. 3(d), these components are reflected across the windings of transformer T_2. The transformer has a turns-ratio 1:2, therefore, the impedance scales up by a factor of N^2. The value of inductor L_x scales down by 4, and capacitor C_2 scales up by 4.
- Step 4) The transformers T_1 and T_2, produced by the mirror-symmetric NTs, now appear in cascade. Both transformers have the same turns ratio of $1:N$ and $N:1$, respectively, which effectively neutralizes them. Stated differently, both transformers can be eliminated from the circuit, without impact on the frequency response, further reducing the net component value and required silicon area.

In summary, after the two Norton transformations are applied, inductor L_2, in the canonical form of the band-pass filter, is reduced to two series inductances of value $\{(L_2/2) - L_1\}/N^2$. The shunt-inductor inductor L_1 is split into two equal halves

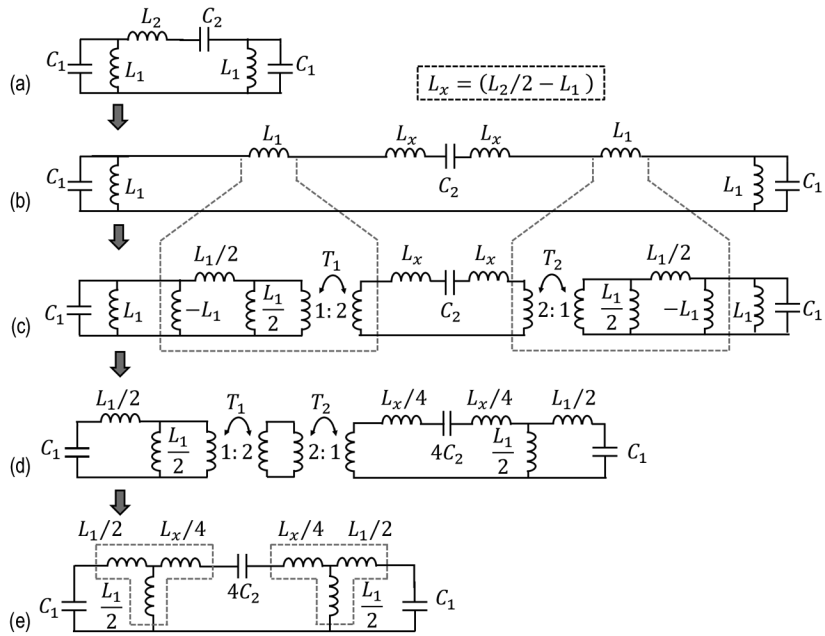

Fig. 3. Derivation of the compact-area bandpass filter starting with the canonical bandpass filter (top figure) through the application of mirror-symmetric dual Norton transforms.

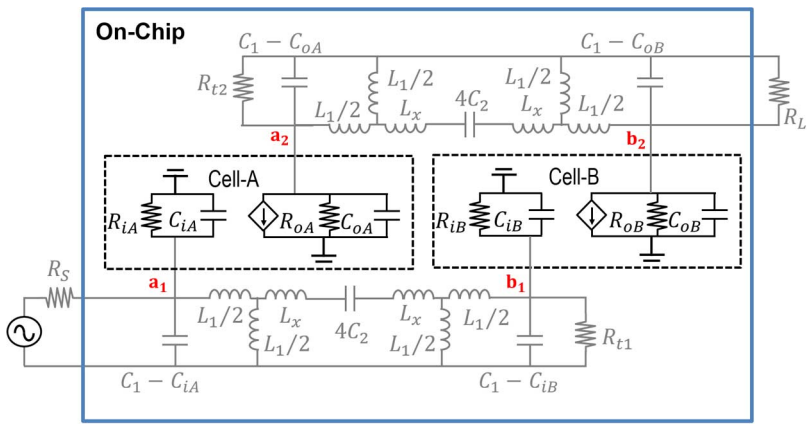

Fig. 4. Circuit diagram of the band-pass DA with representation of the input and output impedances associated with each gain-cell.

TABLE II
COMPONENT VALUES OF THE CANONICAL BPDA BEFORE AND AFTER THE NORTON REDUCTION TECHNIQUE IS APPLIED. NOTE: FOR THIS IMPLEMENTATION THE VALUE OF L_2 IS REDUCED BY ~86%

Canonical		Norton Reduced	
L_1	180pH	$L_1/2$	90pH
		$L_1/2$	90pH
L_2	800pH	$L_x/4$	55pH
		$L_x/4$	55pH
L_3	180pH	$L_1/2$	90pH
		$L_1/2$	90pH
C_1	175fF	C_1	175fF
C_2	45fF	$4C_2$	180fF
C_1	175fF	C_1	175fF

along the series and shunt signal paths. Table II shows component values before and after the NT reduction technique is applied.

IV. IMPLEMENTATION

The preceding discussion assumes the BPDA gain-cells present a purely capacitive load on the LC band-pass filter. However, the input impedance of the gain-cells implemented using a MOS or BJT transistor has a resistive component as well. Fig. 4 shows a simplified model of a BPDA with the input and output resistances of the gain-cells highlighted. Gain-cell A has an input impedance $R_{iA}||C_{iA}$, and an output impedance $R_{oA}||C_{oA}$. Similarly, gain-cell B has an input impedance $R_{iB}||C_{iB}$, and an output impedance $R_{oB}||C_{oB}$. The input capacitors (C_{iA}, C_{iB}) and output capacitors (C_{iA}, C_{iB}) load the input and output band-pass filters, respectively. Therefore, these capacitance values must be lower than the upper-limit specified by (2) and (4).

The input and output BPF are two doubly-terminated LC filters. The output capacitance (C_{DB} or drain-to-bulk capacitance) of the gain-cells is smaller than the input capacitance (C_{GS} or gate-to-source capacitance). Therefore, to ensure identical BPF at the input and output, extra capacitive loading was added at the

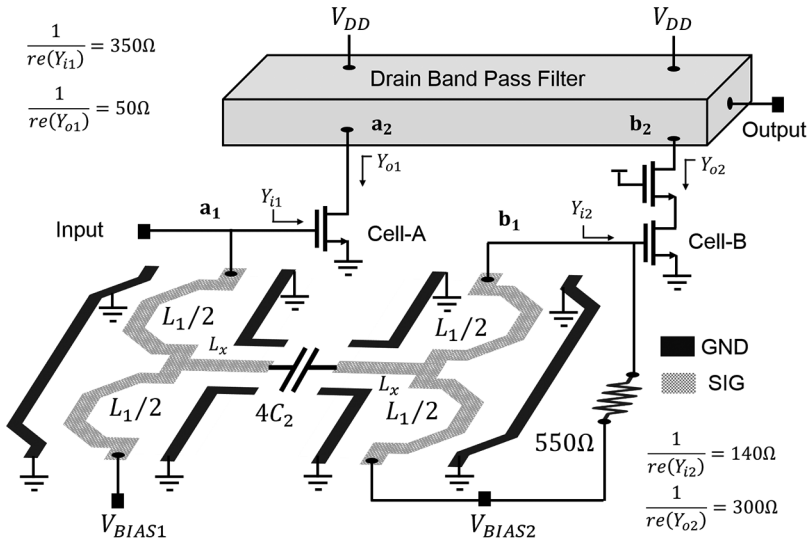

Fig. 5. Circuit diagram of the BPDA.

output. To allow characterization of the chip in a 50 Ω measurement setup, the termination resistances for the LC filters have been set at 50 Ω. Out of the four termination resistances, two are on-chip ($\mathrm{R_S}$ and $\mathrm{R_L}$) and two are off-chip ($\mathrm{R_{t1}}$ and $\mathrm{R_{t2}}$). Maintaining the termination resistances becomes imperative to preserve the filter frequency response in the presence of loading by measurement equipment and the gain-cells.

As shown in Fig. 4, the input resistance of cell-B $(\mathrm{R_{iB}})$ is in shunt with $\mathrm{R_{t1}}$ (the termination resistance on the input BPF). Therefore, instead of placing a 50 Ω termination resistance, matching can be provided by the input impedance of the gain-cell B, or the termination resistance can be selected such that $\mathrm{R_{t1}} \| \mathrm{R_{iB}} = 50\,\Omega$. Similar to $\mathrm{R_{iB}}$, the output resistance of the cell-A $(\mathrm{R_{oA}})$ is in parallel with the output termination resistance. Therefore, cell-A can be sized to have a low-output impedance.

In contrast to the on-chip termination resistances, the off-chip resistances—the source resistance, $\mathrm{R_S}$, and load resistance, $\mathrm{R_L}$—are fixed. Therefore, the loading effects from the input-impedance of cell-A $(\mathrm{R_{iA}})$, and the output-impedance of cell-B $(\mathrm{R_{iB}})$, need to be minimized.

In summary, the output impedance of cell-A and cell-B should be low and high, respectively. This suggests that cell-A could be a common-source device, whereas cell-B should be a cascode. A common-source stage will have a $\mathrm{V_{DS}}$ (drain-to-source) voltage equal to the supply voltage. In advanced technology nodes, the inherent low device output impedance $(\mathrm{r_o})$ results in a drain current heavily dependent on the transistor $\mathrm{V_{DS}}$. The common-source transconductance stage cell-A for this design has a $\mathrm{V_{DS1}} = 1$ V, W = 64 μm, and length of 40 nm, yielding a $\mathrm{R_{iA}} = 350\,\Omega$ and $\mathrm{R_{oA}} = 50\,\Omega$. In contrast to cell-A, the cascode amplifier in cell-B has a two transistor stack; therefore, the transconductance stage does not see the entire 1 V supply. For cell-B to achieve the same transconductance as cell-A, the W of the transconductance device in cell-B must be larger than cell-A, resulting in a lower $\mathrm{R_{iB}}$. Fortunately, this reduction in $\mathrm{R_{iB}}$ can be compensated for by changing the on-chip input-filter termination impedance, as described previously. The cascode gain-cell B has a $\mathrm{R_{iB}} = 140\ \Omega$ and a high $\mathrm{R_{oB}} = 300\ \Omega$. Both cells consume a current of 17 mA from a 1 V supply.

The BPDA reported in this work consists of two doubly-terminated band-pass filters; each filter has a Butterworth-filter response. The circuit diagram of the implemented BPDA with an illustrated layout of inductors $L_1/2$ and $L_{\boldsymbol{x}}$ is shown in Fig. 5. For the sake of clarity, only the input (gate) BPF is shown explicitly in Fig. 5; the output (drain) BPF is identical in structure, and folded on the top portion (attached at nodes $\mathrm{a_2}$ and $\mathrm{b_2}$). Through the application of Norton transforms, the inductance values of $\mathrm{L_1} = 180$ pH and $\mathrm{L_2} = 800$ pH in the canonical structure are reduced to 90 pH, 90 pH, and 55 pH, respectively. The 800 pH series inductor becomes two inductances of 55 pH after applying the NT method. The band-pass section is now realized as two symmetric T-sections, highlighted in Fig. 3(e). Thus, although the Norton transform (NT) appears to increase the number of inductors in the circuit, the aggregate value of these inductors is significantly lower. In addition to the size advantage of this BPDA, it is noteworthy to mention the 55 pH inductor will have a higher SRF as compared to an 800 pH inductor, further ensuring a proper frequency response for wideband filters with a high center frequency.

Although reducing the BPDA inductance values to as low as 55 pH provides an area advantage, it makes the transfer function more sensitive to routing-dependent parasitic inductance and capacitance. To alleviate this concern, the scaled inductor $L_x/4$ is realized as a coplanar waveguide (CPW) and used as routing between two symmetric T-sections in the simplified BPDA structure, as shown in Fig. 5. The series and shunt inductors $L_1/2$ are implemented as half-turn spiral inductors to eliminate additional routing to the supply and bias pads. To account for stray parasitic capacitance and mutual magnetic-coupling, the three inductors in each T-section were modeled and simulated as a single, three-port passive structure.

V. Measurement Results

The die microphotograph of the prototype BPDA fabricated in a 40 nm CMOS process is shown in Fig. 6. The process consists of a 6-metal stack with one ultra-thick metal (UTM)

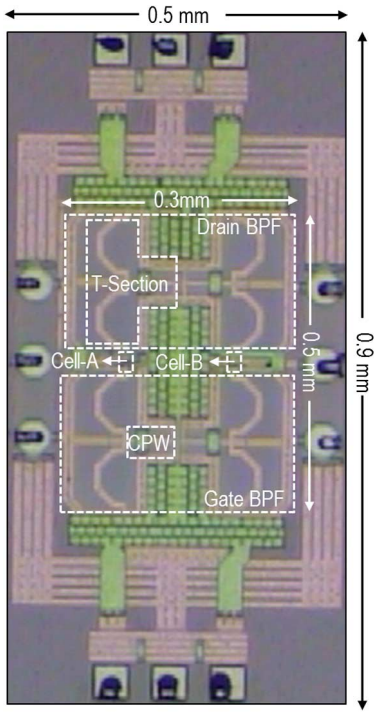

Fig. 6. Chip microphotograph for the BPDA.

and one aluminum passivation layer (AP). The compact DA core occupies an area of less than 0.5 mm $\times$ 0.3 mm. The chip was characterized using on-chip wafer probing. The DC-supply is brought on chip using a 3-pin DC-probe on the north-end of the die, and the gate bias voltages, through a DC-probe from the south-side. The millimeter-wave input and output are brought on-chip using GSG probes on the west and east-side, respectively.

Measurements were performed using Agilent's N5247A PNA-X. For accurate S-parameter measurements, a two-port SOLT calibration was done on the Impedance Standard Substrate (ISS). For linearity metrics, such as IIP3 and $P_{-1\mathrm{dB}}$, which require an accurate power measurement, power-calibration was performed up to the end of the probe-cable interface. The millimeter-wave input and output were provided through 67 GHz GSG Cascade infinity probes, and all the instruments were interconnected using 1.85 mm high-frequency co-axial cables. The measured S-parameters of the BPDA are plotted in Fig. 7. The S_{11} and S_{22} are less than 10 dB across a frequency range of 26.8–54 GHz, and 24.8–55 GHz, respectively. The peak-gain of the amplifier is 7 dB with a 3 dB pass-band from 24 GHz to 54 GHz, a BW of 30 GHz which results in an fBW of 77%. The total in-band gain-variation is less than 2 dB. The reported CMOS BPDA achieves a higher fBW, while occupying the lowest silicon area, in comparison to prior implementations realized in BiCMOS [3] and SiGe BiCMOS [9], [19] technologies.

The noise figure is characterized using the Y-factor method, with Agilent's 346CK01 noise-source and Agilent's N8975, a 26.5 GHz noise figure analyzer (NFA). A block diagram of the test setup is shown in Fig. 8. The output frequency of the BPDA, 26–56 GHz, lies outside the measurement range of the NFA.

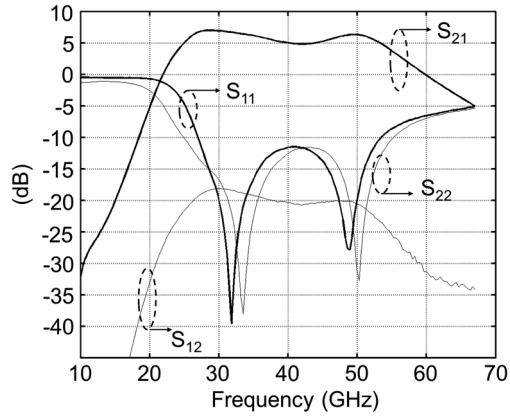

Fig. 7. BPDA measured S-parameters.

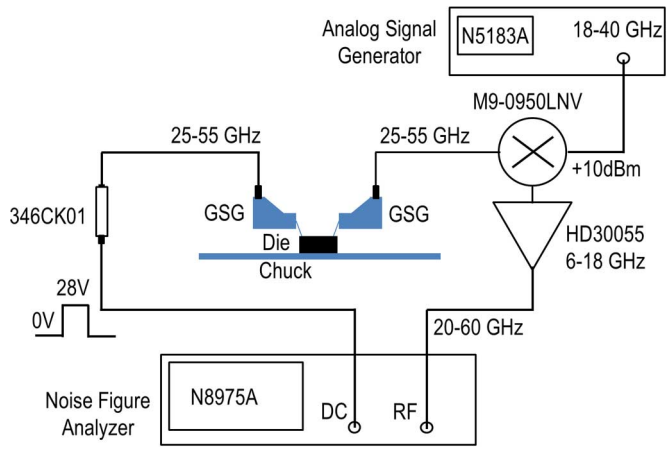

Fig. 8. Setup for BPDA noise characterization using the N8975A noise-figure analyzer.

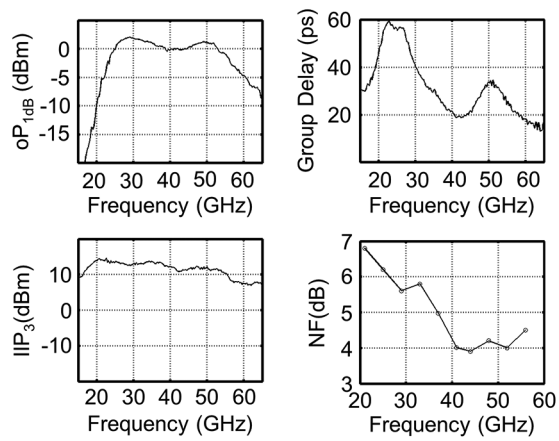

Fig. 9. Compression-point, group-delay, and IIP3 characterization versus frequency.

Therefore, an external down-conversion is required to bring the output noise of the NFA within the measurement band of the NFA. The output of the BPDA drives a M9-0950 wideband passive mixer. To compensate for the 10 dB in-band conversion loss of the mixer, the signal is amplified by 20 dB using a 6–18 GHz wideband low noise amplifier. The power at the output of the amplifier is measured by the NFA. The NF as a function of frequency is plotted in Fig. 9. The minimum NF is 3.9 dB and remains less than 6.2 dB over the frequency range from 24 to 54 GHz.

TABLE III
COMPARISON AND PERFORMANCE SUMMARY FOR THE BPDA

Parameters	[3]	[9]	[19]	This work
Technique	Coupled resonator	T-type matching	High-pass DA	Band-pass DA
Bandwidth (GHz)	23-32	47-77	21-42.5	24-54
ω_c (GHz)	9	30	31.75	39
fBW	33%	48%	67.7	77%
Gain (dB)	12 (voltage-gain)	22.5 (power gain)	8.3 (power-gain)	7 (power gain)
Power (mW)	13	52	28	34
NF (dB)	4.5 to 6.3	< 7.2	> 6.9	< 6.2
IIP3 (dBm)	-6.3 to -4.5	-x-	-x-	10 to 13
OP_{-1}(dBm)	-x-	4.5 (simulated)	0	-0.5 to 2
Area (mm^2) Pads not included	0.25	0.5	0.28	0.15
Technology	180nm BiCMOS	250nm BiCMOS	120nm SiGe-BiCMOS	40nm CMOS

To characterize the wideband linearity of the BPDA, the compression and intercept points were measured across frequency. The N5247A contains two internal signal-sources, thereby simplifying two-tone testing. The linearity measurement setup is identical to the one used for S-parameter measurement. The minimum and maximum in-band output 1 dB compression points are -0.5 dBm and 2 dBm, respectively. The minimum in-band IIP3 for a 100 MHz tone-spacing is 11 dBm. As shown in Fig. 9, the in-band group-delay varies between 20 ps and 55 ps over the frequency-range of interest. The performance of the BPDA is summarized in Table III.

VI. CONCLUSIONS

A compact band-pass distributed amplifier design technique was presented as an alternative to the more popular low-pass distributed amplifier for high frequency wideband signal amplification. The limitations of the canonical BPDA were discussed and a design methodology which enables practical integrated distributed amplifiers using dual mirror-symmetric Norton transformations which overcomes those limitations was described. In a 50 Ω input/output environment, the prototype test chip [24] achieved a peak-gain of 7 dB, an in-band ripple of 2 dB, and a 3 dB bandwidth of 30 GHz, while consuming a core area of 0.15 mm^2.

A plethora of evolving applications present numerous opportunities which would require ultra-wideband single-chip mm-wave systems. Potential applications for the BPDA described in this paper include automotive-radar systems (22–29 GHz), phase-array systems for satellite communication in the K_a (26.5 GHz) and Q-band (30–50 GHz), and potentially, components for 5th Generation (5G) standards. The 77% fBW CMOS BPDA presented in this work spans both the K_a and Q-bands, making the design techniques described in this paper suitable for a variety of high-frequency CMOS applications.

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