An Integrated CMOS Passive Self-Interference Mitigation Technique for FDD Radios

Tong Zhang, *Student Member, IEEE*, Apsara Ravish Suvarna, Venumadhav Bhagavatula, *Member, IEEE*, and Jacques Christophe Rudell, *Senior Member, IEEE*

***Abstract*—This paper presents an integrated passive self-interference mitigation (SIM) technique for FDD radios. A Four Port Canceller (FPC) serves a dual function as a receiver input matching network, and provides an auxiliary path from the transmitter (TX) to the receiver (RX) to perform leakage cancellation, with minimal penalty on the RX noise figure (NF), and power consumption. An example of this technique is applied to the design of a WCDMA front-end consisting of a low noise amplifier (LNA), the FPC, and an emulated power amplifier (PA) in a 40 nm, 6-metal-layer TSMC CMOS process. With proper tuning of the FPC and the use of an off-chip +30 dBm power amplifier, greater than 20 dB of TX leakage suppression is achieved over a cancellation bandwidth of 5 MHz.**

***Index Terms*—Fully passive, interference suppression, SAW-less transceivers, transmitter leakage, Wideband Code Division multiple access (WCDMA).**

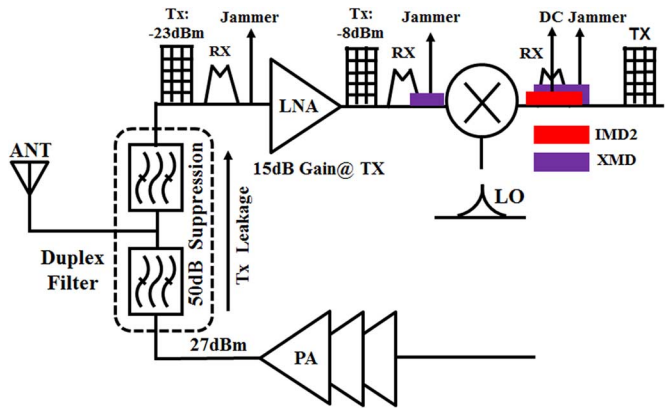


Fig. 1. Potential sources of RX interference form TX self-interference, in FDD radios.

I. Introduction

As INTEGRATED transceiver design enters the era of big data, the demand for both higher data rate and better utilization of existing spectrum becomes essential for future mobile applications. Frequency division duplexing (FDD) is one method of enhancing wireless network capacity by allowing a single user to simultaneously transmit and receive using different carrier frequencies. Typically, a discrete front-end duplex filter is used to prevent the transmitted signal from appearing ("leaking") at the RX input. However, these filters provide at most, 50 dB of isolation between the TX and RX. Thus, for applications requiring a high output power transmitter, such as cellular radios, a high performance receiver is necessary, which incurs a power consumption penalty.

For the purposes of illustration, a well-known wireless standard, WCDMA, is used to describe some of the challenges associated with FDD transceivers; see Fig. 1. The worst-case self-interference scenario for an FDD system occurs when transmitting at maximum output power; for WCDMA, this is +27 dBm. Assuming the duplex filter suppresses the transmitted signal by 50 dB, a −23 dBm TX leakage signal will appear at the LNA input. Further assuming the LNA provides 15 dB of gain at the TX frequency, the leakage signal becomes −8 dBm. This places a high linearity burden, mainly IIP2, on the subsequent components following the LNA (usually a mixer). In this example, a mixer IIP2 >45 dBm is necessary [1], [2] to ensure a sufficiently low-level of mixer intermodulation distortion. In addition, when a strong jammer appears in the vicinity of the RX band, the TX leakage signal will potentially cross-modulate as it passes through the nonlinearities in the LNA. Another mode of interference in the RX band arises from the transmit self-interference reciprocal mixing with the phase noise of the RX oscillator, lowering the carrier-to-interference (C/I) ratio at the output of the RX mixers. Other forms of interference attributed to TX self-interference relate to the effect of a large transmit carrier leaking into the receiver, and modulating the transconductance of individual devices in the RX signal path. This potentially up-converts low-frequency noise (including 1/f noise) from the bias circuitry into the band of interest, which has the effect of raising the noise floor in the RX signal path and further degrading the C/I ratio. Also, the presence of a large TX blocker will cause gain compression in the RX path. All of these effects act in concert to degrade the RX C/I ratio, thus, signifying the importance of mitigating, or cancelling, the TX self-interference as early as possible, in the RX chain; ideally cancellation would happen at the RX input.

The challenges associated with TX leakage signals in FDD systems are exacerbated by future applications such as 5th generation wireless standards, cognitive, and software-defined radios where the duplex band would ideally be kept to a minimum,

Manuscript received September 18, 2014; revised December 13, 2014 and February 10, 2015; accepted February 12, 2015. Date of publication March 26, 2015; date of current version April 30, 2015. This paper was approved by Guest Editor Ranjit Gharpurey. This work was supported by grants from Qualcomm, Google Inc., and CDADIC.

T. Zhang, A. R. Suvarna, and V. Bhagavatula are with Department of Electrical Engineering, University of Washington, Seattle, WA 98195 USA (e-mail: togzhang@uw.edu; apsara@uw.edu; bvenu@uw.edu).

J. C. Rudell is with the Department of Electrical Engineering and Computer Science, University of Washington, Seattle, WA 98195 USA (e-mail: jcrudell@uw.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2015.2408324

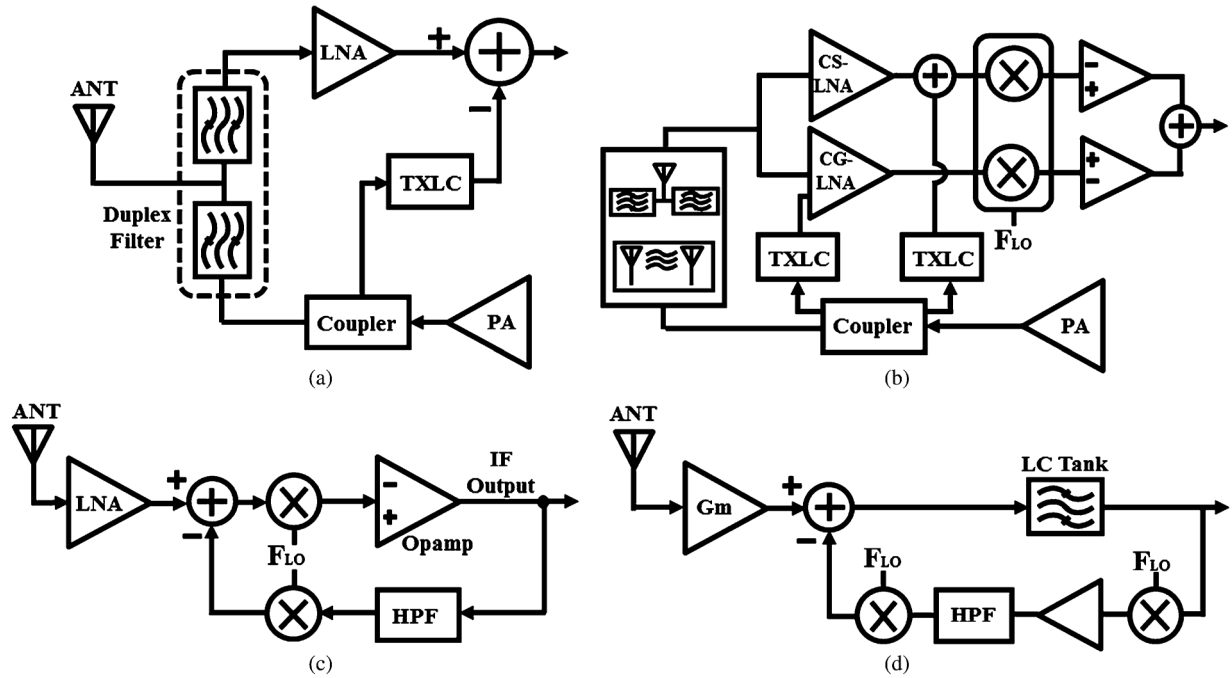


Fig. 2. Active TX leakage suppression using. (a) feed-forward (FF) techniques, (b) a two-point FF technique with cancellation at both the LNA input & output, (c) feedback (FB) loop incorporates the RX down-converter, (d) a separate feedback loop between the LNA and the RX down-converter.

to improve spectral efficiency. To address these interference issues, commercial FDD transceivers [3], [4] often use an off-chip surface acoustic wave (SAW) filter between the LNA and down-converter to further suppress the TX leakage, reducing the possibility of second order intermodulation distortion in the mixer. However, these band-specific discrete SAW filters [5], [6] prohibit highly programmable broadband transceiver solutions and require an increase in the radio cost and power consumption. Recent efforts have focused on improving RX selectivity in the presence of a self-interfering TX, without the use of off-chip filters [1], [2], [7]–[10]. Some have taken the concept of improving spectral efficiency to the extreme by simultaneously transmitting and receiving, using the same carrier frequency for both the RX and TX [11]–[13]; this is often referred to as a full-duplex system. However, depending on the commercial application, up to a 120 dB (cellular) TX carrier suppression would be required to share the transmit and receive spectrum.

This work seeks to realize a self-interference cancellation function for an existing wireless standard, WCDMA, with an eye toward eventually performing in excess of a 120 dB cancellation for use in a full duplex system. This paper is organized as follows, Section II describes the relevant state-of-the-art integrated self-interference cancellation systems and briefly introduces the proposed SIM concept. A detailed description of a passive four port canceller (FPC) is given in Section III. Section IV presents the circuit implementation details of a WCDMA front-end implemented in a 40 nm TSMC process, while measurement results of the prototype SIM are provided in Section V. Lastly, a few concluding comments are given in Section VI.

II. State-of-the-Art: Self-Interference Cancellation Techniques

Numerous recent efforts have explored methods to attenuate TX leakage signals in the RX signal path. These efforts have

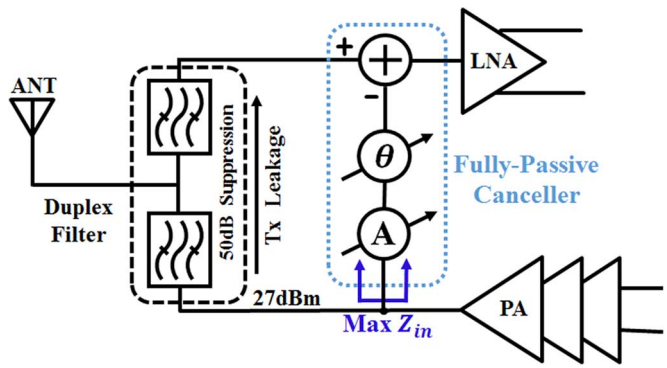


Fig. 3. High-level architecture of the proposed self-interference mitigation (SIM) system.

mainly focused on eliminating the need for the front-end RF SAW filter and can be categorized as either attempting to perform cancellation or filtering of the TX signal, with the use of active circuits. Feed-forward cancellers [2], [8], shown in Fig. 2(a) and (b), sample the TX output and inject an amplitude-adjusted and phase-rotated signal into the RX signal path. A set of alternate architectures [16], [17] proposes using a feedback loop by effectively creating an RF channel-select bandpass filter; see Fig. 2(c) and (d). Other TX leakage suppression techniques include integrated filtering methods using a high-Q passive filter with bond wires [9], an active bandpass sink filter [1], [18], a LMS adaptive filter [19], and a notch filter created by a frequency translational high pass filter [20], [21].

Other options for TX leakage suppression include techniques detailed in [10]–[13], [22], [23]. An integrated duplexer [10], [23], antenna cancellation [11], active balun cancellation [12] and a mixer-first full-duplex LNA [22] could potentially be applied to cancelling or filtering the TX self-interference.

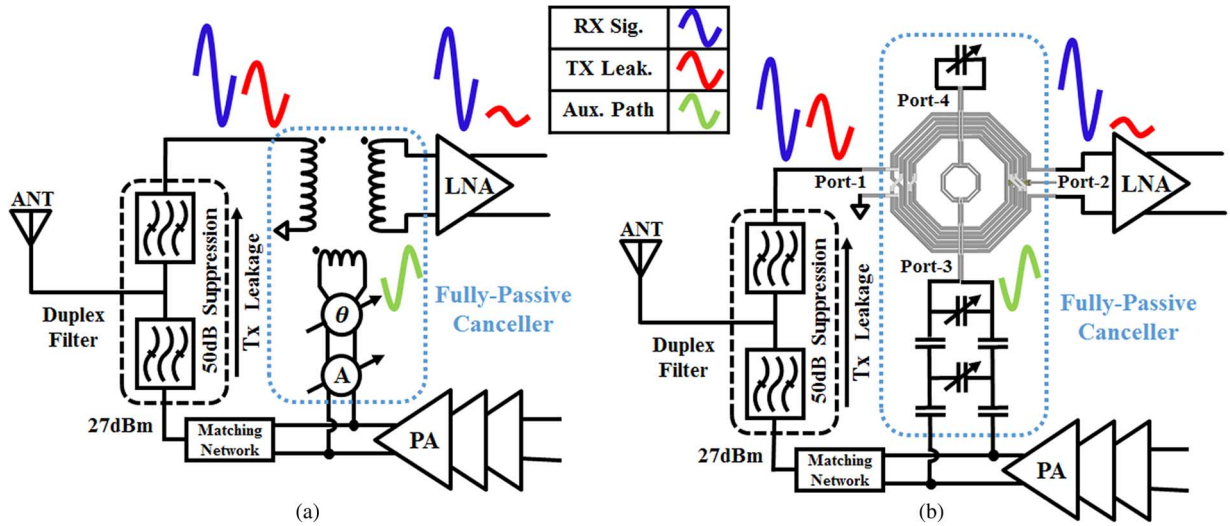


Fig. 4. The proposed transformer-based TX leakage canceller. (a) The SIM block with a proposed canceller in schematic, (b) A hybrid circuit schematic and layout of the SIM block.

A passive filter uses bond wires to perform leakage suppression [9]; however, the amount of suppression depends on the order of the filter which trades off with pass-band insertion loss. Most of the other aforementioned methods utilize an active cancellation path, which is problematic from a noise, linearity, and power perspective. An ideal integrated TX leakage canceller would possess the following characteristics:

- Introduce minimal RX noise and additional power, while occupying minimal silicon area.
- Perform cancellation as close to the RX input as possible to relax the required performance of subsequent blocks.
- Present negligible loading (high impedance) to the TX/PA output, which minimizes any power loss and efficiency degradation.
- Minimal sensitivity to packaging and EMI effects.

The remainder of this paper explores a TX leakage cancellation method which attempts to embody all of these characteristics. This is followed by an expanded description of the proposed prototype cancellation chip first given in [24].

III. Proposed Passive Self-Interference Mitigation (SIM) Technique

This section provides an architectural-level description of the proposed passive SIM technique, followed by a detailed analysis of the proposed four-port canceller (FPC). Later, this SIM approach is compared with recently published work on integrated duplex filters [10], [23].

A. Proposed Self-Interference Mitigation (SIM) System

The placement of the proposed feed-forward SIM device, relative to both the TX and RX is shown in Fig. 3. This system assumes the use of a discrete front-end duplex filter, and as such, the objective of the canceller is to significantly attenuate the leakage signal at the filter output. For this implementation, the canceller network, realized with a four-port canceller (FPC), is introduced between the TX output and RX input, thus routing the TX output signal in a parallel path to an on-board FBAR duplex filter. However, by injecting a TX cancellation signal early in the RX chain, extreme caution is necessary to minimize any noise or nonlinearities that might be injected. Therefore, minimizing the use of active components in the cancellation path is critical to reduce the possibility of injecting unwanted noise. An equally important feature of the canceller is to present a high-load impedance at the TX output.

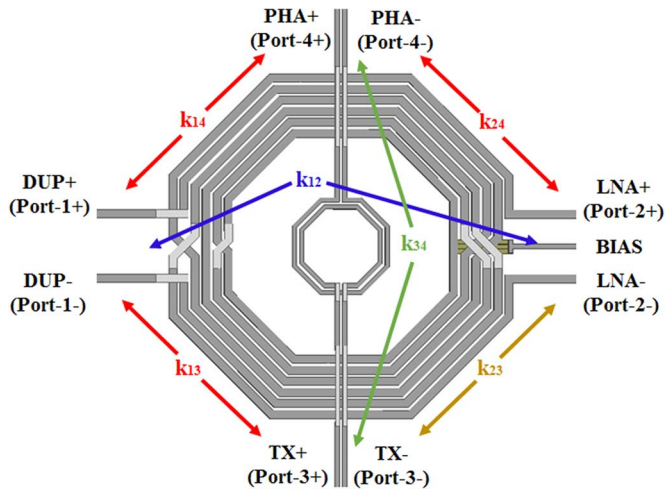


Fig. 5. Various coupling coefficients in four-port canceller (FPC).

The approach taken in this work utilizes components from a transformer-based RX matching network to inject the cancellation signal. Transformers have the added advantage of easily coupling in several signals through the use of additional primaries. A conceptual diagram of the proposed transformer-based TX leakage canceller is shown in Fig. 4. Integrated transceivers often use differential signal paths to increase the immunity to unwanted common-mode noise from the substrate and power supplies [25], [26]. However, commercial antennas supply a single-ended input to the receiver, thus a single-to-differential conversion is necessary between the antenna and receiver interface. A balun serves a dual purpose of performing a single-ended to differential conversion, and impedance matching at the RX input [27], [28]. The proposed canceller exploits the existing

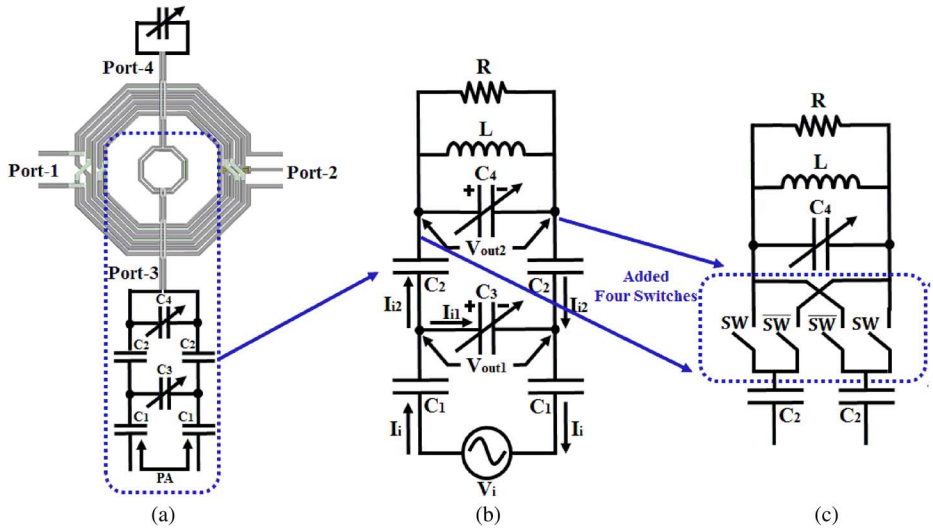


Fig. 6. Simplified circuit model describing the TX-PA cancellation path. (a) The full canceller path between the TX and RX, (b) model of TX-PA cancellation path, (c) added four switches in the cancellation path to expand the phase tuning range.

transformer topology to inject a component of the cancellation signal. A second, relatively small primary is added to the center of the transformer to couple a component of the TX signal into the receiver signal path, see Fig. 4(a). As such, the canceller becomes a component of the RX matching network with minimal additional area. The signal received on the main primary attached to the RX input (antenna side shown as port-1) travels from port-1 to port-2 with the TX leakage signal; this is shown as a hybrid schematic and layout in Fig. 4(b). The TX signal from the canceller network is intentionally coupled into the RX with 180° phase shift, through the use of a significantly smaller primary, shown as port-3. Since the discrete duplexer has a rejection of approximately 50 dB at the TX frequency, any practical cancellation technique must accurately adjust to match the amplitude and have the opposite phase of the attenuated leakage signal. This is done with two techniques: First, port-3 and port-4 are weakly coupled with port-1 and port-2. Second, the amplitude of the coupled-TX-signal is precisely controlled by the capacitor values in the cancellation path, while the phase is modified by varying the termination reactance on port-3 and port-4 of the transformer.

B. FPC Analysis

The different coupling coefficients inside the FPC are shown in Fig. 5. To minimize both the RX noise figure and signal path attenuation the transformer magnetic coupling coefficient, k_{12}, should be maximized between the primary on the antenna side (port-1), and the secondary on the receiver/LNA side (port-2). The coupling between port-2 and port-3 is optimized to match the TX leakage signal strength coming into the receiver (port-1). Because a duplex filter is used and the leakage signal is weak at the RX input, the coupling coefficient for the leakage path, k_{23}, is kept low. This is accomplished by making the primary at port-3 small, with a single turn. The phase of the coupled-TX-signal is adjusted by varying the termination reactance at port-4, which has the effect of modulating the phase of the signal coupled between port-3 and port-4; this effectively rotates the phase of the cancellation signal. All other modes of coupling are minimized to reduce the impact on the LNA matching network, particularly when modulating the phase by tuning a capacitor array on port-4.

As discussed in the previous section, an ideal integrated canceller should present a high input impedance (PA-side) to mitigate any loading effects on the TX output. Accordingly, accurate characterization of the canceller input impedance is important. A derivation of the input impedance from the perspective of the transmitter can be obtained by analyzing the schematic in Fig. 6. Applying Kirchoff's current and voltage laws to the circuit in Fig. 6(b) yields

$$\mathrm{I_i} = \mathrm{I_{i1}} + \mathrm{I_{i2}} \tag{1}$$

$$\mathrm{V_{out1}} = \mathrm{V_{out2}} + \frac{2}{\mathrm{sC_2}}\mathrm{I_{i2}} \tag{2}$$

$$\mathrm{V_{out2}} = \mathrm{I_{i2}} \cdot \mathrm{Z} \tag{3}$$

$$\mathrm{V_{out1}} = \mathrm{I_{i1}} \cdot \frac{1}{\mathrm{sC_3}} \tag{4}$$

$$\mathrm{V_i} = \mathrm{V_{out1}} + \mathrm{I_i}\frac{2}{\mathrm{sC_1}} \tag{5}$$

where $Z = R||sL||1/sC_4$.

Solving (1)–(5), the input admittance, $\mathrm{Y_{in}}$, is shown to be

$$\mathrm{Y_{in}} = \frac{\mathrm{I_i}}{\mathrm{V_i}} = \frac{\mathrm{s}\left(1 + 2\frac{\mathrm{C_3}}{\mathrm{C_2}}\right) + \mathrm{s_2C_3Z}}{2\left(\frac{1}{\mathrm{C_1}} + \frac{1}{\mathrm{C_2}} + 2 \cdot \frac{\mathrm{C_3}}{\mathrm{C_2}} \cdot \frac{1}{\mathrm{C_1}}\right) + \mathrm{sZ}\left(1 + 2\frac{\mathrm{C_3}}{\mathrm{C_1}}\right)}. \tag{6}$$

Assuming a front-end duplex filter is used, as in this implementation, the TX leakage signal is significantly attenuated at the RX input (50 dB attenuation). Thus, to match the TX leakage signal, the cancellation path must significantly attenuate the signal coming from the TX output. This implies the value of C_1 and C_2 are significantly lower than C_3, to achieve enough attenuation in the cancellation path. C_3 is realized as a switched-capacitor bank which facilitates a digitally assisted gain adjustment of the cancelling TX signal. A high attenuation

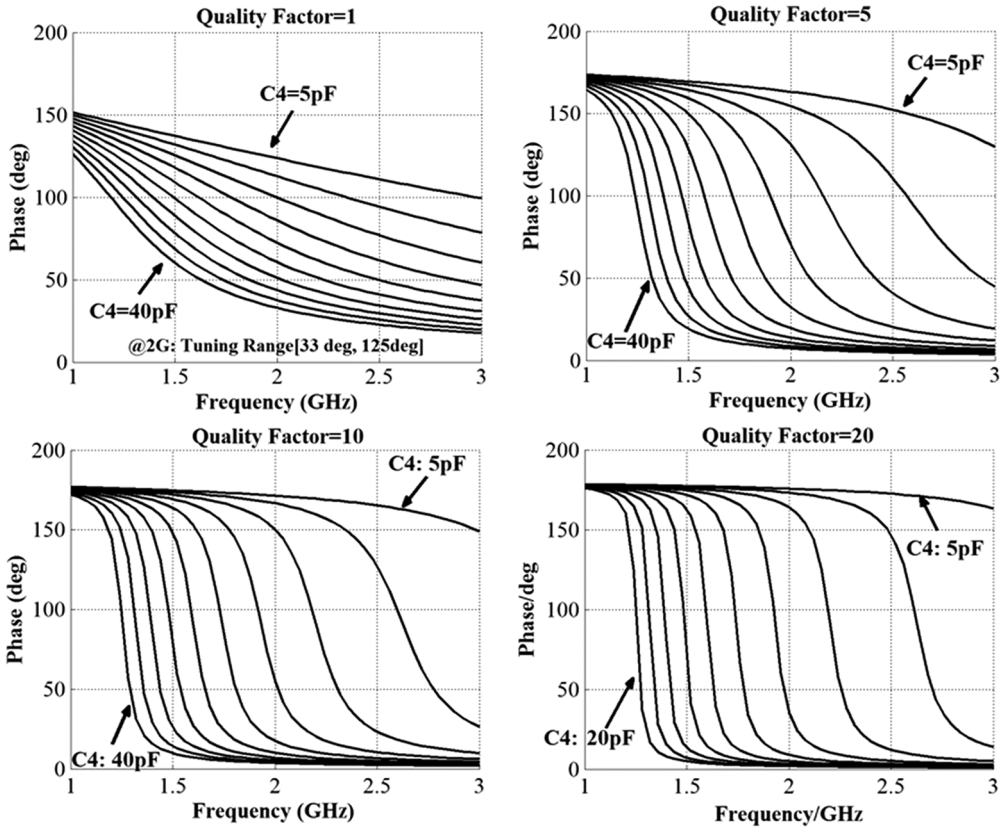


Fig. 7. Simulation results of phase tuning range as a function of C_4 and different values of Q.

in the cancellation path also helps to relax any reliability concerns on the switches associated with C_3; the canceller input from the PA output can be as high as 10 V.

Under the condition $C_1, C_2 \ll C_3$, the input admittance $Y_{\rm in}$ reduces to

$$\mathrm{Y_{in}} \approx \frac{\mathrm{s}\cdot 2\frac{\mathrm{C_3}}{\mathrm{C_2}} + \mathrm{s^2 C_3 Z}}{4\frac{\mathrm{C_3}}{\mathrm{C_1 C_2}} + \mathrm{sZ}\cdot\frac{2\mathrm{C_3}}{\mathrm{C_1}}} = \frac{\mathrm{s}\left(2\frac{\mathrm{C_3}}{\mathrm{C_2}} + \mathrm{sC_3 Z}\right)}{\frac{2}{\mathrm{C_1}}\left(2\frac{\mathrm{C_3}}{\mathrm{C_2}} + \mathrm{sC_3 Z}\right)} = \frac{\mathrm{C_1 s}}{2}. \quad (7)$$

From (7), the input impedance of the canceller, from the perspective of TX, looks mostly capacitive, and thus easily absorbed into the PA output matching network design. Because the loading from the TX side looks almost purely imaginary, the matching network can be made to resonate with the load presented by the canceller, and minimize any loss in the TX output power and efficiency.

The amplitude tuning is performed in the cancellation path, and an equally critical feature is the adjustment of phase. Usually the coupling coefficient from port-3 and port-2 is fixed by the physical dimensions of the primary and secondary coils. This approach utilizes two mechanisms to apply phase tuning, both through the capacitor divider in the cancellation path, and at the input of port-3 ($\mathrm{V_{out2}}$ in Fig. 6(b)). The derivation of the transfer function (TF) between $\mathrm{V_{out2}}$ and V_i (in Fig. 6(b)) begins by reusing (1)–(5) to obtain (8):

$$\frac{\mathrm{V_{out2}}}{\mathrm{V_i}} = \frac{1}{1 + \frac{\mathrm{C_3}}{\mathrm{C_1}} + \frac{2}{\mathrm{sZ}}\left(\frac{1}{\mathrm{C_1}} + \frac{1}{\mathrm{C_2}} + \frac{2\cdot\mathrm{C_3}}{\mathrm{C_1}\cdot\mathrm{C_2}}\right)}. \quad (8)$$

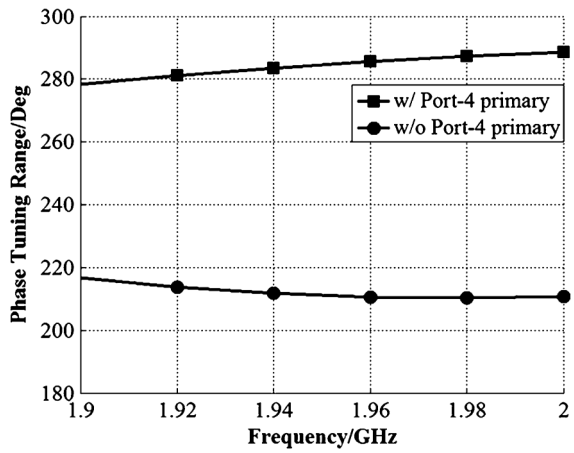


Fig. 8. Phase tuning range simulations w/ and w/o port-4 primary.

As discussed earlier, C_1 and C_2 are always designed with a lower value than C_3 and C_4, therefore, the transfer function in (8) simplifies to

$$\frac{\mathrm{V_{out2}}}{\mathrm{V_i}} \approx -\frac{\mathrm{C_1 C_2 w^2 L}}{4\mathrm{C_3}} \cdot \frac{1}{\frac{\mathrm{j}}{\mathrm{Q}} + (1 - \mathrm{w^2 C_4 L})} \quad (9)$$

where $\mathrm{Q} = \mathrm{R/wL}$.

Solving for the phase response of the transfer function,

$$\measuredangle\left(\frac{\mathrm{V_{out2}}}{\mathrm{V_i}}\right) = \pi - \mathrm{atan}\left(\frac{1}{\mathrm{Q}(1 - \mathrm{w^2 C_4 L})}\right). \quad (10)$$

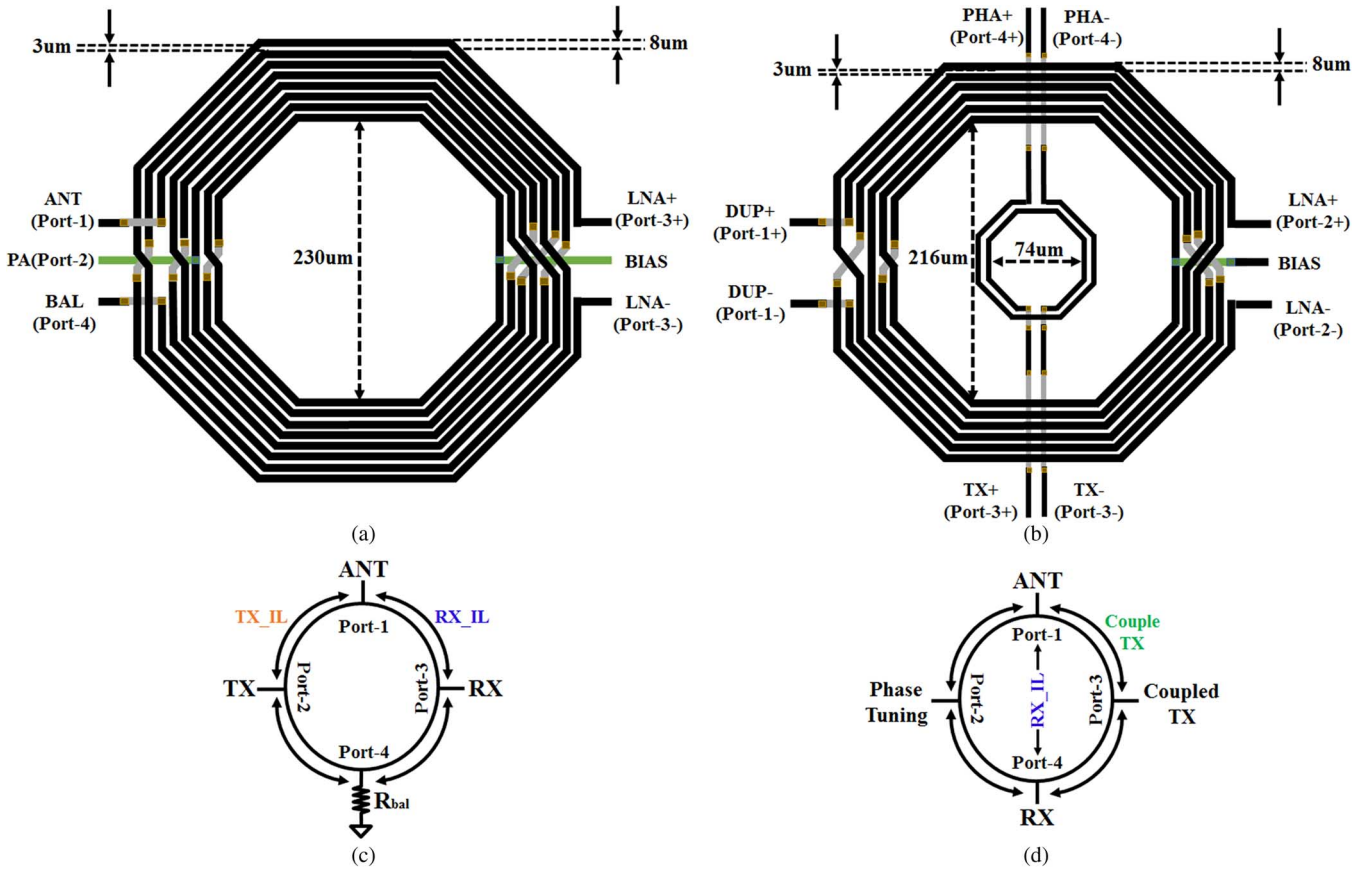


Fig. 9. Comparison between the proposed FPC and the integrated duplexer. (a) layout of the integrated duplexer, (b) layout of the FPC, (c) symbolic model of the integrated duplexer, (d) symbolic model of FPC.

From (10), one observes that the phase modulation of coupled-TX-signal in the FPC is controlled mainly by the tank Q and impedance at port-3.

Using (10), the phase tuning range can be expressed as

$$\text{Phase Tuning Range} = \pi - \text{atan}\left(\frac{1}{\text{Q}(1-\text{w}_0{}^2\text{C}_{4,\text{min}}\text{L})}\right) + \text{atan}\left(\frac{1}{\text{Q}(1-\text{w}_0{}^2\text{C}_{4,\text{max}}\text{L})}\right) \quad (11)$$

where $C_{4,min}$ and $C_{4,max}$ are the minimum and maximum value of the tuning capacitor, C_4.

Using arctangent subtraction formula, $\text{atanx} - \text{atany} = \text{atan}((\text{x}-\text{y})/(1+\text{xy}))$, (11) simplifies to

$$\text{Phase Tuning Range} = \pi + \text{atan}\left(\frac{Qw^2L(C_{4,max}-C_{4,min})}{1+Q^2(1-w^2C_{4,min}L)\cdot(1-w^2C_{4,max}L)}\right). \quad (12)$$

In the extreme case, where $w^2C_{4,min}L \ll 1$, $w^2C_{4,max}L \gg 1$ and $\text{Q} > 1$

$$\text{Phase Tuning Range} \approx \pi - \text{atan}\left(\frac{1}{Q}\right). \quad (13)$$

From (13), the phase tuning range can be seen to approach 180° when the Q is large (Q > 5). To further extend the phase tuning range, four switches are added in the cancellation path between C_2 and the tank R, L, and C_4 (see Fig. 6(c)). The additional switches effectively double the phase tuning range to 360° by flipping the polarity of the coupled-TX signal in the cancellation path.

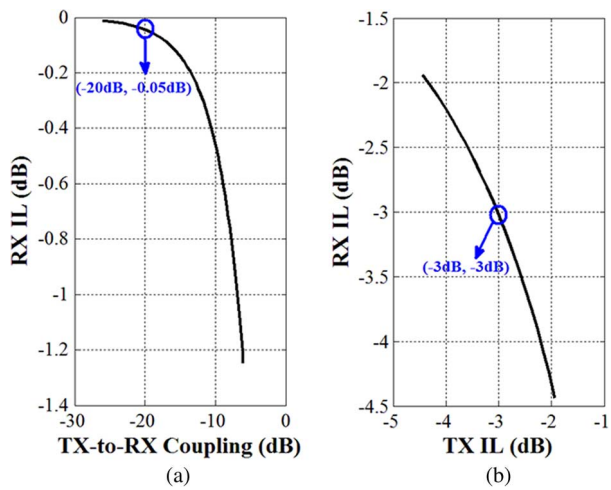


Fig. 10. Simulation results derived from the extracted layout given in Fig. 9, to illustrate the power division in the proposed FPC and integrated duplexer. (a) FPC. (b) Integrated duplexer.

The simulated phase tuning range for different values of C_4 (varied from 5 pF to 40 pF) and Q (from 1 to 20) are shown in Fig. 7. Using simulation results of the FPC from HFSS, a model of the inductance looking into port-3 was built, Fig. 6. The value of the capacitors were then selected to modulate the tank impedance which effectively tunes the phase

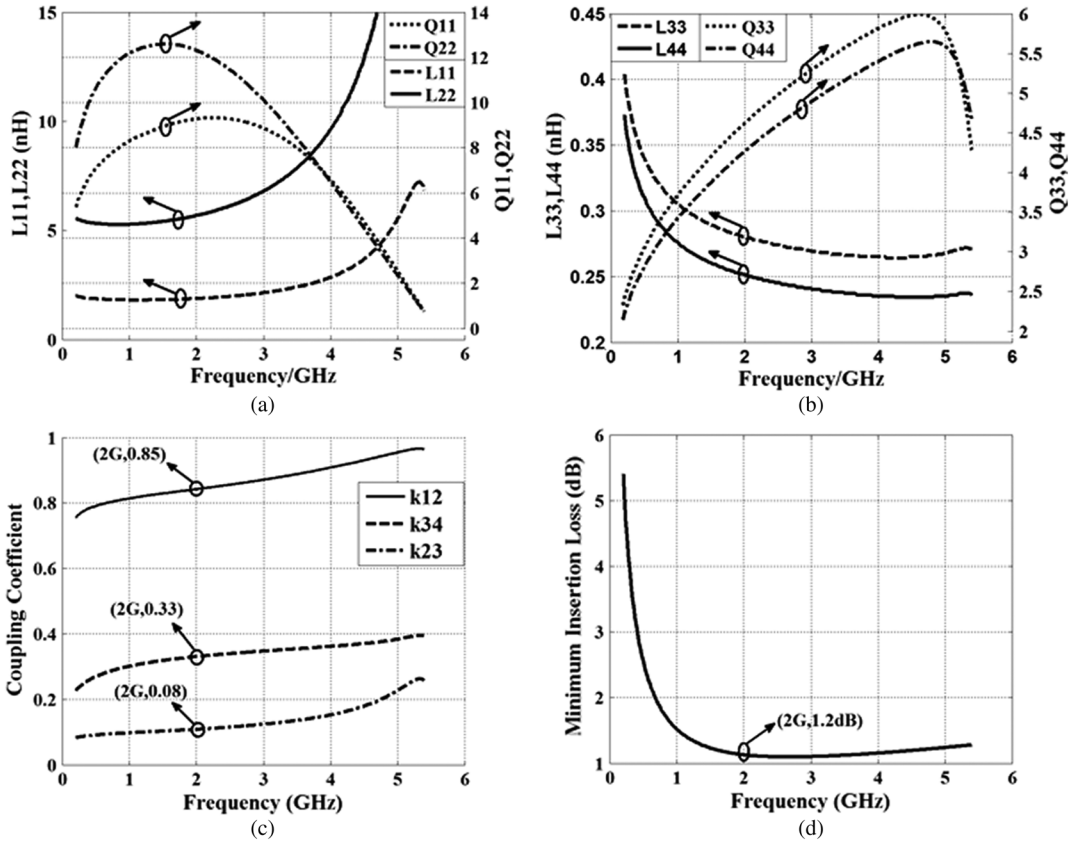


Fig. 11. FPC characteristics: (a) inductance and quality factor of the transformer primary and secondary windings, (b) inductance and quality factor of coupled-TX coil and phase-tuning coil, (c) port-one-to-port-two, port-three-to-port-four, and port-two-to-port-three coupling coefficients, (d) RX signal path FPC insertion loss.

in the cancellation path. From Fig. 7, one observes that as the tank Q increases, this has the effect of expanding the phase tuning range. However, the phase becomes a strong function of frequency for a given setting with a high-Q tank, which is undesirable for wideband applications. Conversely, for a low-Q tank, the total phase tuning range becomes narrower (see (13)), with the advantage that the phase has a lower dependence on frequency. Thus, a fundamental trade-off between the phase tuning range and the frequency dependence of the phase exists. For this design a Q of 5 was found to produce a sufficient tuning range for the canceller with a moderate dependence on frequency, Fig. 7.

The tank impedance is modulated by adjusting the value of C_4. The total tuning range of C_4 is limited by the parasitic capacitance in the capacitor tuning bank, thus limiting the range of tank impedances, which ultimately leads to an unacceptably small phase tuning. From (11), if the tank impedance tuning range can be made wider at port-3, this will increase the total phase tuning range of the canceller. Thus, alternative impedance modulation techniques were explored to augment the phase tuning using C_4.

To enhance the tank impedance tuning beyond what is achievable by modulating just C_4, an additional primary (shown as port 4; see Fig. 6(a)) was introduced in the FPC. The port-4 primary is tightly coupled (high coupling coefficient) to the port-3 primary, thus modulating the impedance at port-4 impacts the impedance looking into port-3. For this implementation, a varactor diode was attached to the port-4 primary. This has the effect of enhancing the impedance tuning range looking into port-3, thus increasing the phase tuning range. The varactor control voltage is generated by a 6 bit digital-to-analog converter (DAC). The addition of the port-4 primary can increase the canceller's phase tuning range by more than 30%. From extracted simulations, the canceller was found to have a phase tuning range of greater than 280 degrees by combining the two tuning techniques: modulating C_4 and through the addition of the port-4 primary with a varactor diode, see Fig. 8.

C. Comparison Between an FPC and an Integrated Duplexer

The FPC in schematic form appears similar to an integrated duplexer [10], [23]. Although the FPC and integrated duplexer appear quite similar, they are, in fact, functionally very different. The motivation of the FPC concept is to act as a canceller between the transmitter and receiver which augments the duplex filter, rather than replacing an off-chip SAW duplexer. The layout for both the integrated duplexer and FPC are shown in Fig. 9(a) and (b), where the differences between these two structures become apparent, particularly the primary which is attached to the PA output. From Fig. 9(a), the primary associated with the TX is matched in both the size, and the turns ratio, to the primary used in the RX signal path; this is essential to realize the function of the duplexer. Likewise, the impedance looking into both primaries is typically matched to 50 Ω. As such, the power from the PA is split by two, thus creating a fundamental 3 dB loss in both the RX and TX signal paths, and significantly degrading the PA efficiency [10]. In contrast, the

TABLE I
COMPARISON BETWEEN THE PROPOSED SIM TECHNIQUE AND IDEAL INTEGRATED CANCELLER

	Proposed SIM technique	Ideal integrated canceller
Additional power overhead	≈ 0mW	Minimal
Additional silicon area	≈ 0*	Minimal
NF Penalty	*<0.1dB or 1.2dB	Minimal
Cancellation location	RX input	RX input
Loading to TX-PA output	Minimal	Minimal
Capability of handling TX output power	>30dBm	As large as possible
LO-feedthrough, stability problems	No	No

*The single-ended to differential transformer (port-one and port-two) has an area of approximately 400 μm × 400 μm and an insertion loss of 1.2 dB. The added port-three (TX) and port-four (Phase) introduces no extra area and an additional loss of less than 0.1 dB.

FPC has a strong asymmetry between the transformer primaries in the RX and TX paths; see Fig. 9(b). The small single-turn primary in the TX cancellation path (port-3) with the capacitor network between the combiner and transmitter, realizes an impedance which is primarily capacitive and has a large real part, greater than 1.5 kΩ. Thus, there is not an inherent 3 dB loss at the PA output when using the FPC.

From a more analytical perspective (identical to [29], [30]) the three-port lossy reciprocal network is analyzed as a four-port lossless network where the port-4 termination is provided with a resistor to represent the loss, see Fig. 9(c). A perfectly matched and ideal TX-RX isolated four-port duplexer can be described by the following S-parameter matrix [29], [30]:

$$S = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & 0 & S_{24} \\ S_{13} & 0 & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix}. \quad (14)$$

Applying the condition of lossless network and minimizing the TX/RX insertion loss [29], [30]

$$|S_{12}|^2 + |S_{13}|^2 = 1. \quad (15)$$

A symbolic model of the FPC is shown in Fig. 9(d). After putting in matching, isolation and lossless conditions, one of the solutions to the matrix is the same as (15). A plot of the RX insertion loss (IL) as a function of TX IL for the integrated duplexer is shown in Fig. 10(b). The power applied at the antenna port is divided between RX and TX ports of the duplex filter. Therefore, if the power is split evenly between these two ports, both the TX and the RX signal paths have an equal insertion loss of 3 dB. However, in the FPC, a lower coupling coefficient is required between port-3 and port-1, thus the insertion loss is lower. Fig. 10(a) illustrates the power division inside the proposed FPC. If the coupled-TX-signal is 20 dB lower than the original signal, less than 0.1 dB RX insertion loss will be observed.

D. FPC Characteristics

Electromagnetic simulations using HFSS were performed on the FPC layout to extract the S-parameters [31] and verify the canceller performance. From Fig. 11, the primary and secondary windings demonstrate a strong coupling (k = 0.8–0.88) while maintaining a high quality factor (Q = 9–12) to minimize the insertion loss (IL ≈ 1.2 dB). The third and fourth windings show moderate coupling (k = 0.3–0.4) with an optimized quality factor (Q = 3–5). The coupling coefficients from port 1-to-3, port 1-to-4, and port 2-to-4 are made relatively weak (k < 0.1), and optimized to minimize the insertion loss and maximize the tuning range.

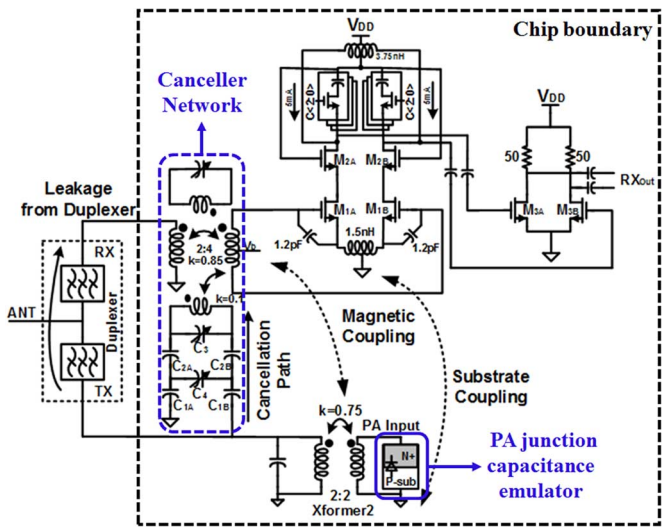


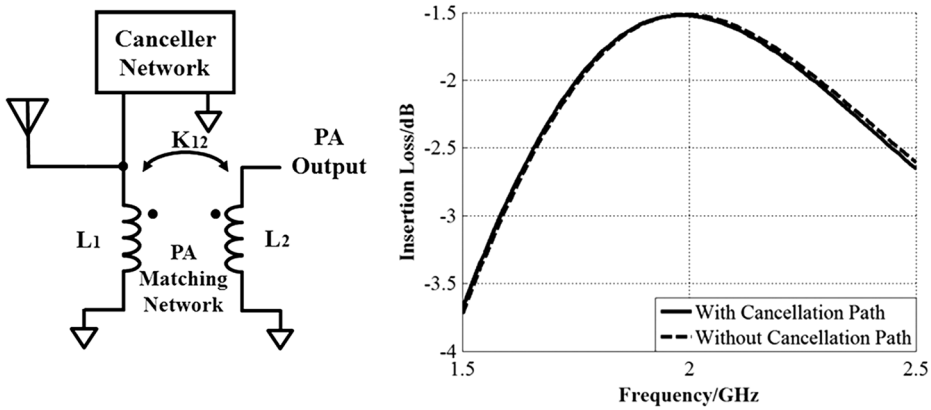
Fig. 12. CMOS WCDMA LNA with TX leakage suppression.

Table I is a brief summary of the proposed technique with a comparison to an ideal TX leakage canceller.

IV. PROTOTYPE CANCELLER CIRCUIT IMPLEMENTATION

A circuit diagram of the integrated WCDMA front-end with the TX leakage cancellation block is shown in Fig. 12. This chip includes the transmitter output matching network, the FPC, the LNA, and output test buffers. Although the PA was not integrated on this die, an array of devices to emulate a PA output stage was included.

The RX portion of the chip consists of a differential LNA and buffer. To achieve a good noise figure, the FPC provides some passive voltage gain (~6 dB) by setting the transformer turns ratio 2:4. A transmitted signal can be applied to the chip using



(a) (b)

Fig. 13. Simulated impact on PA loading with/without canceller network. (a) Schematic diagram; (b) extracted simulation results.

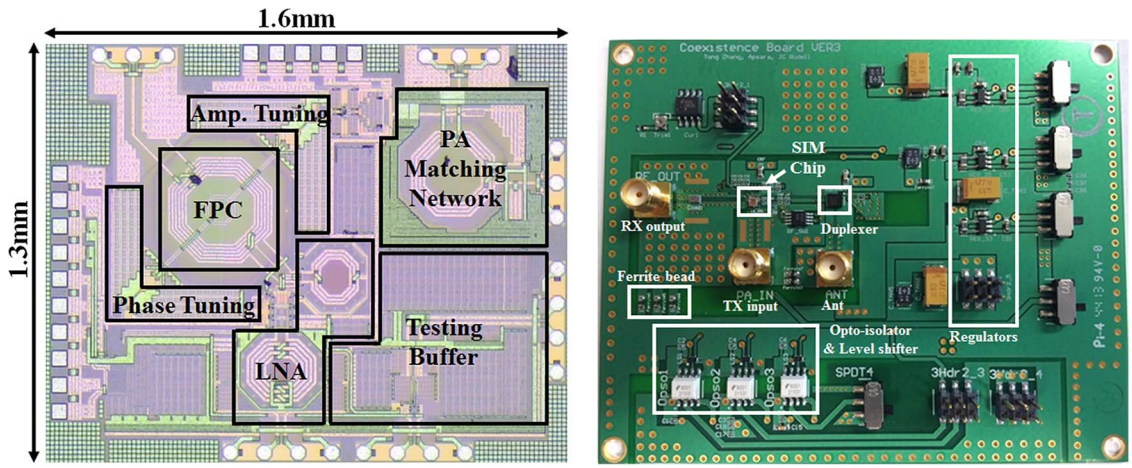


Fig. 14. (a) Microphotograph of 6-layer metal TSMC 40 nm CMOS die; (b) testboard photo; chip-on-board packaging used to attach SIM die.

either a discrete on-test-board PA, with a $P_{sat} = +30$ dBm, fed to the PA matching network, or a signal generator to emulate a TX signal. The matching network consists of a single-ended to single-ended transformer, designed to drive the 50 Ω load of the duplex filter. To replicate the effect of substrate coupling of an integrated PA (PA is not included on this chip), an nwell-to-psub diode was added in-parallel with the primary winding of the PA output matching network. The size of the diode was based on the total active region (NMOS device area: 22,400 μm^2) which was derived from [32]. The intention of adding these devices with an off-chip PA, was to capture the effect of drain-to-substrate coupling that might otherwise be present with an integrated power amplifier.

Extracted simulations were used to verify whether the canceller has minimal loading effects on the PA output. Simulation results show the effect of both loading the output of the PA with the FPC, and the unloaded case, see Fig. 13; the canceller adds a 0.05 dB loss.

The chip was fabricated in a 40 nm 6-metal-layer TSMC CMOS process and occupies 1.6 mm × 1.3 mm including the bond pads; a die photo is shown in Fig. 14(a). The die is wire-bonded directly to the test board using chip-on-board packaging (see Fig. 14(b)). The RX input and TX output are connected using an FBAR duplexer on-board.

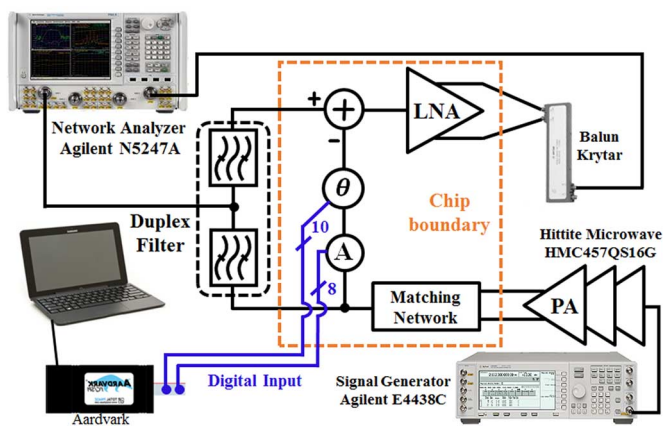


Fig. 15. SIM chip measurement setup.

V. Measurement Results

To test the validity of the canceller design, standard front-end measurements were taken with respect to noise figure and linearity, in addition to the amount of TX suppression achieved by the FPC concept. The device was measured using an Agilent Network Analyzer (N5247A) to characterize the LNA's S-parameters (see Fig. 15). The LNA gain, input matching

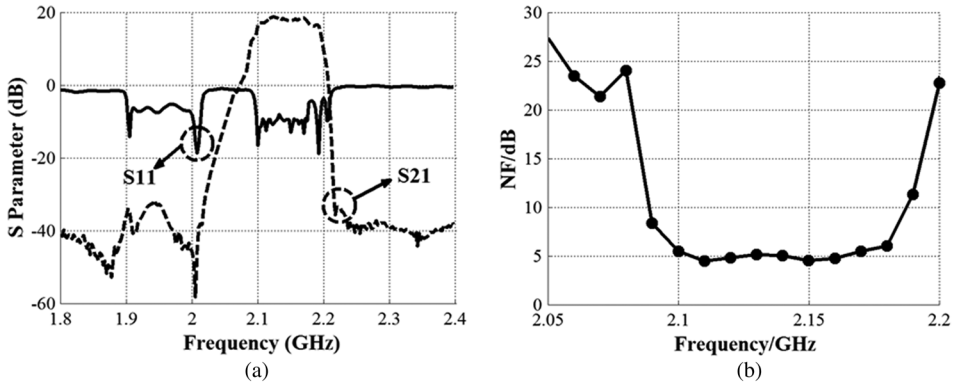


Fig. 16. RX performance. (a) 1.8 GHz to 2.4 GHz S-Parameter measurement results for the S_{21} (RX main signal path), and the S_{11} from the perspective of the antenna side, (b) RX noise figure. Measurement taken with duplexer, which has 1.5–2 dB insertion loss.

network, and noise figure were measured with an on-board FBAR duplexer (Avago Technologies: ACMD-7612). The TX leakage cancellation was measured using the following test setup. An Agilent vector signal generator (E4438C) supplied both a CW and WCDMA modulated signal to a discrete PA (Hittite Microwave Corporation: HMC457QS16G), which then drove the on-chip PA matching network with an array of devices to emulate the drain-to-bulk capacitance of an integrated PA not included in this chip. The PA delivered up to +30 dBm of power to the chip. A laptop with an Aardvark I2C/SPI host adapter (Total Phase, Inc.) provided digital control.

A. LNA Measurement Results

The peak measured conversion gain of the combiner and LNA was 20.4 dB, which included the 1.5 dB insertion loss (IL) from the duplex filter, and a gain variation of 1.2 dB within 60 MHz RX band; see Fig. 16(a). The RX measured double-sideband NF was roughly 5 dB across the RX band; see Fig. 16(b). The estimated contributors to the NF were 1.5 dB IL from the duplexer, an additional loss of 1–1.5 dB from the FPC/RX matching network, and 2–2.5 dB NF from the LNA. The linearity was measured using a two-tone test with CW signals applied at 10 MHz offset from a 2.14 GHz center frequency. The in-band IIP3 of the RX was +3 dBm; see Fig. 17. The overall power consumption was 10 mW from a 1 V supply, which included the LNA and cancellation network.

B. TX Leakage Cancellation Measurement Results

To measure the functionality of the proposed canceller, two signals were injected into the FPC, one through the RX input and the other was applied to the TX input. By adjusting amplitude and phase inside the on-chip cancellation network, an average suppression of 23 dB was observed over a range of PA power levels from +5 dBm to +30 dBm, across a frequency band which included the entire TX band (1.92–1.98 GHz); see Fig. 18(a) and (b). These measurements were taken by digitally modulating the phase and amplitude tuning network for a given frequency, to maximize the cancellation. From extracted simulations, the on chip phase tuning range was expected to be more than 280 degrees. However, the measured phase tuning range of this chip was 50 degrees. The source of the reduction in the

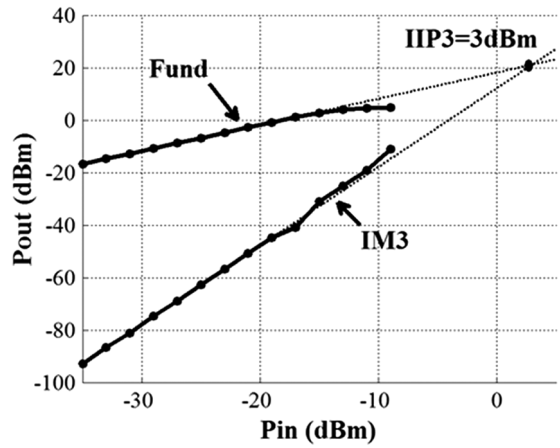
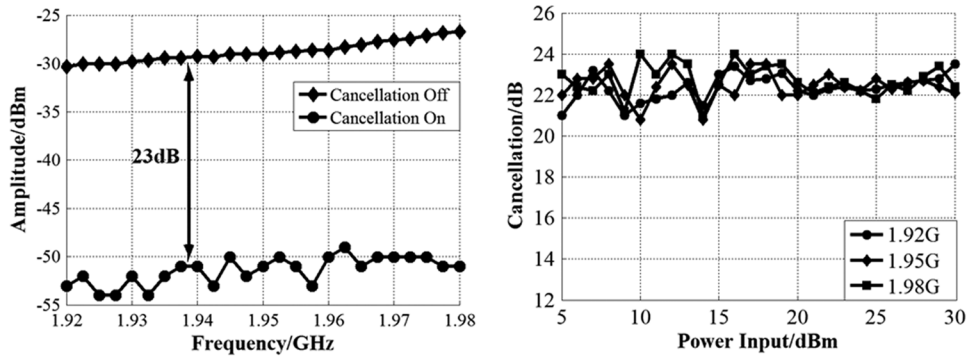


Fig. 17. Measurement results of RX In-band IIP3 with two tones at 10 MHz offset from 2.14 GHz.

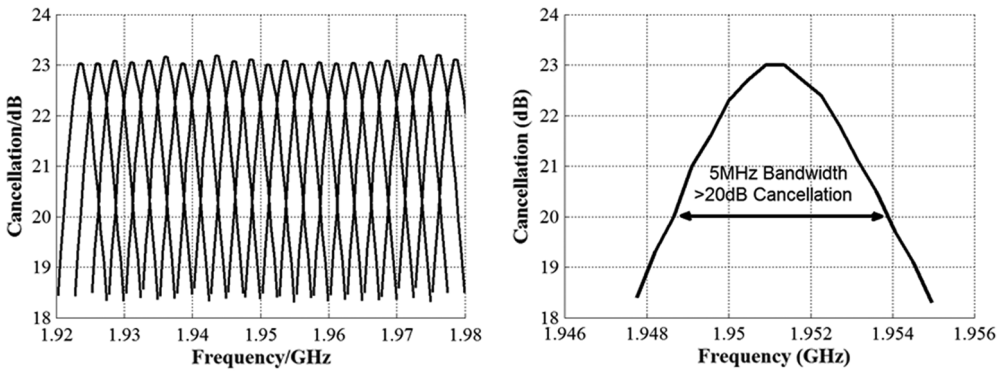
phase tuning range was traced to improperly modeled series resistance associated with an unexpected parasitic inductance. The extra parasitic resistance comes from the interconnection of tunable capacitors, C_3 and C_4 in Fig. 6. Equation (13) reveals the phase tuning range has a high sensitivity to the tank Q, and ultimately, the series routing resistance associated with C_3 and C_4; see Fig. 6. To compensate for the loss in phase tuning range, an additional on-board phase shifter was added to perform some of the measurements.

The cancellation bandwidth was measured in two steps. First, the cancellation was maximized at a particular frequency by adjusting the phase and amplitude for maximum suppression. These settings were then held, and a CW signal was applied, which was then swept in frequency while the relative cancellation at the output of the LNA was measured. After sweeping the CW signal for a given setting, the FPC was re-tuned for a frequency 2.5 MHz higher. The CW interference signal was again swept, which formed the second bell shaped curve. The results were plotted in Fig. 19(a), which shows a sum of these plots across the TX band. A 20 dB cancellation was achieved with greater than 5 MHz bandwidth, which was sufficient to accommodate a 3.84 MHz channel bandwidth associated with the WCDMA standard (see Fig. 19). Next, the phase and gain settings were fixed, and a modulated WCDMA signal was applied



(a) (b)

Fig. 18. Measurement results of TX leakage suppression using a single CW signal. (a) TX cancellation versus frequency @30 dBm output power, (b) TX cancellation versus input power @1.92 GHz, 1.95 GHz and 1.98 GHz.



(a) (b)

Fig. 19. Measurement results of TX leakage suppression versus bandwidth. (a) Leakage cancellation (dB) measured by sweeping tone over TX band, (b) enlarged figure of leakage suppression over a particular TX channel.

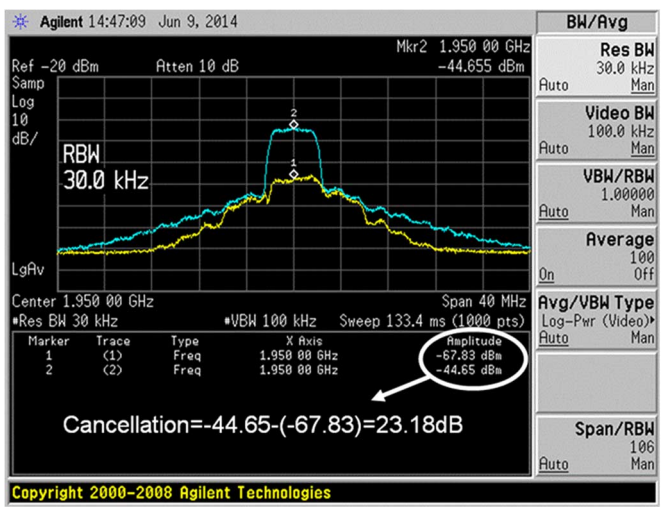


Fig. 20. Measured TX suppression using a modulated WCDMA signal. LNA output spectrum with both cancellation enabled and disabled.

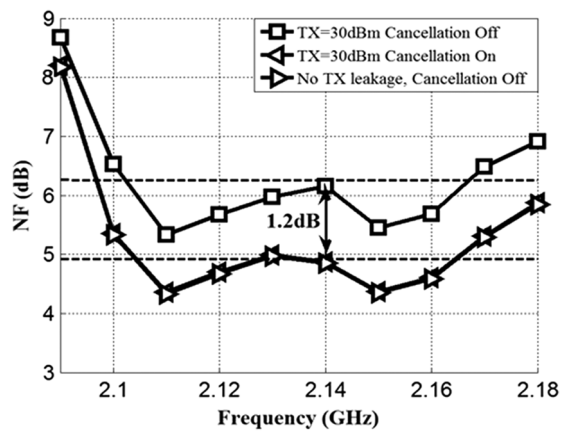


Fig. 21. Measured RX noise figure with and without a TX leakage signal. Also, NF is plotted with +30 dBm block for the case of the canceller enabled and disabled.

to the TX input while the LNA output spectrum was again measured. Data was recorded for this measurement with the canceller network both enabled and disabled. A minimum 20 dB of cancellation was observed over the signal bandwidth, which represents less than 1% of residual leakage power remained post cancellation at the LNA input; see Fig. 20.

A set of measurements were performed to see the impact of the TX leakage signal. As mentioned earlier, a large TX blocker will generate several sources of interference and noise. A +30 dBm CW signal was applied to the transmitter and the noise figure was measured with the canceller enabled and disabled; see Fig. 21. When the canceller was enabled, the RX noise floor went down by 1.2 dB, which was nearly identical to the standalone noise figure measurement when no TX blocker

TABLE II
COMPARISON AND PERFORMANCE SUMMARY

		H. Khatri' 2010 JSSC[1]	H. Kim' 2013 TMTT+ [2]	J. Zhou' 2014 ISSCC [8]	This Work+
Architecture		Active filtering	Feed-forward filtering	Active two port cancellation	Transformer coupling
Technology/VDC		65nm/2V	180nm/1.8V	65nm/?	40nm/1V
TX Suppres.(dB)	Single Tone	-NA-	25	>30	23
	Modulated Signal	-NA-	22.5	-NA-	20△
NF with cancellation circuits active(dB)		4.9	2.84	5	5*
NF degradation due to leakage cancellation(dB)		1.7	0.44	0.8	◊<0.1dB or 1.2dB
RX Gain(dB)		45	25.4	19-34	*18
RX Power Consumption(mW)		44[1a]	16.38[1a]	74.6-83[1b]	10[1a]
Canceller Power Consumption(mW)		48	18.9	13-72	≈0

*RX Gain/NF measured with front-end duplexer, which has 1.5–2 dB loss.
+RX includes only the LNA.
△Measured with a 3.84 MHz WCDMA signal.
◊The transformer used for single-ended to differential conversion has a insertion loss of 1.2 dB and the added two primaries for TX leakage suppression introduces an additional loss of less than 0.1 dB.
[1a]Power consumption includes LNA only. [1b]Power consumption includes the entire RX.

was applied to the receiver (LNA). This implied a negligible noise figure degradation introduced by the cancellation circuitry, which was one of the primary goals of this effort.

C. Comparison With Prior Art

A comparison and performance summary for the proposed integrated canceller network is shown in Table II. The proposed SIM technique introduces a negligible NF penalty with virtually no power overhead.

VI. CONCLUSIONS

This paper explored methods for TX leakage cancellation in traditional frequency division duplexing (FDD) radios with an eye on eventually realizing systems for full-duplex radios. The presence of a large TX blocker in FDD systems places stringent linearity (IIP2 and IIP3) performance demands on the receiver, which can be achieved at the expense of an increased power consumption. This effort uses a passive SIM feed-forward cancellation path with a four-port canceller, and has a minimal noise figure, area, and power consumption penalty. The FPC device was implemented in 40 nm TSMC CMOS technology for a WCDMA application. A measured cancellation of greater than 20 dB over a 5 MHz signal bandwidth is achieved with negligible impact on the overall power consumption and noise figure.

Potential applications for this technique include the current FDD radios, Wi-Fi-Bluetooth coexistence, and any radios dealing with a non-negligible self-interference signal from the transmitter.

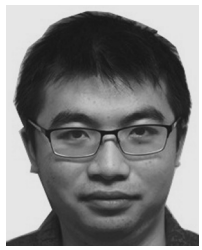
ACKNOWLEDGMENT

The authors wish to acknowledge the assistance and support of Beomsup Kim, Mazhareddin Taghivand, Magnus Wiklund, Roger Brockenbrough, Dennis Yee, David Allstot, Chenxi Huang, and Eric Pepin.

REFERENCES

[1] H. Khatri, P. S. Gudem, and L. E. Larson, "An active transmitter leakage suppression technique for CMOS SAW-Less CDMA receivers," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, Aug. 2010.
[2] H. Kim, S. Woo, S. Jung, and K. Lee, "A CMOS transmitter leakage canceller for WCDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 9, Sep. 2013.
[3] B. A. Floyd, S. K. Reynolds, T. Zwick, L. Khuon, T. Berkema, and U. R. Pfeiffer, "WCDMA direct-conversion receiver front-end comparison in RF-CMOS and SiGe BiCMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1181–1188, Apr. 2005.
[4] D. L. Kaczman *et al.*, "A single-chip tri-band (2100, 1900, 850/800 MHz) WCDMA/HSDPA cellular transceiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1122–1132, May 2006.
[5] P. V. Wright, "A review of SAW resonator filter technology," in *Proc. IEEE Ultrasonics. Symp.*, Oct. 1992, vol. 1, pp. 29–38.
[6] M. Ueda, J. Tsutsumi, S. Inoue, T. Matsuda, O. Ikata, and Y. Satoh, "Ultra-miniaturized and high performance PCS SAW duplexer with steep cut-off filters," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2004, vol. 2, pp. 913–916.
[7] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
[8] J. Zhou, P. R. Kinget, and H. Krishnaswam, "A blocker-resilient wideband receiver with low-noise active two-port cancellation of >0 dBm TX leakage and TX noise in RX band for FDD Co-existence," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 352–353.
[9] H. Khatri, P. S. Gudem, and L. E. Larson, "Integrated RF interference suppression filter design using bond-wire inductor," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1024–1034, May 2008.

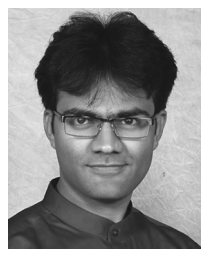
[10] M. Mikhemar, H. Darabi, and A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, Sep. 2013.
[11] J. I. Choi, M. Jain, K. Srinivasan, P. Levis, and S. Katti, "Achieving single channel, full duplex wireless communication," *Proc. ACM MobiCom*, pp. 1–12, 2010.
[12] M. Jain *et al.*, "Practical, real-time, full duplex wireless," *Proc. ACM MobiCom*, pp. 301–312, 2011.
[13] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," *Proc. ACM SigComm*, pp. 375–386, 2013.
[14] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-Band CMOS low-noise amplifier exploiting thermal noise cancelling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, Feb. 2004.
[15] A. Safarian, A. Shameli, A. Rofougaran, M. Rofougaran, and F. de Flaviis, "Integrated blocker filtering RF front ends," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, 2007, pp. 13–16.
[16] S. Youssef, R. V. d. Z, and B. Nauta, "Active feedback technique for RF channel selection in front-end receivers," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, Dec. 2012.
[17] T. D. Werth, C. Schmits, R. Wunderlich, and S. Heinen, "An active feedback interference technique for blocker filtering in RF receiver front-ends," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, May 2010.
[18] H. Khatri, P. S. Gudem, and L. E. Larson, "A SAW-less CMOS CDMA receiver with active TX filtering," in *Proc. IEEE Custom Integrated Circuit Conf.*, 2009, pp. 379–382.
[19] V. Aparin, G. J. Ballantyne, C. J. Persico, and A. Cicalini, "An integrated LMS adaptive filter of TX leakage for CDMA receiver front ends," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1171–1182, May 2006.
[20] H. Darabi, "A blocker filtering technique for SAW-less wireless receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2766–2773, Dec. 2007.
[21] S. Ayazian and R. Gharpurey, "Feedforward interference cancellation in radio receiver front-ends," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 10, pp. 902–906, Oct. 2007.
[22] D. Yang and A. Molnar, "A widely tunable active duplexing transceivers with same-channel concurrent RX/TX and 30 dB RX/TX isolation," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, pp. 321–324.
[23] S. Abdelhalem, P. Gudem, and L. Larson, "A tunable differential duplexer in 90 nm CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, 2012, pp. 101–104.
[24] T. Zhang, A. R. Suvarna, V. Bhagavatula, and J. C. Rudell, "An integrated CMOS passive transmitter leakage suppression technique for FDD radios," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, 2014, pp. 43–46.
[25] J. C. Rudell *et al.*, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, Dec. 1997.
[26] H. Sjoland, A. K. Sanjaani, and A. A. Abidi, "A merged CMOS LNA and mixer for a WCDMA receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, Jun. 2003.
[27] Y. Liao, Z. Tang, and H. Min, "A CMOS wide-band low-noise amplifier with balun-based noise-canceling technique," in *IEEE ASSCC Dig.*, 2007, pp. 91–94.
[28] M. A. Martins, P.-I. Mak, and R. P. Martins, "A single-to-differential LNA topology with robust output gain-phase balancing against balun imbalance," in *Proc. IEEE ISCAS*, 2011, pp. 289–292.
[29] M. Mikhemar, "Interference cancellation in software-defined CMOS receivers," Ph.D. Dissertation, University of California, Los Angeles, 2010.
[30] S. Abdelhalem, P. Gudem, and L. Larson, "Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1316–1326, March 2013.
[31] O. El-Gharniti, E. Kerherve, and J. Begueret, "Modeling and characterization of on-chip transformers for silicon RFIC," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 607–615, Apr. 2007.
[32] D. Chowdhury, C. D. Hull, O. B. Degani, P. Goyal, Y. Wang, and A. M. Niknejad, "A single-chip highly linear 2.4 GHz 30 dBm power amplifier in 90 nm CMOS," in *IEEE ISSCC Dig.*, Feb. 2009, pp. 378–380.



Tong Zhang received degrees in electrical engineering from Southeast University (BS), and University of Washington (MS) in 2011 and 2014, respectively. He is currently pursuing the Ph.D degree in electrical engineering department at University of Washington.

From July 2013 to March 2014, he was an intern in Qualcomm Atheros, San Jose, working on developing new techniques for wideband IQ generation. He was a recipient of ISSCC Analog Devices Outstanding Student Designer Award in 2015. His research interests include self-interference cancellation systems and ultra-wideband millimeter wave transceivers.

Apsara Ravish Suvarna received her B.E. degree from the National Institute of Technology Karnataka, Surathkal, India and M.S. degree from the University of Washington, Seattle in 2006, and 2013, respectively. From 2006 to 2010, she was an analog designer in the power management group of Cosmic Circuits Pvt. Ltd., Bangalore, where she worked on low-drop out regulators, bandgap references and power-on-reset circuits. Her research interests include RF circuit and system design, and low-power mixed-signal circuits. Since 2013, she has been working as an RFIC designer with the cellular transceiver group at Qualcomm, San Diego.



Venumadhav Bhagavatula (S'10) received the B.E. degree from the University of Delhi, New Delhi, M.Tech. degree from the Indian Institute of Science, Bangalore, and Ph.D. degree from the University of Washington, Seattle, in 2005, 2007, and 2013, respectively. Since 2014, he has been with the Modem Lab at Samsung Semiconductors Inc., San Jose, CA.

His research interests include RF/mm-wave, and low-power mixed-signal circuits. Dr. Bhagavatula was the recipient of the CEDT Design Medal from the Indian Institute of Science (2007), the Analog Devices Outstanding Student Designer Award (2012), and co-recipient of the best student-paper award at the RFIC 2014.

Jacques Christophe Rudell (M'00–SM'09) received degrees in electrical engineering from the University of Michigan (B.S.), and UC Berkeley (M.S., Ph.D.).

After completing his degrees, he worked for several years as an RF IC designer at Berkana Wireless (now Qualcomm), and Intel Corporation. In January 2009, he joined the faculty at the University of Washington, Seattle, as an Assistant Professor of Electrical Engineering. While a Ph.D. student at UC Berkeley, he received the Demetri Angelakos Memorial Achievement Award, a citation given to one student per year by the EECS department. He has twice been co-recipient of the best paper awards at the International Solid-State Circuits Conference, the first of which was the 1998 Jack Kilby Award, followed by the 2001 Lewis Winner Award. He received the 2008 ISSCC best evening session award, and was co-recipient of the 2014 RFIC Symposium best student paper award. Dr. Rudell served on the ISSCC technical program committee (2003–2010), and on the MTT-IMS Radio Frequency Integrated Circuits (RFIC) Symposium steering committee (2002–2013), where he was the 2013 General Chair. He served as an Associate Editor for the Journal of Solid-State Circuits (2009–2015).

Dr. Rudell's research interests include topics in RF and mm-wave integrated circuits design for communication systems, in addition to biomedical electronics for imaging and neural interface applications. He is an active member at the Center for Sensorimotor Neural Engineering (CSNE), an NSF Engineering Research Center (ERC) based at the University of Washington, and he is the recipient of an NSF CAREER award.