High-Voltage Compliant, Capacitive-Load Invariant Neural Stimulation Electronics Compatible with Standard Bulk-CMOS Integration

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***Abstract*—A neural stimulator architecture is described which can drive biphasic, constant-current waveforms through a wide range of electrode impedances with approximately ±11V compliance, while using a low-voltage, modern bulk-CMOS technology. The design, based on an H-bridge topology, utilizes a regulated "discharge" phase during biphasic delivery to account for "capacitive-looking" electrodes, extending the bipolar on-chip headroom of a CMOS stimulator. Stimulus current is supplied by integrated switched-capacitor, dynamic voltage supplies (0-12V), which operate with closed-loop control. The stimulator topology also uses a single, low-voltage current DAC to regulate the entire biphasic current waveform. The voltage supply block has been fabricated in 65nm standard CMOS. Cadence simulations of the proposed biphasic driver, designed for 250µA maximum current, are given for several "high" impedance electrode models. The efficacy of the proposed integrated electronics in potential neural stimulation applications is demonstrated with a board-level prototype, which has been designed and evaluated *in-vivo* (rat).**

Keywords—neural stimulation; high-voltage; bulk-CMOS

I. INTRODUCTION

Electrical stimulation of the nervous system has found successful use in FDA-approved devices (retinal and cochlear implants, deep brain stimulation for Parkinson's disease and neuropsychiatric disorders, functional electrical stimulation of periphery nerves), and, in recent years, has gained traction as an important complement to neural-recording systems in brain-computer interfaces (BCIs). In the latter, neural stimulation could be used as a direct means of closing the "BCI loop" and/or re-establishing brain control over paralyzed muscles [1]. Such closed-loop systems could lead to new, exciting neuroprostheses and rehabilitation methods [2] requiring implantable neural interfaces.

In delivering electrical stimuli to neural tissue, biphasic, current-regulated pulses are typically applied between two electrodes using specialized electronics, with the resulting electrode-tissue-interface having a complex electrical impedance, Z_E. Although Z_E varies across stimulation applications, high bipolar driving voltages (> ±10V) are often required to deliver the requisite charge to trigger the desired level of neural response. Moreover, Z_E often displays both resistive and capacitive characteristics, and even if Z_E is well-characterized in the lab, the impedance can change after implantation [3], [4]. Thus, practical biphasic stimulators must both support high headroom voltages and be invariant to Z_E in reliably driving biphasic, charge-balanced waveforms.

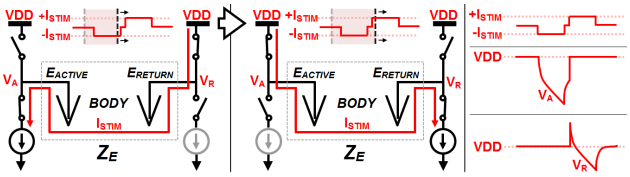

Fig 1. Biphasic constant-current stimulus delivery via traditional H-bridge driver when Z_E exhibits capacitive characteristics.

Neural stimulators have been realized in many technologies with varying levels of integration. Yet, silicon CMOS serves as the backbone of modern digital electronics and allows the realization of complex mixed-block systems (i.e. both analog and digital) on a single silicon die. Therefore, integration of all neural interface functionality on a single-silicon substrate, (e.g. recording, wireless interfaces, energy harvesting, signal processing, stimulation) has the primary benefit of providing for a small form-factor, easy to implant, low-cost system. However, the discussed headroom voltages required for a practical general-purpose stimulator present barriers to modern CMOS design, since terminal-to-terminal device voltages in such a process must be kept below a low-voltage threshold (e.g. 1V to 3.3V) to ensure device reliability. Hence, many CMOS stimulators published to date have output compliance constrained by the device limits [4]; e.g., a chip using 2.5V devices would be limited to ±1.25V compliance.

Extending CMOS stimulator voltage compliance past individual device limits has been previously investigated. [5] and [6] achieve close to ±VDD compliance. The highest compliance figure known to the authors is reported in [7], which features a biphasic stimulator using a sinking H-bridge topology. This work achieves approximately ±9V compliance (30µA max. stimulus) using 3.3V devices, yet the reliability of its "pre-driver" circuits under varied capacitive loading is unclear, and the H-bridge appears to deliver current in two complementary phases (Fig. 1). Problems with such a scheme could arise when Z_E stores significant charge (due to capacitive qualities), so that during the current direction reversal (Fig. 1), voltages exceeding VDD can be created at the driver output, potentially causing device failure, junction breakdowns, and unregulated current through Z_E. While Z_E should "self-discharge" if given time, it is impractical to have the system design and stimulation pattern determined by an empirically found decay rate which could change over time.

To provide reliable operation over a wide range of neural stimulation applications, this paper proposes biphasic, constant-current stimulator electronics, designed in 65nm

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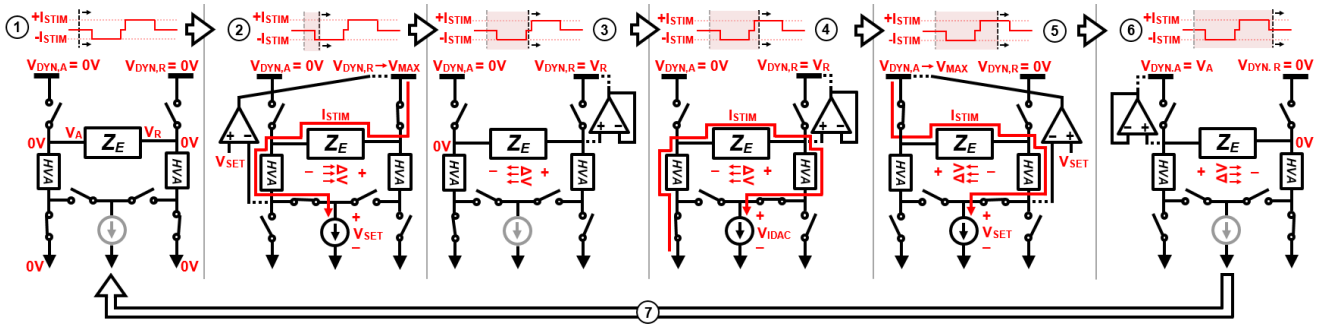

Fig 2. Biphasic constant-current driver state cycle (1-7) during stimulus delivery.

CMOS, which reliably operate with approximately ±11V compliance, independently of Z_E. Section II describes the H-bridge based biphasic driver architecture, which accounts for Z_E charge storage in its design to avoid large voltage excursions on the driver electronics. This is followed by a description of the system-critical dynamic voltage supply circuit in Section III. Finally, dynamic voltage supply chip measurements, biphasic driver simulations, and *in-vivo* (rat) results from a board-level prototype are given in Section IV.

II. System Overview

A. Biphasic H-Bridge with Regulated Discharge Phase

Fig. 2 depicts the proposed biphasic constant-current driver, which incorporates the discharge of the electrode-tissue interface (Z_E) into stimulus delivery to account for Z_E charge storage. Z_E is treated as a two-port load, with "active" and "return" electrode connections. Each power rail is the output of a dynamic voltage supply circuit, which works within a positive-current driver (PCD) loop (Fig. 3), modeled by op-amps in Fig. 2, to deliver stimulus current and to track the electrode voltage when unloaded. The high voltage adapters (HVAs) effectively function as conducting NMOS devices, and protect the low-side circuits from voltages exceeding VDD; each HVA is biased by the supply on the same-side of Z_E. Stimulus delivery is carried out in a 7-state cycle (Fig. 2):

1) Idle: PCDs are off/discharged and electrodes are shorted to chip ground (GND); low-power consumption state.

2) Negative Current via H-Bridge: Current DAC (IDAC) is connected to the active side of H-Bridge and the return PCD is activated; $-I_{STIM}$ is seen by the active electrode and the IDAC voltage is maintained at V_{SET}, which is high enough to keep the IDAC in regulation (i.e. a few hundred millivolts).

3) Interphase Delay: One clock cycle (or more).

4) Positive Current via Z_E Discharge: IDAC is connected to the return side of H-Bridge and GND is switched in to act as low-Z node; during Z_E discharge, active electrode (with voltage V_A) sees $+I_{STIM}$. Return PCD follows falling return electrode voltage (V_R), keeping the return HVA properly biased. A low V_R will force the IDAC out of regulation; detection of V_{IDAC} passing V_{SET} forces a transition to State 5.

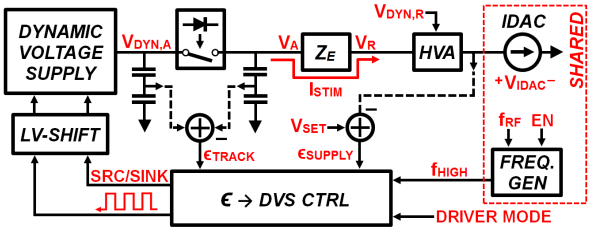

Fig 3. Active positive-current driver (PCD); return PCD is the same, but with complementary return/active connections.

5) Positive Current via H-Bridge: Remainder of balancing pulse is supplied in the same way as leading pulse, but with the active PCD supplying I_{STIM}.

6) Passive Discharge: Return electrode is switched to GND. Z_E passively discharges (while active PCD tracks V_A).

7) Active Discharge/Charge Balance: Z_E is discharged via electrode shorting and/or auxiliary charge balance circuitry.

The PCDs are guided through the Fig. 2 cycle by a low-voltage, digital state-machine operated at low clocking rates; the State 4 to State 5 transition can be triggered outside of the state-machine to decouple the transition speed from the clock.

B. Positive-Current Driver

The biphasic driver relies on the coordinated operation of two (active and return) high-voltage compliant positive-current drivers (PCDs), each having three operating modes (IDLE, TRACK, and SUPPLY, with feedback used in the two latter). For optimal efficiency, all circuits in the stimulus current path are implemented with the process I/O devices, allowing the use of a boosted VDD (up to 2.5V). The block diagram for the active PCD is shown in Fig. 3; key blocks/concepts include:

1) Dynamic Voltage Supply: Switched-capacitor block which can source current (SRC) up to a "V_{MAX}" and sink current (SINK), when unloaded, down to 0V; this current (magnitude set by pulse signal frequency) flowing in/out of internal output capacitor results in variable voltage generation.

2) High Voltage Adapter (HVA): Acts as a closed switch while protecting IDAC from high voltages. Comprised of stacked triple-well NMOS devices, biased by the supply interfacing with the same electrode; a capacitor string with in-parallel voltage-locking diodes safely distributes the supply voltage across the NMOS gates. When the supply voltage is low, this block is biased by VDD, maintaining HVA conduction. The HVA boosts the IDAC output impedance.

3) Current DAC (IDAC): Can be realized with low-voltage devices/topologies. Low drop-out voltage required to maximize driver output range. Shared by both drivers; could improve charge-balance (before using auxiliary circuitry).

4) Frequency Generation: To supply high stimulus currents at high voltages, the form-factor tradeoffs of the voltage supplies require "high" pulse frequencies (>100 MHz); can be generated on-chip via an integer-divider PLL

optimized for low-power performance. Most of the time the drivers will be in IDLE mode, allowing PLL power-down.

5) Feedback: In SUPPLY mode, the high-side switch is closed, V_{IDAC} - V_{SET} is the error signal (ε), the supply is set to SRC (assuming V_A - V_R has non-negative slope during active PCD constant-current delivery), and the feedback loop sets the average period of the supply pulse signal to produce a $V_{DYN,A}$ which maintains V_{IDAC} at V_{SET}. ε can be 1-bit (on/off), detected by a simple comparator. In TRACK mode, the high-side switch is open, ε is $V_{DYN,A}$ - V_A, and feedback is applied to make $V_{DYN,A}$ track V_A (approx.). With only two PCDs in consideration, ε can be 1-bit, and used to gate pulses into the supply. Each pulse passed results in a ΔV at $V_{DYN,A}$; by knowing where in the Fig. 2 cycle the driver is, the SRC/SINK supply control (determining the ΔV sign) can be reliably set.

6) High-Side Switch: Implemented with diode; stimulus current direction and described feedback scheme adequately function to keep the diode "on" and "off" when desired.

III. Dynamic Voltage Supply Circuit

The schematic of the dynamic voltage supply (DVS) is shown in Fig. 4. The single-stage circuit can supply switched-capacitor current from V_{IN} to V_{OUT} (SRC) while establishing a voltage difference between V_{OUT} and V_{IN}, as well as sink switched-capacitor current in the V_{OUT} to V_{IN} direction (SINK), which in our stimulator allows for the safe and feedback-controlled discharge of the positive-current drivers; for both settings, $0 < V_{OUT} - V_{IN} < VDD$. A circuit similar to [8] is used but all switch signals have been decoupled from the C_{PUMP} capacitors via the M_{N5-6} level-shifter, and the NMOS devices M_{N3-4} have been added to allow the complete discharge of the output capacitor under non-loaded conditions.

In Fig. 4, $\Phi_{A,B}$ are complementary pulse/clock signals. Assuming a large output capacitance, the single-stage circuit, operated in both settings, displays the same effective internal resistance; this term is inversely proportional to C_{PUMP} and the $\Phi_{A,B}$ frequency, making V_{OUT} linearly related (approx.) to the "pumping period" under constant-current loading. When unloaded, V_{OUT} - V_{IN} can traverse the 0V to VDD span, with rise/fall time determined by the internal resistance and output capacitance; the circuit can maintain V_{OUT} by setting $\Phi_{A,B}$ to DC, since there is no load resistor to ground.

To create high voltages, several stages are cascaded (Fig. 4), as in [8], with a large output capacitor (C_{OUT}) attached to the terminating stage. All NMOS transistors are triple-well devices, allowing local body-biasing to suppress the body-effect. The highest voltage (V_{MAX}) generated by this circuit is limited by the reverse breakdown voltage of the p-sub/n-well junction; for the 65nm CMOS process used in this work, this limit is approximately 12V. High voltages also force the use of MiM/MoM capacitors for C_{PUMP}, C_{LS}, and C_{OUT}. To provide 0V to V_{MAX} at the output, the input of the multi-stage supply is set to chip ground; this connection also provides enhanced DC power-supply isolation for the electrodes/tissue. A DVS can be designed with 50% to 60% efficiency at peak output power.

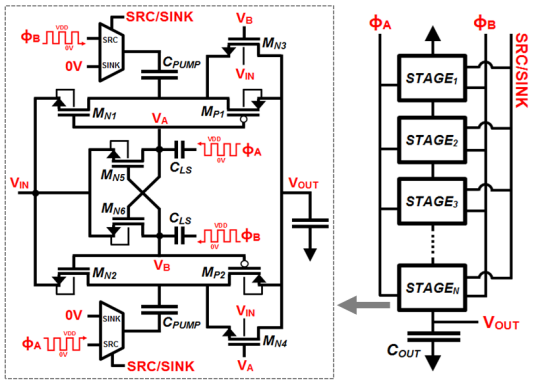

Fig 4. Proposed dynamic voltage supply circuit; transistor-level, single-stage schematic, and high-voltage, multi-stage circuit block diagram.

IV. Results

A. Chip Measurements

A 6-stage dynamic voltage supply (DVS) has been fabricated in 65nm CMOS; a die photo of the test-chip is given in Fig. 5, with the supply circuit highlighted. The 2.5V devices of the process were used to implement the circuit. C_{PUMP} and C_{OUT} (see Fig. 4) are 2pF and 75pF, respectively, and the switching devices are sized for 400MHz (max.) operation.

The supply rise/fall time under non-loaded conditions (Fig. 5), shows the ability to track quickly changing electrode voltages; a "faster" supply, operated at the same frequency, can be realized by making C_{PUMP} larger and/or C_{OUT} smaller. Loaded performance (constant-current) can be seen in Fig. 5, showing output voltage versus $\Phi_{A,B}$ period (both measured and predicted); the prediction is derived from a model of the supply internal resistance. The difference in slope between the predicted/measured SRC curves is attributed to reverse leakage current due to Φ_A, Φ_B overlap; the result is reduced efficiency (an improved non-overlapping clock would mitigate this issue).

B. Biphasic Driver Simulations

A biphasic driver designed for 250μA stimulus delivery (max.) and ±11V compliance has been implemented at the schematic level in *Cadence*; potential uses include intracortical and intraspinal stimulation. The IDAC has an R_{OUT} of 500kΩ; the high frequency supply clock is 125MHz, and error detection circuitry (using non-ideal comparator model) is operated at 25MHz; all other blocks are implemented at the transistor level. Fig. 6 shows the voltage across Z_E for several "high-impedance" interfaces (Z_{E1-4}), when 250μA biphasic current (200μs pulse-width, 5μs interphase delay) is delivered.

System performance, for a "worst-case" stimulus rate of 1kHz, is given in Table 1. Frequency synthesis and error detection front-end circuitry are not included in the power

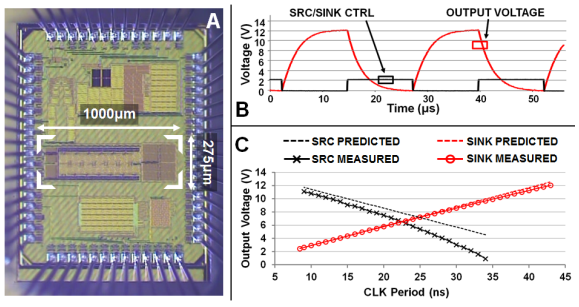

Fig 5. Dynamic voltage supply measurements; (A) test-chip die photo with supply circuit highlighted; (B) unloaded transient response (f_{CLK} = 120 MHz, VDD = 2.3V); (C) 200μA SRC/SINK output voltage vs. T_{CLK} (VDD = 2.5V).

figures (the draw of these blocks should be low compared to the supplies and not contribute to "idle" consumption). The stimulator demonstrates adequate stimulus current regulation, and although HVA mismatches are not simulated, the DC stimulus mismatch, just by using fixed-duration passive/active discharge phases post-stimulus, is below 100nA for $Z_{E1\text{-}4}$. Considering relative stimulus levels and duty cycles, the power consumption is comparable to systems featuring a static high-voltage rail (which also needs to be generated) and high-voltage tolerant devices (e.g. [9]). A system with similar performance can be designed for higher current levels by increasing the clock frequency of the supply/error-detection and/or increasing the C_{PUMP} size (Fig 4).

C. *In-Vivo Board Testing*

A board-level prototype has been realized to investigate potential uses for the proposed integrated stimulator (considering its ±11V compliance), and to verify the current-regulating ability of an H-bridge driver *in-vivo*. The board uses discrete, high-voltage tolerant components and is operated by a microcontroller; charge balance is assured by the inclusion of large blocking capacitors; the fabricated DVS chip is not used in this system. Two rats, previously surgically implanted with several electrode configurations (subdural cortical, intraspinal, and intramuscular) were stimulated while moving freely about an observation area. The stimulator board was connected to the electrodes with a tethered cable. A 300µm multi-stranded, stainless steel (SS) wire was used for the current return, and the active electrode was either a 300µm multi-stranded SS wire (intramuscular, cortical) or 30µm Pt/Ir (intraspinal). Electromyographic (EMG) responses in the muscle and spinal cord (latter for cortical stimulation) were recorded during stimulus delivery. Sufficient current was delivered to cortical, spinal, and muscle electrodes to evoke forelimb or neck contractions.

Z_E voltage at movement-eliciting current levels (verified visually and with EMG) is shown for intramuscular stimulation (SS active/return wires in close proximity) in Fig. 7; Z_E voltages for subdural cortical stimulation (distant SS return) also stay within the capabilities of the proposed stimulator. Responses were also provoked with spinal stimulation (distant SS return), and with lower Z_E driving voltages. Active/return currents measured during stimulus delivery (Fig. 7) suggest an H-bridge biphasic driver scheme, independent of return placement, is functionally equivalent to a traditional stimulator architecture with current regulation only interfacing with the active electrode. The frequency-dependent nature of the Fig. 7 voltage waveforms supports the need for the proposed "capacitive-load invariant" biphasic stimulator (albeit a portion of the capacitance can be attributed to the blocking capacitors).

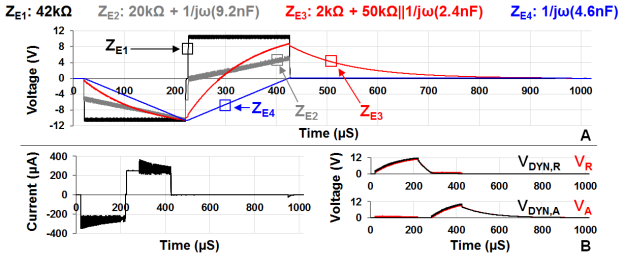

Fig 6. *Cadence* simulations of biphasic stimulator driver ($VDD_{DIGITAL}$ = 1V, $VDD_{DVS/HVA}$ = 2.5V): (A) Z_E voltage for several electrode models; (B) active electrode current and PCD voltages for Z_{E3} stimulation.

TABLE 1. SIMULATED PERFORMANCE FOR 250 MICROAMP, 200 MICROSECOND PULSE-WIDTH, BIPHASIC CURRENT DELIVERY

Stimulator Performance Metric	Electrode-Tissue Model			
	Z_{E1}	Z_{E2}	Z_{E3}	Z_{E4}
I_{AVE} (NEG) Delivered (µA)	-249.8	-249.5	-248.8	-248.3
I_{AVE} (POS) Delivered (µA)	249.7	250.1	249.6	251.3
I_{DC} Delivered @ 1kHz (nA)	4.7	96.1	-16.5	-20.6
Power Cons. @ 1kHz (mW)	3.00	2.71	1.93	1.19
Power Cons. @ Idle (µW)	30*			

*1MHz System Clock

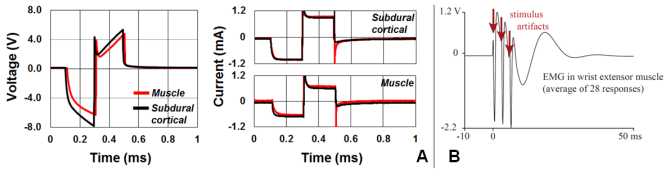

Fig. 7 Board *in-vivo* results for 200µs pulse-width biphasic stimulation: (A) Z_E voltage and active/return current (switching transients result of on-board parasitics) for 710µA intramuscular stimulation (3@300Hz repeated at 1Hz), and for 1000µA cortical stimulation (5@300Hz repeated at 1Hz); (B) wrist-extensor (triceps) EMG recordings during 710µA intramuscular stimulation.

V. CONCLUSION

A biphasic, constant-current stimulator architecture is presented in 65nm CMOS (with its key block fabricated and tested) which shows to reliably function, independent of electrode type/placement, with ±11V compliance; the highest reported for such a system designed in low-voltage CMOS, to the knowledge of the authors. *In-vivo* evaluation of a board-level H-bridge stimulator shows the potential use of the proposed integrated system in several stimulation applications, including cortical, intraspinal, and intramuscular stimulation.

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