A Class-G Switched-Capacitor RF Power Amplifier

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***Abstract*—A switched-capacitor power amplifier (SCPA) that realizes an envelope elimination and restoration/polar class-G topology is introduced. A novel voltage-tolerant switch enables the use of two power supply voltages which increases efficiency and output power simultaneously. Envelope digital-to-analog conversion in the polar transmitter is achieved using an SC RF DAC that exhibits high efficiency at typical output power backoff levels. In addition, high linearity is achieved and no digital predistortion is required. Implemented in 65 nm CMOS, the measured peak output power and power-added efficiency (PAE) are 24.3 dBm and 43.5%, respectively, whereas when amplifying 802.11g 64-QAM OFDM signals, the average output power and PAE are 16.8 dBm and 33%, respectively. The measured EVM is 2.9%.**

***Index Terms*—Envelope elimination and restoration, EER, polar transmitter, power amplifier, RF DAC, SCPA, switched-capacitor power amplifier.**

I. Introduction

THE power amplifier (PA) is the dominant energy dissipater in mobile RF wireless communication systems. High efficiency is critical to conserving energy and increasing battery lifetime, further enhancing the mobility of such devices. Moreover, non-constant envelope (non-CE) modulation methods (e.g., *QPSK*, *QAM*, *OFDM*, etc.) are needed to achieve high spectral efficiency in modern communication standards (e.g., *Wi-Fi*, *WiMAX*, *LTE*, etc.) [1], [2]. Generally, energy efficiency trades off against spectral efficiency which increases the PA design challenge.

Power efficiency in an RF PA is usually defined by the drain efficiency (η) or the total power-added efficiency (PAE):

$$\eta = P_{\rm out}/P_{\rm DC} \tag{1}$$

$$\text{PAE} = P_{\rm out}/(P_{\rm in} + P_{\rm DC}) \tag{2}$$

where $P_{\rm in}, P_{\rm out}$, and $P_{\rm DC}$ are the input power, output power, and DC power dissipation, respectively. A linear RF PA shows a quadratic relation between $P_{\rm out}$ and the output voltage $V_{\rm out}$:

$$P_{\rm out} = 0.5\, V_{\rm out}^2 / R_{\rm LOAD} \tag{3}$$

where $R_{\rm LOAD}$ is the transformed load resistance.

A communication standard with superior spectral efficiency encodes information instantaneously in both the amplitude, $A(t)$, and phase, $\phi(t)$, domains. A large peak-to-average power ratio (PAPR) is a well-known drawback of such standards. In a linear PA (e.g., class-A, -AB, etc.), $V_{\rm out}$ varies over time but $P_{\rm DC}$ remains relatively constant; hence, the efficiency is very low when the output power level is low. This problem is worse with a large PAPR (e.g., $\sim$13 dB for *Wi-Fi* and *WiMAX*) because the probability is increased for signals with low output power.

In order to improve the efficiency for large PAPR signals, it is desirable to operate the PA close to its saturated output power level where it is inherently most efficient. However, external linearization circuitry is often necessary in this region because of strong non-linearities. Several approaches take advantage of power-efficient switching amplifiers for non-CE standards such as pulse-width modulation (PWM) [3], [4], outphasing [5], [6] and envelope elimination and restoration (EER) [2], [7], [8]. The EER technique, for example, combines a highly-efficient switching power amplifier with an efficient, linear supply modulator [7]. Digital PA (DPA) architectures, which modulate the envelope signals digitally, have gained substantial interest with scaled CMOS technologies [9]–[11]. The SCPA extends EER to a digitally-modulated switching topology to achieve high average efficiency and output power with superior linearity [12]–[14].

Class-G amplifiers utilize several power supplies at different voltages. The class-G SCPA described herein operates from two independent power supply voltages which increases the average efficiency substantially for large PAPR signals [15]. The optimal power supply voltage(s) is selected based on a digital code word representation of $A(t)$; i.e., selected capacitors are switched between $V_{\rm DD}$ and $V_{\rm GND}$ and/or $V_{\rm DD2}$ and $V_{\rm GND}$ where $V_{\rm DD2}$ is larger than $V_{\rm DD}$ (e.g., $V_{\rm DD2} = 2V_{\rm DD}$). A unique advantage of the SCPA approach is the ability to use $V_{\rm DD}$ and $V_{\rm DD2}$ *simultaneously* to further increase energy efficiency and linearity. A novel switch design allows charging of the capacitor array over the $V_{\rm DD}$ and $V_{\rm DD2}$ domains while maximizing efficiency and minimizing reliability concerns due to leakage currents and voltage overstresses. The theory of operation for an SCPA is reviewed briefly and the class-G topology is described in Section II. Circuit designs are detailed in Section III and experimental results are given in Section IV while Section V concludes the paper.

II. Theory of Operation

A. Conventional SCPA and Efficiency

A block diagram of an SCPA is shown in Fig. 1(a). The output amplitude is modulated by selecting the number of capacitors, *n*,

Manuscript received September 03, 2012; revised January 30, 2013; accepted February 01, 2013. Date of current publication April 19, 2013. This paper was approved by Guest Editor Srenik Mehta. Research funded by the Semiconductor Research Corporation contract 1836.085.

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Digital Object Identifier 10.1109/JSSC.2013.2252754

being switched between $V_{\rm GND}$ and $V_{\rm DD}$ from among the total number of capacitors, N, in the array [14]. Assuming that inductor (L) and capacitor (C) are resonant at the operating frequency, the equivalent circuit of Fig. 1(b) is used to calculate the corresponding $V_{\rm out}$ where $2/\pi$ is the first coefficient of the Fourier series:

$$V_{\rm out} = \frac{2}{\pi}\left(\frac{n}{N}\right)V_{\rm DD}. \tag{4}$$

The output power is quadratically related to $V_{\rm out}$:

$$P_{\rm out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\frac{V_{\rm DD}^2}{R_{\rm opt}}. \tag{5}$$

The ideal peak efficiency of the SCPA is 100% as in other switching power amplifiers. In practice, however, the peak efficiency is degraded for several reasons. First, some of the power generated by the PA is dissipated in the output matching network because of the low quality factors of passive devices (e.g., integrated spiral inductors). This drawback is mitigated using off-chip inductors with higher quality factors, or by minimizing the impedance transformation ratio using a higher supply voltage. Second, the parasitic resistances associated with the switching transistors dissipate power. This loss is reduced with process scaling because of the reductions of switch parasitics. Third, the power required to drive the switches is significant if the switches are large. Each switch is driven by an inverter-based buffer chain from the decoder logic. The dynamic power dissipation for a given carrier frequency is less in scaled CMOS processes because of the reduced capacitances and supply voltage. Finally, the dynamic power required to charge the switched-capacitor (SC) array in an RF DAC is proportional to the effective capacitance in the SC array that is switched and is also related to the loaded quality factor, $Q_{\rm LOAD}$, of the output matching network. Although all of these factors affect efficiency, the last has the greatest effect at low output power levels.

Considering inductance as a high impedance component for a signal with fast transitions, the dynamic power consumed by the bottom-plate switches driving the array is:

$$P_{\rm SC} = C_{\rm in}V_{\rm DD}^2 f \tag{6}$$

where f is the RF carrier frequency and $C_{\rm in}$ is the series combination of the switched and un-switched capacitors (Fig. 1(c)):

$$C_{\rm in} = \frac{n(N-n)}{N^2}C. \tag{7}$$

The overall efficiency follows from (5)–(7):

$$\eta_{\rm ideal} = \frac{P_{\rm out}}{P_{\rm out}+P_{\rm SC}} = \frac{1}{1+\frac{\pi}{4}\frac{(N-n)}{n}\frac{1}{Q_{\rm LOAD}}} \tag{8}$$

where $Q_{\rm LOAD}$ is:

$$Q_{\rm LOAD} = \frac{2\pi fL}{R_{\rm opt}} = \frac{1}{2\pi fCR_{\rm opt}}. \tag{9}$$

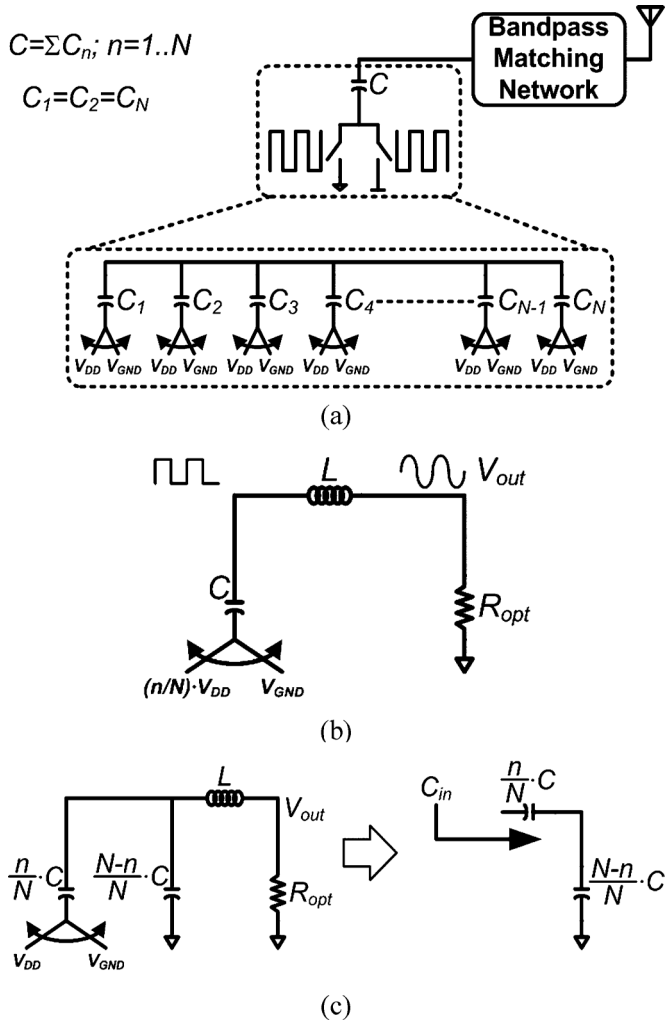


Fig. 1. (a) Conceptual block diagram of an SCPA, and equivalent circuits to calculate (b) $P_{\rm out}$ and (c) the dynamic power dissipation $P_{\rm SC}$.

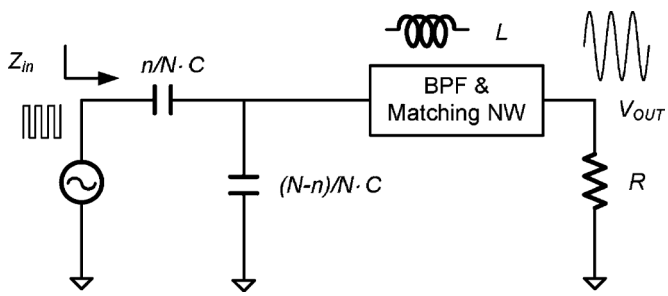


Fig. 2. SCPA model seen by the operating switches.

Efficiency can be investigated from the viewpoint of the switches which are generating square waves; Fig. 2 shows a model where C is the total array capacitance and $Z_{\rm in}$ is the effective impedance. $Z_{\rm in}$ is purely resistive for the maximum power case $(n = N)$ because the bandpass matching network resonates with the total array capacitance at the carrier frequency. For different envelope codes, however, $Z_{\rm in}$ varies as the capacitor connections vary with n.

$Z_{\rm in}$ is derived versus the input code from Fig. 2:

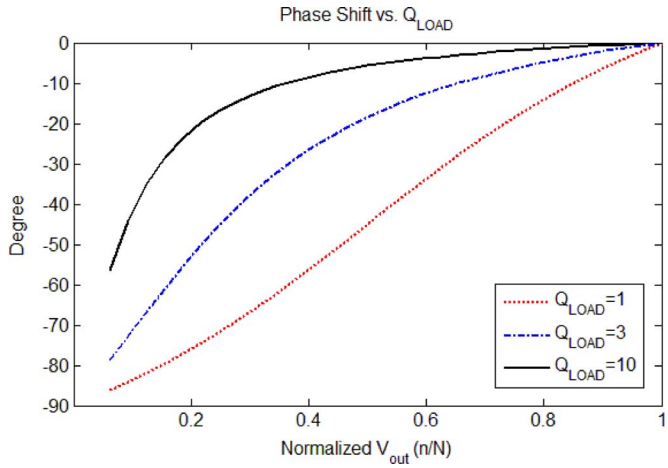


Fig. 3. Phase angle of $Z_{\rm in}$ versus the normalized output voltage.

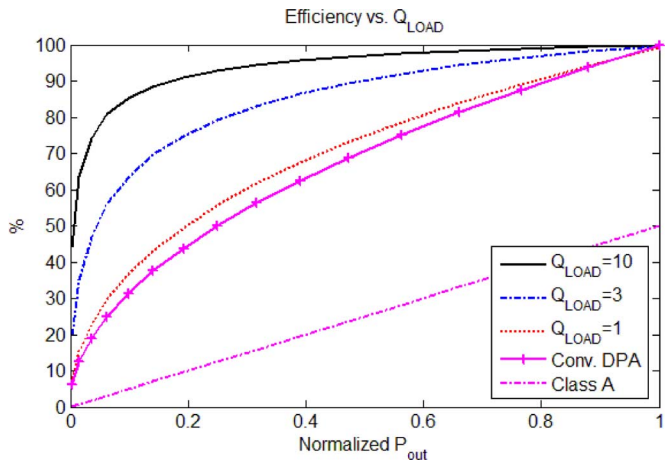


Fig. 4. Ideal efficiency vs. $P_{\rm out}$ for an SCPA with several $Q_{\rm LOAD}$ values and for conventional class-A and DPA circuits.

$$Z_{\rm in} = \frac{1}{j\omega\frac{n}{N}C} + \frac{1}{\frac{1}{R+j\omega L} + j\omega\frac{(N-n)}{N}C}. \qquad (10)$$

Because $Z_{\rm in}$ is purely resistive when $n = N$, a 0° phase shift exists between the voltage and current signals at the switches. As n decreases, $Z_{\rm in}$ becomes capacitive and the phase shift increases which degrades the efficiency. The total phase shift depends on the quality factor of the matching network; it is reduced using a higher $Q_{\rm LOAD}$ (Fig. 3).

Ideal efficiency versus normalized $P_{\rm out}$ is plotted in Fig. 4 for an SCPA with several values of $Q_{\rm LOAD}$, a conventional current source-based DPA and a class-A PA. These results are computed using (8) and verified via *SpectreRF*™ simulations using ideal passive components and *AHDL*-modeled switches. The ideal peak efficiency of 100% degrades with lower $P_{\rm out}$ in all cases. The SCPA shows higher efficiency with higher $Q_{\rm LOAD}$ values because of reduced power in switching the capacitors and less phase shift with the modulated impedance at the switches [14].

One way to increase efficiency at power backoff is to use higher $Q_{\rm LOAD}$ values. However, the maximum $Q_{\rm LOAD}$ for an SCPA is limited to ∼2–3 to minimize the insertion loss in the matching network.

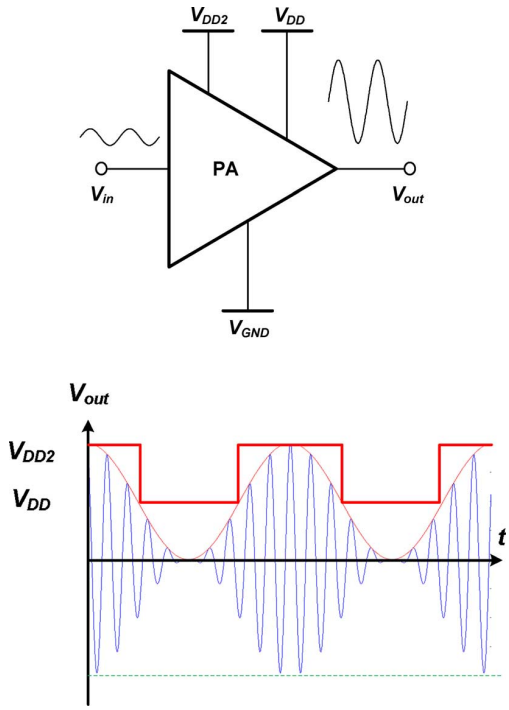


Fig. 5. Conceptual class-G amplifier and its operation with two power supply voltages.

Another way to increase energy efficiency is to employ a class-G architecture that uses a second power supply voltage [2], [15]. For example, if $V_{\rm DD}/2$ is employed as well as $V_{\rm DD}$, there is a second peak in the efficiency characteristic −6 dB below the peak output power. This increases the average efficiency when amplifying non-CE signals as detailed below. In a conventional linear amplifier, switching the power supply voltage during operation can lead to glitches that degrade fidelity [16]. The class-G architecture is more amenable to switching power amplifiers because the supply can change when the switches connected to it are turned off.

B. Class-G Architecture

Most power amplifiers exhibit lower efficiency as $P_{\rm out}$ is decreased because their static DC power remains constant. Because a class-G PA uses multiple power supply voltages, however, lower $V_{\rm DD}$ can be used to generate lower $P_{\rm out}$ as depicted in Fig. 5. This leads to higher efficiency at low $P_{\rm out}$ because the static DC power consumption is reduced. The optimum supply voltages depend on the signal power level and the characteristics of the modulation standard (e.g., PAPR, envelope probability density function (pdf) etc.). A conventional class-G amplifier uses a lower (higher) supply voltage to generate the lower (higher) output power levels in order to achieve improved average efficiency. In other words, multiple supply voltages can be used to create multiple peaks in the overall efficiency characteristic.

The realization of class-G functionality is easier in an SCPA than in other topologies because each additional power supply voltage requires the addition of only one bottom-plate switch for

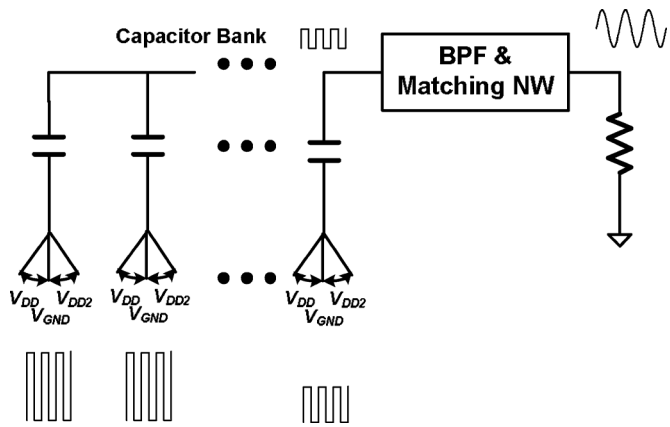


Fig. 6. Class-G SCPA architecture with ideal bottom-plate switches.

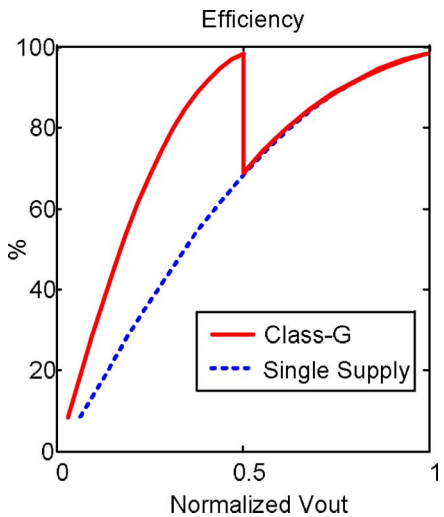


Fig. 7. Efficiency characteristics of conventional single-supply and dual-supply class-G SCPAs.

each capacitor in the array (Fig. 6). In a dual-voltage SCPA implementation, the switches are toggled between $V_{\rm DD}$ and $V_{\rm GND}$ and/or $V_{\rm DD2}$ and $V_{\rm GND}$ in accordance with the desired output power.

The efficiency characteristic of the ideal conventional class-G SCPA with two supply voltages is illustrated in Fig. 7. It shows a second efficiency peak at a smaller $P_{\rm out}$ level, which leads to higher average efficiency for an envelope-modulated signal. $V_{\rm DD}(V_{\rm DD2})$ is used at low (high) output power levels. The compelling advantage is that higher average efficiency is achieved for high PAPR signals because of the increased efficiency at low power levels where the envelope pdf of OFDM signals is highest. This switching scheme also enables power control; a change to the coding scheme could allow the PA to operate selectively from one of multiple supply voltages provided to the PA, thereby controlling the peak power that the PA would deliver.

The efficiency characteristic near the transition from the $V_{\rm DD}$ to the $V_{\rm DD2}$ supply is not continuous for a conventional class-G PA (Fig. 7). In fact, it shows no improvement compared to a conventional SCPA at normalized output voltages between 0.5 and 1. A key advantage of SC circuits is their DC-blocking capability. As a result, different unit capacitors in the array can have different DC supply voltages applied to them at the same time; i.e., both $V_{\rm DD}$ and $V_{\rm DD2}$ can be used *simultaneously* to generate different values of $P_{\rm out}$. Accordingly, it is possible to achieve the smooth efficiency characteristic shown in Fig. 8. All that is required is a change in the digital coding that controls the bottom-plate switches. The coding schemes for conventional and enhanced-efficiency class-G SCPA circuits are detailed in Tables I and II, respectively. The effective resolution is 4 bits—3 bits from the array of unary capacitors and 1 bit from the two power supply voltages. In the tables, $V_{\rm GND}$ indicates no switching, $V_{\rm DD}$ means bottom-plate switching between

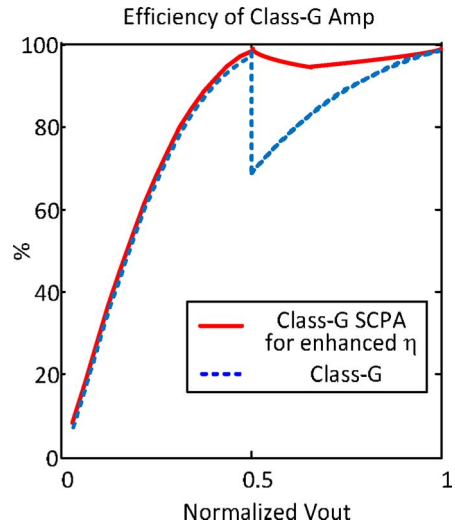


Fig. 8. Efficiency characteristics of a dual-supply class-G SCPA with conventional switching scheme and a dual-supply class-G SCPA with the enhanced efficiency switching scheme.

TABLE I
A SWITCHING SEQUENCE FOR A CONVENTIONAL CLASS-G SCPA. ONLY THE $V_{\rm DD2}$ SUPPLY IS SWITCHED WHEN MSB $=$ 1 IN GENERATING THE NORMALIZED $V_{\rm out}$ OF 0.5–1

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_{8A}	C_{8B}
0000	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0001	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0010	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0011	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0100	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0101	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0110	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}
0111	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}
1000	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
1001	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}	V_{GND}	V_{DD2}	V_{GND}
1010	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
1011	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}	V_{DD2}	V_{GND}
1100	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}	V_{GND}
1101	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{DD2}	V_{GND}
1110	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}	V_{GND}
1111	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{GND}

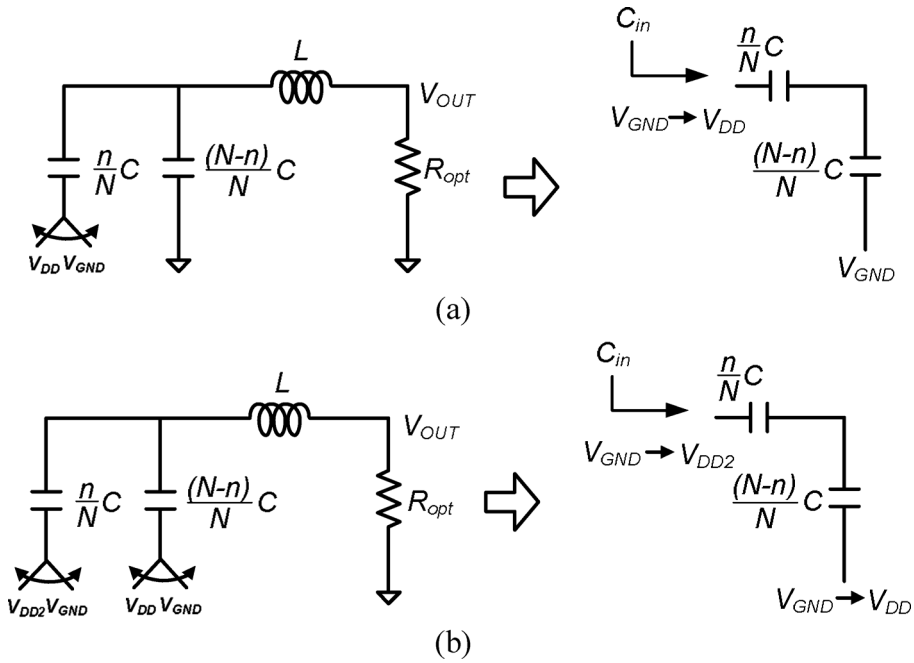


Fig. 9. Equivalent circuits for calculating of the efficiency of the improved class-G switched capacitor PA with (a) $m \leq N$ and (b) $m > N$.

TABLE II
A SWITCHING SEQUENCE FOR THE ENHANCED EFFICIENCY CLASS-G SCPA. BOTH $V_{\rm DD}$ AND $V_{\rm DD2}$ ARE SWITCHED WHEN MSB $= 1$ IN GENERATING THE NORMALIZED $V_{\rm out}$ OF 0.5–1

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
0000	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0001	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0010	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0011	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0100	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}	V_{GND}
0101	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}	V_{GND}
0110	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}	V_{GND}
0111	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{GND}
1000	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1001	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1010	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1011	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1100	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}	V_{DD}
1101	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}	V_{DD}
1110	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}	V_{DD}
1111	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD2}	V_{DD}

$V_{\rm GND}$ and $V_{\rm DD}$, and $V_{\rm DD2}$ means switching between $V_{\rm GND}$ and $V_{\rm DD2}$. In the classical scheme (Table I), only $V_{\rm DD2}$ bottom-plate switching is used for normalized output voltages between 0.5 and 1. In the enhanced-efficiency scheme of Table II, both $V_{\rm DD}$ and $V_{\rm DD2}$ bottom-plate switches are used simultaneously.

The dynamic power required to drive the SC array is analyzed carefully to determine the efficiency of the class-G SCPA with the enhanced-efficiency switching scheme. The total number of codes doubles when using a dual-supply scheme; i.e., the total number of codes is $M = 2N$ with $V_{\rm DD2} = 2V_{\rm DD}$. The number of switched capacitors is n where $0 \leq n \leq N$ and the selected code is m where $0 \leq m \leq M$.

When $m \leq N$, m is equal to n and the selected capacitors are switched between $V_{\rm DD}$ and $V_{\rm GND}$ as shown in Fig. 9(a). Thus, the output voltage and efficiency are the same as for the original SCPA as derived in (4)–(9):

$$V_{\rm out} = \frac{2}{\pi}\left(\frac{n}{N}\right)V_{\rm DD} \tag{11}$$

$$\eta_{\rm ideal} = \frac{P_{\rm out}}{P_{\rm out}+P_{\rm SC}} = \frac{1}{1+\frac{\pi}{4}\frac{(N-n)}{n}\frac{1}{Q_{\rm LOAD}}}. \tag{12}$$

When $m > N, m$ is equal to $N+n$ and n capacitors are switched between $V_{\rm DD2}$ and $V_{\rm GND}$ while $N-n$ capacitors are switched between $V_{\rm DD}$ and $V_{\rm GND}$ (Fig. 9(b)). Hence, the output voltage is:

$$\begin{aligned} V_{\rm out} &= \frac{2}{\pi}\left\{\left(\frac{n}{N}\right)V_{\rm DD2}+\left(\frac{N-n}{N}\right)V_{\rm DD}\right\} \\ &= \frac{2}{\pi}\left(\frac{N+n}{N}\right)V_{\rm DD} \end{aligned} \tag{13}$$

and the RF output power is:

$$P_{\rm out} = \frac{2}{\pi^2}\left(\frac{N+n}{N}V_{\rm DD}\right)^2\frac{1}{R_{\rm opt}}. \tag{14}$$

The dynamic power required to charge and discharge the switched capacitor array, $P_{\rm SC}$, is:

$$P_{\rm SC} = C_{\rm in}(V_{\rm DD2}-V_{\rm DD})^2 f = C_{\rm in}(V_{\rm DD})^2 f. \tag{15}$$

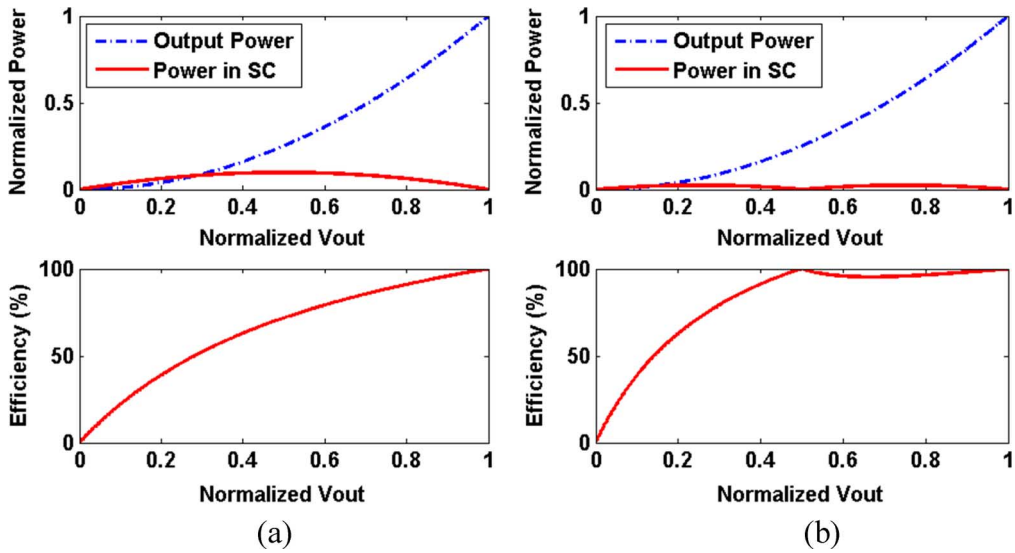


Fig. 10. Output power, dynamic power consumption, and efficiency in (a) a conventional SCPA and (b) the enhanced efficiency class-G SCPA architecture.

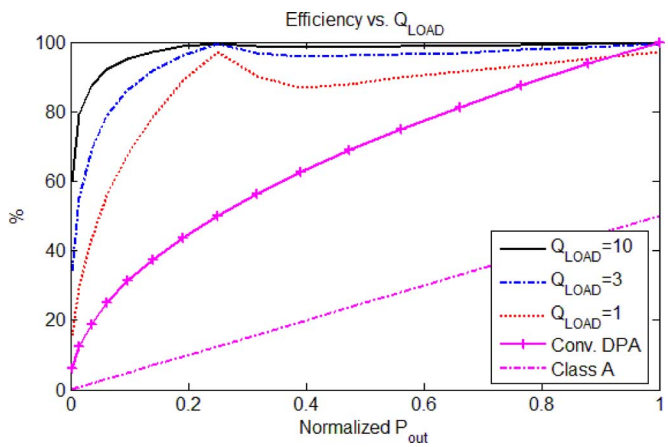


Fig. 11. Ideal efficiencies of the SCPA with the enhanced efficiency class-G switching scheme vs. $P_{\rm out}$ and $Q_{\rm LOAD}$ and for class-A and conventional DPA circuits.

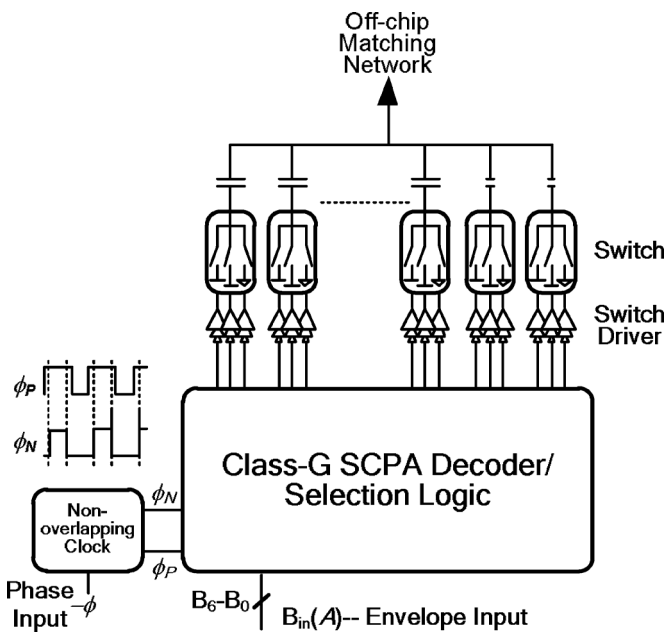


Fig. 12. Top-level block diagram of a single-ended class-G SCPA. The actual implementation is fully-differential.

Dynamic power consumption depends on the difference between the supply voltages switched in the capacitor array. Combining (14) and (15) yields the overall efficiency:

$$\eta_{\rm ideal} = \frac{P_{\rm out}}{P_{\rm out}+P_{\rm SC}} = \frac{1}{1+\frac{\pi}{4}\frac{n(N-n)}{(N+n)^2}\frac{1}{Q_{\rm LOAD}}}. \qquad (16)$$

Because the power consumption required to switch the capacitors in the array is zero at the normalized output voltages of 0.5 and 1.0 (e.g., $V_{\rm DD}$ and $V_{\rm DD2}$) as shown in Fig. 10, the class-G architecture exhibits the ideal peak efficiency at these two voltages. Moreover, the modified coding scheme reduces the dynamic power consumption for normalized $V_{\rm out}$ values greater than 0.5 compared to conventional coding, which leads to higher efficiency in that region of operation.

Efficiency characteristics for the enhanced efficiency class-G SCPA vs. $P_{\rm out}$ are plotted in Fig. 11 for several values of $Q_{\rm LOAD}$. Higher $Q_{\rm LOAD}$ values give higher efficiencies at lower $P_{\rm out}$ levels with smooth transitions between the peaks. Also shown for comparison are the efficiency characteristics of a conventional current cell-based DPA and a class-A PA. The efficiency characteristic of the modified class-G SCPA is always higher than for the alternative architectures even for low values of $Q_{\rm LOAD}$; i.e., its average efficiency is higher for any modulation envelope.

In an actual implementation, several additional losses should be considered to better estimate PAE [14]. The CMOS transistor as a switch is not ideal; it needs time to switch on and off and it also has parasitic capacitances and resistances. If the square waveform applied to the capacitor array from the switch is not ideal, it loses output power and PAE is reduced. Additionally, it needs a CMOS buffer to drive the switches connected to the

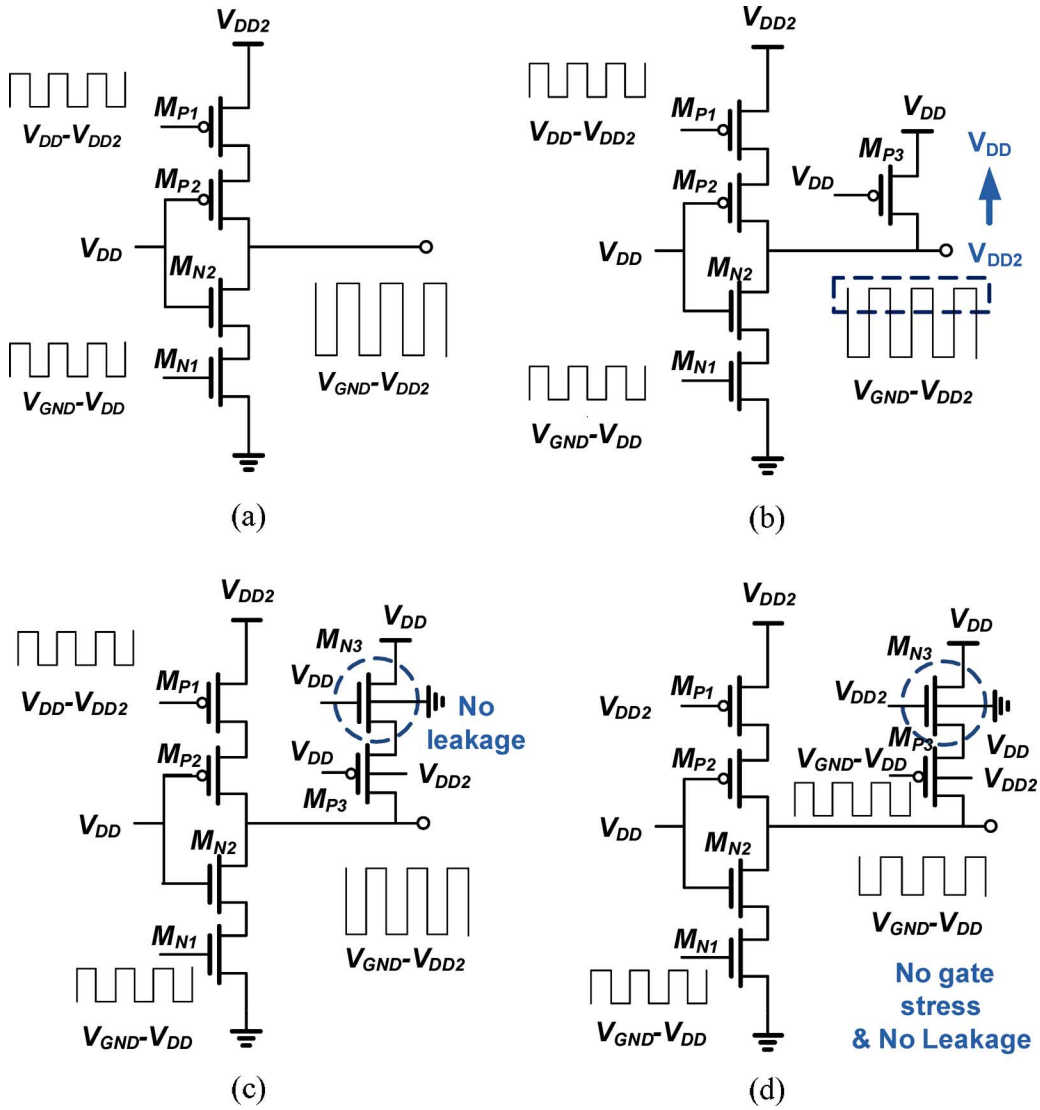


Fig. 13. Switch implementation for the class-G SCPA with voltage supplies $V_{\rm DD2}$, $V_{\rm DD}$, and $V_{\rm GND}$.

capacitors. Considering these effects, the SCPA provides higher efficiency at lower frequencies.

III. Circuit Details

A top-level block diagram of the class-G SCPA is shown in Fig. 12 (the actual implementation is fully-differential). A digital EER technique is used where code word representations of the amplitude component of the signal comprise the input to the system. This allows the SCPA to linearly amplify non-CE modulated signals using a highly-efficient switching configuration.

The signal is first transformed from a Cartesian to polar form where $A(t)$ and $\phi(t)$ represent the amplitude and phase modulated components, respectively. $A(t)$ is input as a digital code word, $B_{\rm in}(A)$, to the decoder that selects the switches to be toggled and the power supply voltage to be used in order to precisely control the signal amplitude at the capacitor summing node of the class-G SCPA. Each capacitor is either switched between $V_{\rm DD}$ and $V_{\rm GND}$, or $V_{\rm DD2}$ and $V_{\rm GND}$, or held at $V_{\rm GND}$ (i.e., not switched). $\phi(t)$ is up-converted to the desired RF carrier frequency and used to create non-overlapping clock waveforms ϕ_N and ϕ_P to minimize crowbar current [14]. These clocks are gated and buffered to drive the relatively large transistors that switch the bottom plates of the selected capacitors.

A resolution of 7 bits is achieved as follows: First, the MSB selects either $V_{\rm DD}$ or $V_{\rm DD2} = 2V_{\rm DD}$ as the power supply voltage. A 6 b capacitor array comprises the lower resolution bits: the first 4 b are 16 unary-weighted capacitors and the last two LSBs are binary-weighted. This choice trades off the larger decoder size and the complexity of a full unary-weighted array versus the larger mismatches of the capacitors, switches and drivers of the binary-weighted components. Such mismatches adversely impact both AM-AM and AM-PM performance.

NMOS and PMOS transistors make good switches in deep submicron CMOS processes. For reliability reasons, however, they should operate at a relatively small voltage, which limits the efficiency and maximum output power of CMOS PAs. To increase the maximum output power, a supply voltage greater than $V_{\rm DD}$ is desired because it minimizes the effects of losses

associated with the matching network; i.e., the impedance transformation ratio is smaller as are the proportionate losses in the matching network [4]. The cascode topology of Fig. 13(a) is popular in CMOS PA designs because it allows supplies $>V_{\rm DD}$ by dividing the high voltage stress among multiple devices [17]. The NMOS (PMOS) transistor, $M_{N1}(M_{P1})$, is driven by a logic signal between $V_{\rm GND}$ and $V_{\rm DD}$ ($V_{\rm DD}$ and $V_{\rm DD2}$) as shown.

A class-G SCPA uses two power supply voltages and additional switches. Because the second supply voltage, $V_{\rm DD2} = 2V_{\rm DD}$, is greater than the specified maximum voltage of the CMOS process, careful switch design is essential for efficient and reliable operation. In the class-G SCPA, the bottom-plate switches need to operate reliably from $V_{\rm DD2}$ and output waveforms that switch either from $V_{\rm GND}$ to $V_{\rm DD}$ or $V_{\rm GND}$ to $V_{\rm DD2}$. Considering these switching requirements in greater detail, one possible design adds M_{P3} (Fig. 13(b)) to the original circuit; this switch operates reliably and safely when the maximum output voltage is $\leq(V_{\rm DD} + |V_{tP}|)$. However, when the maximum output voltage is $>(V_{\rm DD} + |V_{tP}|)$ M_{P3} conducts harmful leakage currents through its channel because $V_{\rm SGMP3} > |V_{tP}|$ and also through the parasitic p+/n− junction diode at the drain/bulk interface. These substantial leakage currents negatively impact the efficiency, linearity and reliability of the class-G SCPA.

A novel switch design is used in two different configurations to overcome these drawbacks in switching the capacitor bottom plates from $V_{\rm GND}$ to $V_{\rm DD2}$ or $V_{\rm GND}$ to $V_{\rm DD}$, respectively, as shown in Figs. 13(c) and (d). In both operations M_{N3} is added in series with M_{P3} of Fig. 13(b). Consider the switch configuration of Fig. 13(c) when the output is switched from $V_{\rm GND}$ to $V_{\rm DD2}$. When the output is at $V_{\rm GND}$, M_{P3} is OFF because $V_{\rm SGMP3} = -V_{tN}$ whereas when the output is at $V_{\rm DD2}$, M_{N3} is OFF because $V_{\rm GSMN3} = 0$. Thus, the series M_{N3}/M_{P3} combination provides complete isolation between $V_{\rm DD}$ and the output that toggles between $V_{\rm DD2}$ and $V_{\rm GND}$. There are no voltage stress concerns with the M_{N3}/M_{P3} combination because the maximum voltage between terminal pairs is $V_{\rm DD}$.

Voltage stress concerns when the switch operates from $V_{\rm DD2}$ and the output swings from $V_{\rm GND}$ to $V_{\rm DD}$ are overcome as shown in Fig. 13(d). When the output is at $V_{\rm GND}$, the common node between M_{P3} and M_{N3} is at $V_{\rm DD}$ because M_{N3} is ON with $V_{\rm GSMN3} = V_{\rm DD}$. At the same time, M_{P3} is OFF because $V_{\rm SGMP3} = 0$. Hence, no leakage current flows. Again, the maximum voltage between terminal pairs is $V_{\rm DD}$ so there are no excessive voltage stresses. When the output is at $V_{\rm DD}$, M_{N3} and M_{P3} are ON to drive the output. As a result, there are no leakage current or excessive voltage stress concerns.

IV. Experimental Results

The new class-G SCPA is designed in a 65 nm RF Low Power CMOS process with an ultra-thick metal (UTM) layer and MIM capacitors. A microphotograph of the chip is shown in Fig. 14. For testing purposes it is flip-chip bonded to a PCB and uses an external impedance matching network that provides a higher $Q_{\rm LOAD}$ for increased efficiency. The matching network is located close to the output of the SCPA on the PCB to minimize parasitic capacitance effects that would reduce the efficiency and output power. The class-G SCPA occupies 1.4 mm × 1.2 mm including the ball array. The core area of only 220 μm × 600 μm comprises the selection logic, switch drivers, and the bottom-plate switches that control the capacitors, as well as a MIM capacitor array. The core area excluding the MIM capacitor array is covered by power supply and ground grids to minimize parasitic inductance to the switches. The selection logic and switch drivers operate from 0 V–1.4 V or 1.4 V–2.8 V whereas the bottom-plate switches operate from either 1.4 V or 2.8 V as described earlier. As an RF DAC, a resolution of 7 bits is achieved with superior linearity. As the technology feature size scales down, additional bits could be afforded as the logic and switching functions would take less area.

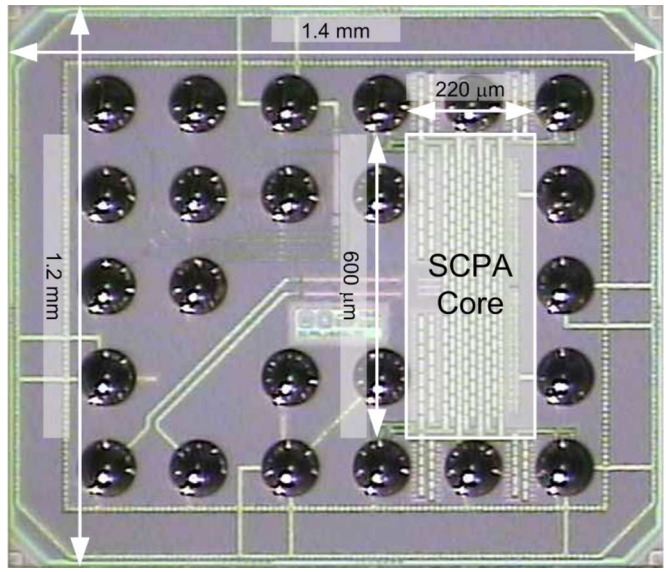


Fig. 14. Microphotograph of the class-G SCPA in 65 nm CMOS.

A. Static Measurements

The measured peak output power and efficiency are 24.3 dBm and 43.5%, respectively, at a center frequency of 2.15 GHz as shown in Fig. 15. The -3 dB bandwidth >500 MHz is consistent with the designed $Q_{\rm LOAD}$ of the band-pass matching network.

The output power of the class-G SCPA versus input code and the PAE versus output power are plotted in Fig. 16. Owing to the class-G operation, the PAE decreases by only 7% at a power backoff level of -6 dB. There is an insignificant reduction in PAE between the two efficiency peaks because of the improved class-G switching code; it behaves similarly to the single-supply SCPA below the second efficiency peak. The difference between the two efficiency peaks is caused by a greater reduction in output power when using $V_{\rm DD}$ as the switch supply relative to when $V_{\rm DD2}$ is used. (e.g., assuming $V_{\rm DD2} = 2 \cdot V_{\rm DD}$, only 25% of peak output power is generated using $V_{\rm DD}$, while the power consumption in the digital logic and buffering does

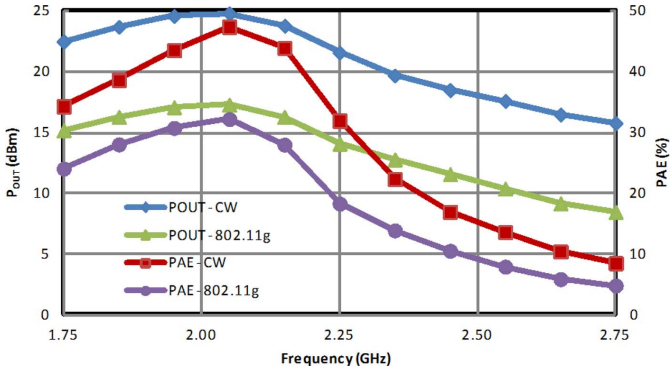


Fig. 15. Measured output power and PAE characteristics vs. frequency.

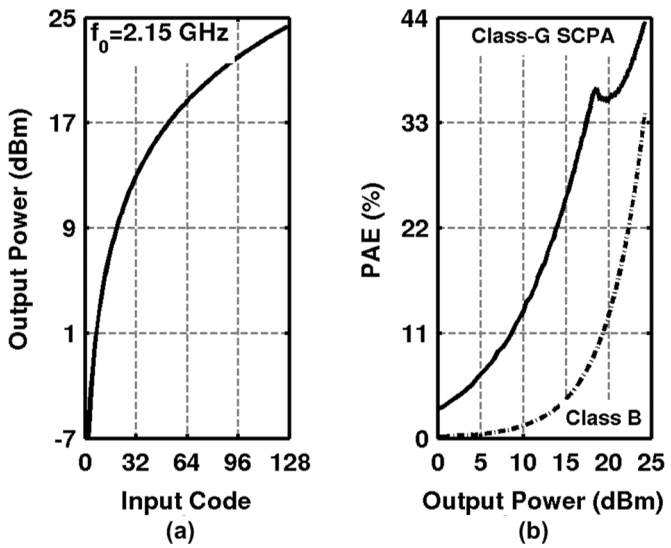


Fig. 16. Measured (a) $P_{\rm out}$ vs. envelope amplitude and (b) PAE vs. $P_{\rm out}$.

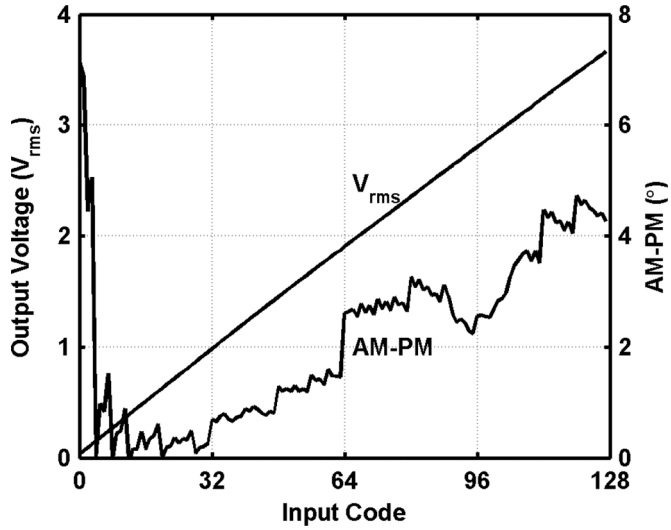


Fig. 17. Measured AM and PM characteristics vs. input code.

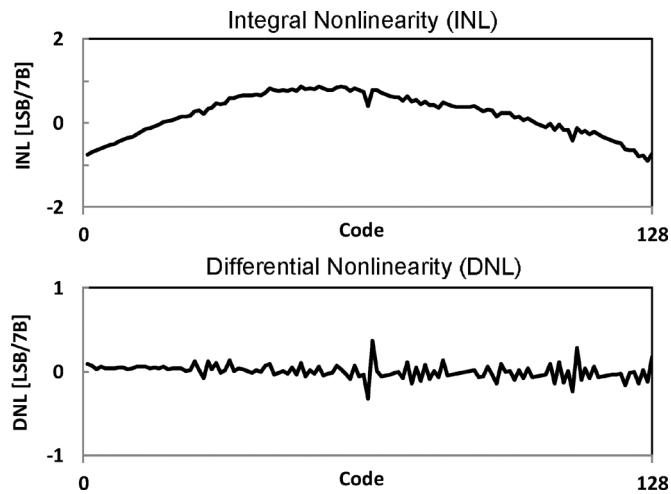


Fig. 18. Measured INL and DNL.

not reduce at the same ratio.) The measured PAE includes the power dissipation of the buffers.

The AM and PM characteristics (Fig. 17) are measured to determine the linearity of the class-G SCPA. Precision device matching techniques and careful design and layout are used to achieve excellent linearity performance at the peak output power of 24.3 dBm. Non-overlapping clocks provide higher efficiency, while suppressing crowbar current in the inverters driving capacitors [14]. It is also noted that during the non-overlapping period of the switching waveforms between ϕ_N and ϕ_P, the impedance of the capacitor array in conjunction with the OFF bottom-plate switches, is large. Because the inductor tends to maintain constant current, a voltage disturbance occurs on the top/bottom-plate of the array. The non-overlapping period between ϕ_N and ϕ_P is minimized to mitigate this concern. Essentially, this trades off linearity against efficiency. Thus, the measured peak AM-PM distortion of $\sim$7 degrees and the AM-AM distortion are significantly improved compared to the original SCPA [14].

The ripples in the AM-PM measurements of Fig. 17 arise from delay variations associated with the binary-weighted LSB switch drivers. The accuracy in this implementation is limited because of the routing parasitics that cannot be scaled exactly for every possible capacitance ratio and the timing differences that occur when a small number of unary drivers are operating with binary drivers at small output power levels. It is also important to note that there is no significant AM-AM and AM-PM shift at the center code where the supply voltage is changed in class-G architecture. This is an improvement over the traditional class-G amplifier where the sudden change of the supply voltage causes glitches and transients that increase non-linearities.

The AM-AM distortion is minimal as represented by the integral (INL) and differential (DNL) non-linearity characteristics. The measured INL is less than ± 0.9 LSB and the measured DNL is less than ± 0.4 LSB at 7 bits as shown in Fig. 18. Thus, superior amplitude linearity is achieved while generating a peak $P_{\rm out}$ of 24.3 dBm and no predistortion is needed for non-CE modulated signals such as *IEEE 802.11g*. If there is mismatch between $V_{\rm DD}$ and $V_{\rm DD2}$, predistortion or calibration may be required for higher linearity. However, monotonicity is still maintained without any predistortion or calibration leading to better linearity with the use of the proposed switching scheme

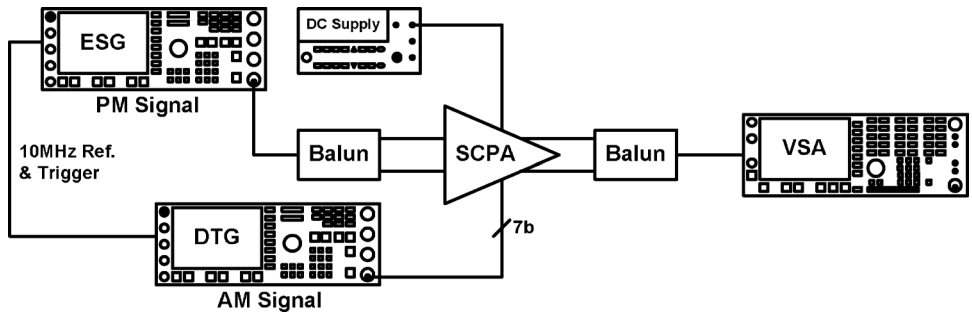


Fig. 19. The measurement set-up used to characterize the dynamic performance of the SCPA.

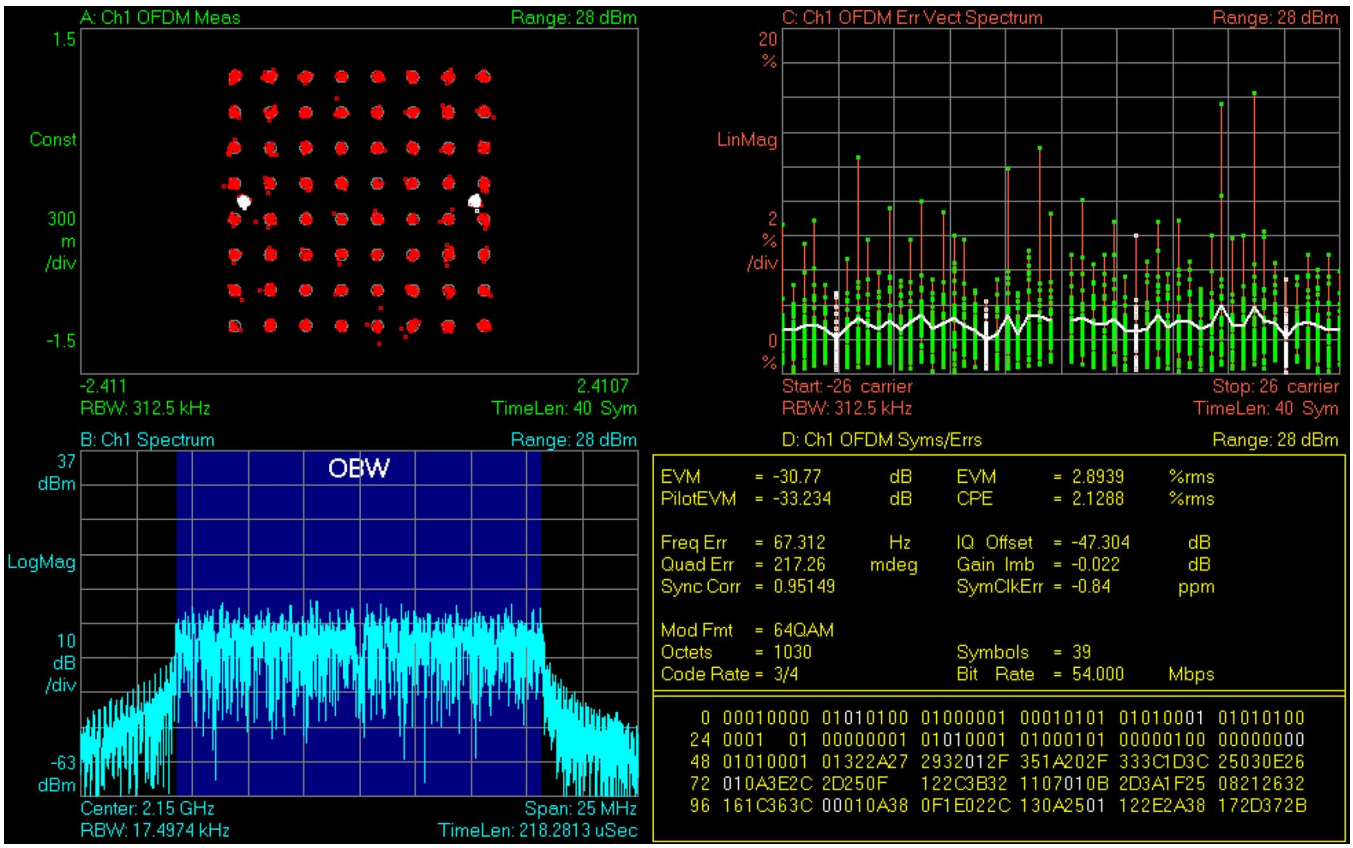


Fig. 20. Measured EVM performance for IEEE 802.11 64-QAM OFDM signals.

in the modified class-G SCPA, while providing no abrupt linearity change in amplitude and phase because the transition of V_{DD} and V_{DD2} is done continuously.

B. Dynamic Measurements

The margin-to-spectral-mask and error vector magnitude (EVM) are also characterized with the class-G SCPA amplifying non-constant envelope modulated signals. An *IEEE 802.11g* signal (e.g., 64QAM OFDM with a 20 MHz channel bandwidth) is used with the measurement setup depicted in Fig. 19. As noted above, no predistortion is used due to the superior AM-AM and AM-PM distortion performance. In the setup, a Cartesian symbol is converted to polar form; the resulting AM and PM signals are loaded onto a DTG digital pattern generator and an ESG RF vector signal generator (VSG), respectively. The signals are synchronized using a 10 MHz reference signal combined with a trigger signal from the VSG. Synchronization between the AM and PM signals is critically important in the measurement of polar architectures

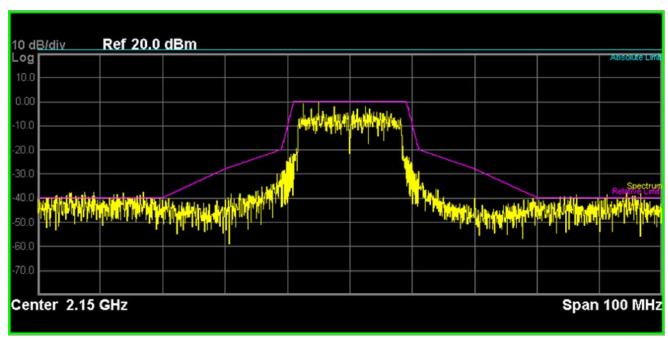
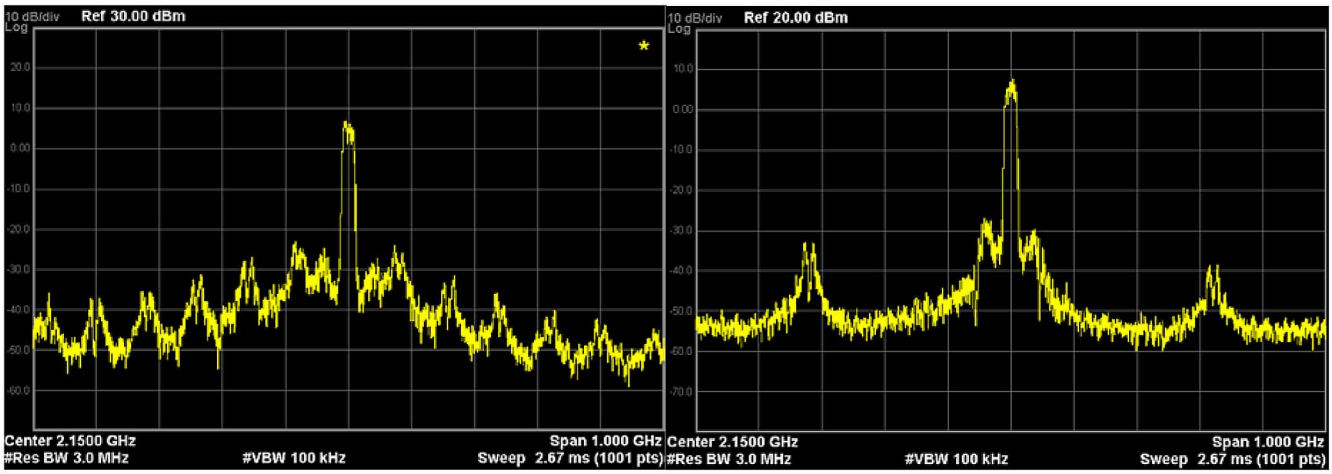


Fig. 21. Measured in- and out-of-band spectral responses relative to the *Wi-Fi* spectral mask.



(a) (b)

Fig. 22. Measured far-out output power spectra with sampling rates of (a) 80 MS/s and (b) 320 MS/s for IEEE 802.11g signals.

TABLE III
COMPARISONS OF THE CLASS-G SCPA TO PRIOR-ART CMOS POWER AMPLIFIERS

Reference	[20]	[11]	[2]	[14]	This Work
Architecture	Class-AB	DPA / Current Cell	Class-G	Switched-Capacitor	Class-G Switched-Capacitor
Process (nm)	90	130	130	90	65
Power Supplies (V)	3.3	1.2 / 2.1	3.3	1.5 / 3	1.4 / 2.8
Peak Power (dBm)	30.1	25	29.3	25.2	24.3
Peak PAE (%)	33	47	69	45	44
Avg. Power (dBm) (OFDM)	22.7	15.3	19.6	17.7	16.8
Avg. PAE (%) (OFDM)	12.4	22	22.6	27	33
Output Matching Network	On-Chip	Off-Chip	On-Chip	On-Chip	Off-Chip

because any timing mismatch significantly degrades the output spectrum and the EVM [18]. A vector signal analyzer (VSA) demodulates the output signal from the PA. The measured EVM and output power spectral density are shown in Figs. 20 and 21, respectively. The class-G SCPA achieves an excellent measured EVM of 2.9%. Although the output spectrum does violate the mask, this performance can be improved using a measurement setup with a smaller synchronization timing error and another bit of resolution. The class-G SCPA achieves an excellent average PAE of 33% with an average $P_{\rm out}$ of 16.8 dBm for *IEEE 802.11g* 64-QAM OFDM signals.

The measured far-out-of-band power spectral densities (PSD) are shown in Fig. 22. The aliased spectrum arises from the sampling of the amplitude signal; it exhibits attenuation consistent with a zero-order hold. The image in Fig. 22(a) shows a PSD attenuated by the *sinc* function at frequencies far from the center frequency. The sampling rates for the envelope signal shown in Fig. 22(a) and (b) are 80 MS/s and 320 MS/s, respectively. Thus, higher sampling rates improve the spectral purity by reducing and scattering the spectral images. Spectral purity is further improved with the use of digital signal processing techniques (e.g., a first-order hold function, dithering, etc.) [10], [19].

The shoulder in the measured in-band spectrum of Fig. 22(b) is caused by delay mismatches between the AM signal and PM signals, which arise because the signals are sourced from two separate generators. The spectrum is improved with better synchronization of the AM and PM components in the time domain [18].

An overall goal in using EER/Polar techniques is to increase the *average* efficiency of the PA:

$$\eta_{\rm avg} = \frac{P_{\rm out,avg}}{P_{\rm DC,avg}} = \frac{\int_{V_{\rm min}}^{V_{\rm max}} P_{\rm out} \cdot p(V) dV}{\int_{V_{\rm min}}^{V_{\rm max}} P_{\rm DC} \cdot p(V) dV} \tag{17}$$

where $V_{\rm max}$ and $V_{\rm min}$ are the maximum and minimum envelope voltages, respectively, and $p(V)$ is the probability density func-

tion of the envelope of the modulated signal. The class-G SCPA achieves an average PAE of 33% with an average P_{out} of 16.8 dBm while amplifying *IEEE 802.11g* 64-QAM OFDM signals.

V. Conclusion

A class-G SCPA is introduced and the theoretical underpinning is detailed. The SCPA operates at the RF frequency as an SC DAC that is modulated with the amplitude and phase information. The use of switches and capacitors to generate non-CE modulated signals enables efficient and linear amplification without using a transistor as a transconductor. The class-G SCPA achieves high power efficiency at the backoff output power level through the use of two power supply voltages. In addition, a modified class-G switching scheme is developed that uses both supply voltages simultaneously to achieve higher linearity and efficiency. The superior linearity of the class-G SCPA enables linear amplification of large PAPR signals without the need for predistortion of the baseband signal. A 7b class-G prototype in 65 nm RF CMOS achieves peak and average efficiency values of 44% and 33% while generating peak and average output power levels of 24.3 dBm and 16.8 dBm, respectively, with 64-QAM OFDM modulated signals. The class-G SCPA is compared with other recent works in Table III.

Acknowledgment

The authors thank Intel Corporation for chip fabrication and valuable measurement assistance.

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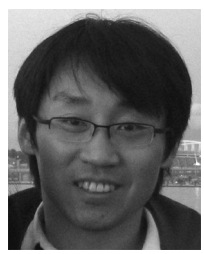

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Prior to starting his graduate education he was employed at Motorola, Plantation, FL, USA, working in cellular handset development. He interned for Intel, Hillsboro, OR, USA, from 2006 to 2007, where he worked on highly-digital transmitter architectures and CMOS power amplifiers and continued this research while a Postdoctoral Research Associate with the University of Washington. He is currently an Assistant Professor in the Electrical and Computer Engineering Department at University of Utah, Salt Lake City, UT, USA. His current research interests include low-power wireless circuits, energy scavenging, high-efficiency transmitter architectures and CMOS power amplifier design for software defined radio.

Dr. Walling has authored over 30 articles in peer-reviewed journals and refereed conferences. Recently he received the Best Paper Award at Mobicom 2012. He has also received the Yang Award for outstanding graduate research from the University of Washington, Department of Electrical Engineering in 2008, an Intel Predoctoral Fellowship in 2007–2008, and the Analog Devices Outstanding Student Designer Award in 2006.

Ofir Degani (M'99) has received the B.Sc. degree in electrical engineering and the B.A. degree in physics (both summa cum laude) in 1996, the M.Sc. degree and the Ph.D. degree in 1999 and 2005, respectively, all from the Technion–Israel Institute of Technology, Haifa, Israel. His Ph.D. research was focused on MEMS inertial sensors and electrostatic actuators.

He joined the Mobility Wireless Group, Intel, Israel, at 2006. His recent research interest includes integrated transceivers, digital transmitters and mmWave radios in CMOS technology. He has published more than 40 journal and conference papers and filed several patents.

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He has over 12 years of RFIC product design experience and is currently leading RFIC design team at Intel Corporation, Hillsboro, OR, USA, working on Wifi and Bluetooth transceivers in advanced CMOS process. Before joining Intel in 2003, he worked with STMicroelectronics and ARM. His current focus and interest is towards the architecture and circuit innovations to enable single-chip digital transceivers and SOC integration for multi-comm products.

Jacques C. Rudell (S'94–M'00–SM'09) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor, CA, USA, and the M.S.E.E. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA.

From 1989 to 1991, he was an IC Design Engineer with Delco Electronics (now Delphi), where his work focused mainly on bipolar analog circuits for automotive applications. From late 2000 to 2001, he was a postdoctoral Researcher at the University of California at Berkeley, in addition to holding consulting positions in several Silicon Valley firms. In late 2001, he joined Berkana Wireless (now Qualcomm), San Jose, CA, USA, as an Analog/RF IC Design Engineer and later became the Design Manager of the Advanced IC Development Group. From September 2005 until December 2008, Dr. Rudell was with the Advanced Radio Technology (ART) Group at Intel. In 2009, he joined the faculty as an Assistant Professor of Electrical Engineering at the University of Washington, Seattle, WA, USA.

Dr. Rudell is a member of Tau Beta Pi and Eta Kappa Nu. In 2000, he received the Demetri Angelakos Memorial Achievement Award, a citation given to one student per year by the EECS department at UC Berkeley. He received the 1998 ISSCC Jack Kilby Best Student Paper Award, was the co-recipient of the 2001 ISSCC Lewis Best Paper Award, and co-recipient of the Best Student Paper award at the 2011 RFIC Symposium. He also received an award at the 2008 ISSCC for best evening session. He was on the technical program committee for the IEEE International Solid-State Circuits Conference (ISSCC) from 2003 to 2011. He is currently the 2013 General Chair for the MTT-IMS Radio Frequency Integrated Circuits (RFIC) Symposium and Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

Dr. Rudell's research interests relate to topics in the area analog, RF, and mixed-signal systems. Recent areas of interest include RF, and mmwave circuits, in addition to interface electronic solutions towards biomedical applications. He is currently a member of NSF ERC Center for Sensorimotor Neural Engineering (CSNE) at the University of Washington.

David J. Allstot (S'72–M'72–SM'83–F'92–LF'12) received the B.S., M.S., and Ph.D. degrees from the University of Portland, Oregon State University, and the University of California, Berkeley, respectively.

He has held several industrial and academic positions including the Boeing-Egtvedt Chair Professor of Engineering at the University of Washington from 1999 to 2012 and Chair of the Department of Electrical Engineering from 2004 to 2007. In 2012 he was a Visiting Professor of Electrical Engineering at Stanford University.

Dr. Allstot has advised about 40 Ph.D. and 60 M.S. graduates, published 300 papers, and received several awards including the 1980 IEEE W.R.G. Baker Award, 1995 and 2010 IEEE Circuits and Systems Society (CASS) Darlington Award, 1998 IEEE International Solid-State Circuits Conference (ISSCC) Beatrice Winner Award, 2004 CASS Technical Achievement Award, 2005 Semiconductor Research Corp. Aristotle Award, 2008 Semiconductor Industries Assoc. University Research Award, and 2011 CASS Mac Van Valkenburg Award. His service includes: 1990–1995 Assoc. Editor/Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, 1990–1993 Member of Technical Program Committee of the IEEE Custom IC Conference, 1994–2004 Member, Technical Program Committee, IEEE ISSCC, 1996–2000 Member, Executive Committee and Short Course Chair of ISSCC, 2001 and 2008 Co-General Chair of ISCAS, 2006–2007 Distinguished Lecturer, IEEE Solid-State Circuits Society, and 2009 President of CASS.