A Fully Integrated, Regulatorless CMOS Power Amplifier for Long-Range Wireless Sensor Communication

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***Abstract*—This paper presents a CMOS power amplifier (PA) system designed with the explicit goal of customizing a high-output power transmitter for sensor applications, where the supply voltage from an energy storage element is often time varying. The PA is intended for use in a long-range sensor transceiver and can operate directly off a super-capacitor source. A constant output-power, regulatorless, series power-combined PA with a fully integrated tunable matching network is implemented in an attempt to eliminate all energy losses associated with a high-current voltage regulator. The PA monitors the output voltage at the off-chip antenna and digitally modulates the PA load impedance to maintain a constant target output power as the super-capacitor discharges. The PA system, integrated in a 90-nm CMOS process, has a peak output power of 24 dBm with an efficiency of 12% at 1.8 GHz, making it suitable for sensor data communication over distances of several hundred meters. As the PA supply varies from 2.5 to 1.5 V, the power control loop maintains a constant output power with an accuracy of $\pm$0.8 dB.**

***Index Terms*—CMOS, long-range sensor transmitter, power amplifier, power control-loop, sensor network, tunable matching network.**

I. Introduction

THE realization of single-chip integrated radios, dating back to the 1990s, has made a profound impact on many consumer applications, most notably the modern smart phone. Every improvement in silicon technology seems to motivate entirely new radio applications from wireless key entry, to high-frequency, short-range, mm-wave communication systems. Some of the early work on highly integrated CMOS radios focused on short-range radios because of the lower performance associated with these front ends with respect to sensitivity, selectivity, and power output [1], [2]. Later, integrated CMOS radios extended their range with high-performance cellular transceivers for mobile phone applications [3], [4].

In parallel with addressing the consumer handset market, there has been interest in using single-chip silicon radio front ends for sensor data communication [5]–[8]. The early wireless sensors utilized mesh networks to report data; employing numerous ultra-low-power radios with cell sizes of less than a few meters between adjacent nodes. For long-distance sensor transmission of several kilometers, data must hop through hundreds, if not thousands, of individual nodes along the mesh. This is convenient for applications requiring a dense coverage of sensors for data collection. Several advantages are afforded by the short-range transmission found in a mesh network. First, the small cell sizes (several meters in diameter) allow frequency reuse, thereby enabling multiple sensor-to-sensor data links within a small geographical area. The second advantage of collaborative mesh networks, from a theoretical perspective, relates to maximizing transmission energy efficiency on a bit/joule basis by optimizing the node-to-node transmission distance [8] (depending on the path-loss conditions, and transceiver characteristics). However, several practical considerations add significant complexity to this class of networks. Issues such as network self-assembly [9], receiver wake-up time synchronization [10], scheduling between various cells, and rerouting around errant nodes, have proven to be a challenge for long-distance wireless sensor communication.

Any advantage with respect to energy efficiency in short-range mesh networks assumes an optimal and uniform spacing between sensor nodes. This assumption of uniformity between nodes has proven problematic for many applications where deployment is rendered in an uncontrolled and random fashion. Sensor nodes used in barrier coverage applications to detect intruders at the boundary of a battlefield, border, or coastline serve as examples. Situations arise where rapid deployment of the "barrier coverage mesh networks " becomes necessary by dropping sensor nodes via aircraft or artillery ordinance delivery systems. Accordingly, the position of each node, relative to one another, is random and influenced by many factors including wind and terrain [11]. To ensure adequate barrier coverage, spatial redundancy is often achieved through the expense of utilizing extra sensor nodes. Moreover, complex network self-assembly [12] and node redundancy further erode the energy efficiency advantage of mesh networks when long-range communication becomes necessary.

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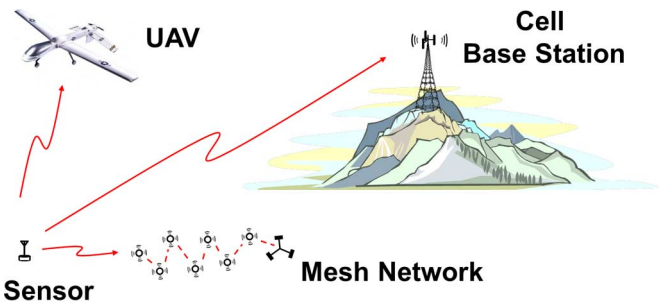

Fig. 1. Concept of long-range sensor communication and "network-scavenging."

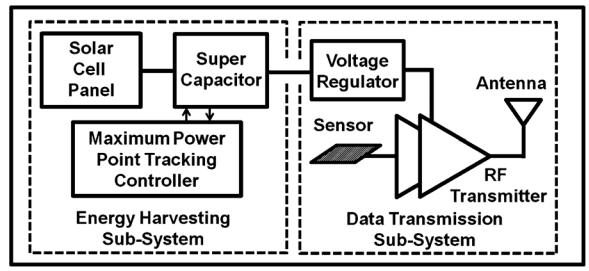

Fig. 2. High-level system block diagram for a wireless sensor transmitter.

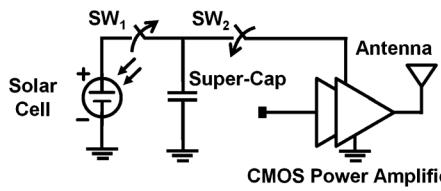

Fig. 3. CMOS power amplifier for long-range sensor TX.

In contrast, single-hop long-range communication would reduce issues surrounding nonuniform coverage by communicating directly with a base station. A small-form factor transceiver that enables long-range communication has the benefit of addressing many sensor data applications which might be challenging to realize using a collaborative mesh network. Measurements in relatively remote locations or applications where a low density of sensor coverage is sufficient remove much of the motivation for short-range transceivers that are coupled with the sensing device. Examples could range from remote monitoring of temperature, humidity, precipitation, and rainfall levels to data collection for global warming research or perhaps homeland security applications. The primary advantage of an extended node range is the potential ability to exploit existing cellular, WiFi, and PAN network infrastructure, thus conceivably obtaining coverage in any urban environment. In addition, if a sensor radio for long-distance communication is realized in CMOS, highly programmable radio front ends with multistandard capability could be realized. This implies that a sensor node could find the most available and energy-efficient access point, even including collaborative mesh networks. Thus, as shown in Fig. 1, a single sensor node could be randomly placed in virtually any environment and left to "network-scavenge" for the closest and most energy efficient access point.

Although many issues spanning a broad selection of disciplines (including networking, digital signal processing, energy scavenging, and communications theory) would need to be addressed to realize the vision of a long-range sensor transceiver, this paper focuses on one of the most challenging aspects of the front-end transceiver electronics—the PA. Techniques for cellular (long-range) and sensor (short-range) PAs have developed independently over the past decade due to the significantly different system specifications (power levels) as well as system architectures (energy sources). The long-range sensor PA [13] proposed in this work lies at the intersection of these two fundamentally different radio front ends.

Any autonomous sensor transmitter can be separated into two basic subsystems, as shown in Fig. 2—the energy harvesting subsystem (EHS) [14]–[16] and the data transmission system (DTS). This paper explores techniques towards improving the DTS efficiency. The block diagram of the proposed sensor transmitter is shown in Fig. 3. The system comprises a solar cell, super-capacitor, switches $(\mathrm{SW}_1, \mathrm{SW}_2)$, and a CMOS PA. During the charging phase, solar energy is harvested by a solar cell and stored on a super-capacitor via switch SW_1. As soon as sensor data is available, switch SW_2 closes to connect the super-capacitor directly to the PA. In order to maximize the super-capacitor energy utilization, while concurrently maintaining constant output power, this work proposes a PA with a tunable matching network (TMN). The sensor PA also includes a fully integrated control loop, which monitors the output power and modulates the TMN in response to variations in the super-capacitor voltage.

The rest of the paper is organized as follows. Section II highlights the important differences between transmitters designed for long-range and short-range applications. Following this, Section III describes the desired characteristics of a long-range Sensor PA. The TMN is described in Section IV. The circuits in the PA signal path and power control feedback path are discussed in Section V. Experimental results and a comparison with prior-art in tunable matching networks are presented in Section VI. The paper concludes with some summary comments in Section VII.

II. Power Amplifiers for Long-Range/ Short-Range Transmitters

To highlight the challenges involved in the long-range sensor PA, the important differences between cellular and sensor PAs are described next.

A. Power Levels

Power amplifiers for handset applications face several challenges with respect to realization in CMOS technologies. A major difficulty, exacerbated in low-voltage CMOS processes, is achieving the high output power required by many commercial PA applications. As an example, the GSM standard, which supports communication between mobile handsets and cell base stations potentially several kilometers away, requires the PA output power to be as high as 1 W (+30 dBm) [17], [18]. While

amplifiers designed for typical mesh-based sensor systems deliver output power on the order of 1–10 mW [19], the proposed sensor PA needs to be designed to support cellular-like power outputs.

B. Energy Source

An additional distinction between cellular and sensor transmitters relates to the PA's power source. In cellular transceivers, the PA typically operates directly from a rechargeable lithium-ion battery [18]. Although the voltage may change by 20% as the battery discharges, frequent battery recharge is acceptable. In contrast, a sensor radio must operate as a fully autonomous unit, requiring some form of energy scavenging (solar [16], vibrational [16], [20]) coupled with an energy storage element, typically a super-capacitor [21]. The voltage across a super-capacitor, in contrast to a relatively constant battery voltage, decreases under normal transceiver operation. A key challenge with the proposed sensor PA relates to designing power efficient transceiver circuits that are unique to the method of energy acquisition, storage, and utilization in sensor systems.

III. Desired Characteristics of This Sensor PA

Two important features of an ideal long-range sensor PA are long active time and high transmitter efficiency. The system-level aspects that relate to the aforementioned characteristics are discussed in the following section.

A. Maximizing Sensor Active Time: Power Combiner Architecture

The active time of a sensor refers to the duration of time over which the supply voltage provided by the super-capacitor is sufficient to transmit data at a desired power level. For example, a sensor TX that can transmit data for a supply voltage ranging from 2.5 to 1.5 V has a higher active time compared with one that operates only over the range of 2.5 to 2.0 V. For this implementation, the PA was designed to operate at as low as 1.5 V.

With the goal of leveraging existing network infrastructure for sensor communication, the upbanded version of GSM, PCS 1900 was used for the initial PA design. Delivering output power on the order of 1 W from a 1.5-V supply makes the power-combined implementation [18], [22] attractive. Ideally, in order to deliver a combined power output $\mathrm{P_{OUT}}$, an "N" element series power-combined PA requires each PA stage to deliver only $\mathrm{P_{OUT}}/N$ output power.

B. Maximizing Efficiency: Switching PA and Regulatorless Power Control

In order to optimally utilize the energy stored in the super-capacitor, it is important to maximize efficiency at both the circuit and system level. The high-power PA output stage holds a dominant share in the total power consumption of the sensor TX; thus, a high-efficiency PA can significantly improve the overall transmitter efficiency. Switching PAs can theoretically achieve higher power efficiency than linear PAs but are limited to transmitting signals using constant-envelope modulation. However, the constant-envelope Gaussian mean shift-keying (GMSK) modulation associated with GSM allows the use of a Class-E switching PA topology [17].

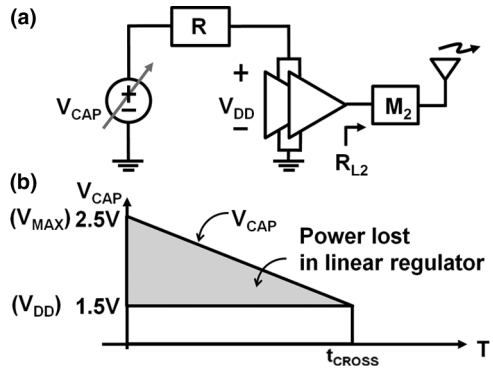

Fig. 4. (a) Sensor PA system with voltage regulator and fixed matching network. (b) Power loss due to voltage regulator in the supply path.

At a system level, it is important to consider efficient techniques to maintain a constant output power from the sensor PA as the super-capacitor discharges. Voltage regulators are commonly used to minimize fluctuations from a battery or supply line for a wide range of loading conditions. These regulators can be categorized either as switch-based regulators, such as a boost–buck converter, or as linear low dropout (LDO) regulators. The general approach to regulating the PA supply using a regulator is shown in Fig. 4(a). High-efficiency switching regulators [23] have been proposed for ultra-low-power body-area network sensors. For this class of applications, the efficiency and spectral output of the regulator is relaxed. However, in cellular applications, interaction between the regulator clock $(\mathrm{F_{SR}})$ and the RF carrier frequency $(\mathrm{F_{RF}})$ of the switching PA could produce unwanted spurious emission at $\mathrm{F_{RF}} \pm \mathrm{F_{SR}}$, ultimately leading to both in-band and out-of-band spectral mask violations. In addition, both the quality factor and value of inductance used in switching regulators typically requires the use of off-chip inductors, which runs contrary to the goal of integration. In contrast, linear regulators avoid the issue of spur generation, but suffer from a comparatively lower efficiency, which is particularly true when the supply voltage has a large variation. To demonstrate the inefficiency of such a regulator in the Sensor TX, the voltage across the super capacitor, while a constant current is being drawn by the load, is shown as a function of time in Fig. 4(b). At the beginning of the transmitter operation, a large voltage drop exists across the linear regulator, introducing an additional power loss directly proportional to the average current flowing through the PA and the difference between the unregulated voltage $(\mathrm{V_{CAP}})$ and the regulated PA supply voltage $(\mathrm{V_{DD}})$. The highlighted section in Fig. 4(b) indicates the power lost in the linear regulator as the super-capacitor discharges, which ultimately degrades the overall transmitter efficiency. Equation (1) describes the reduction in overall transmitter efficiency (η) as a function of the ratio $\mathrm{V_{MAX}}/\mathrm{V_{DD}}$ (derivation in Appendix I), where $\mathrm{V_{MAX}}$ is the fully charged super-capacitor voltage.

$$\eta = \frac{2}{1 + \frac{\mathrm{V_{MAX}}}{\mathrm{V_{DD}}}}. \tag{1}$$

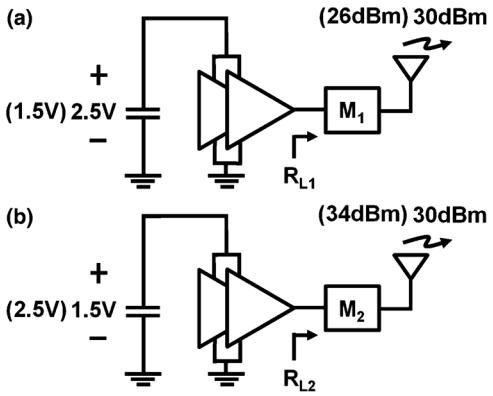

Fig. 5. Unregulated super-capacitor powered PA with fixed matching networks. (a) M_1 designed for 30-dBm output power at 2.5 V. (b) M_2 designed for 30-dBm output power at 1.5 V.

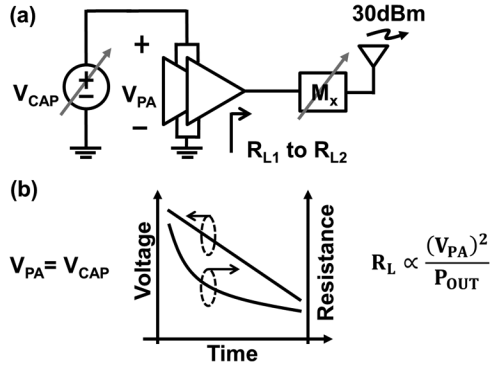

Fig. 6. (a) Regulatorless approach with the super-capacitor connected director to the PA. (b) Plot of supply voltage $\mathrm{V}_{\mathrm{CAP}}$ and tuned load resistance as a function of time.

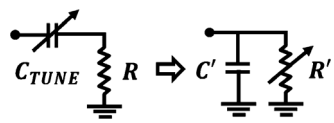

Fig. 7. Series to parallel *RC* transformation.

From (1), it can be noted that for a $\mathrm{V}_{\mathrm{MAX}} = 3\mathrm{V}_{\mathrm{DD}}$, the maximum achievable transmitter efficiency is limited to 50% due to the power lost in the linear regulator. Thus, a regulatorless approach in the sensor PA is desirable from an efficiency standpoint.

Eliminating the regulator and connecting the sensor PA directly to the super capacitor makes the design of the output matching network quite challenging. The dynamic nature of the supply voltage for sensor PAs leads to a unique relationship between the PA matching network and the variable super capacitor voltage, which is best understood by considering a GSM +30-dBm transmit signal. For example, consider the two extreme voltages on the super capacitor: the first being when the super capacitor is fully charged to $\mathrm{V}_{\mathrm{MAX}}$, and the other when the storage element has discharged to a value $\mathrm{V}_{\mathrm{MIN}}$. By applying realistic $\mathrm{V}_{\mathrm{MAX}}$ and $\mathrm{V}_{\mathrm{MIN}}$ values of 2.5 and 1.5 V, respectively, the impact of this supply variation on the PA performance can be explored. If a matching network M_1 is designed for maximum output power (+30 dBm) with a $\mathrm{V}_{\mathrm{DD}} = \mathrm{V}_{\mathrm{MAX}}$ (2.5 V), as shown in Fig. 5(a), then as the capacitor discharges to $\mathrm{V}_{\mathrm{MIN}}$ (1.5 V), the PA output power would drop to +26 dBm; this assessment assumes a switch-based PA in which the output power, $\mathrm{P}_{\mathrm{OUT}}$, is proportional to $\mathrm{V}_{\mathrm{DD}}^2$. Conversely, if a matching network M_2 is designed for a $\mathrm{P}_{\mathrm{MAX}}$ (+30 dBm) at $\mathrm{V}_{\mathrm{MIN}}$ (1.5 V), as shown in Fig. 5(b), then the output power would now be too high (+34 dBm) when the capacitor is fully charged (2.5 V).

To maintain constant output power, a TMN that tracks the large variation in the supplied super-capacitor voltage is proposed. As shown in Fig. 6, when the super-capacitor discharges and the supply voltage $(\mathrm{V}_{\mathrm{CAP}})$ decreases, in order to maintain a constant output power, the PA load has to scale down at a rate proportional to $\mathrm{V}_{\mathrm{DD}}^2$. The TMN (M_X) transforms the fixed antenna impedance into a variable load, R_L, at the PA output over the range of supply voltage. The circuit details of the fully integrated TMN are described next.

IV. Tunable Matching Network

The desired function of the TMN is to modulate the real part of the PA load impedance. Furthermore, it is critical to maintain the PA output resonant tuning as close to the carrier frequency as possible. The realization of the TMN implemented in this chip is best described by starting with a series *RC* as shown in Fig. 7. The series *RC* network with $Q = 1/\omega RC_{\mathrm{TUNE}}$ can be transformed into an equivalent parallel *RC* network at frequency ω_c; this transformation is defined by

$$R' = R(1+Q^2) = R\left(1 + \frac{1}{(\omega_c R C_{\mathrm{TUNE}})^2}\right) \tag{2}$$

$$C' = C_{\mathrm{TUNE}}\frac{Q^2}{1+Q^2} = \frac{C_{\mathrm{TUNE}}}{1+(\omega_c R C_{\mathrm{TUNE}})^2}. \tag{3}$$

To demonstrate the implications of the above equations and explore the impact of variable C_{TUNE}, consider R and ω_c set to 7 Ω and $(2\pi \times 1.9\ \mathrm{Grad/s})$, respectively. Fig. 8 shows R', C', $\frac{\partial C'}{\partial C_{\mathrm{TUNE}}}$ and $\frac{\partial R'}{\partial C_{\mathrm{TUNE}}}$ as C_{TUNE} changes from 3 to 20 pF. Qualitatively, as C_{TUNE} increases, the Q of the *RC* network reduces and R' asymptotically approaches R. For this particular example, R' varies by as much as 12× over the swept range of C_{TUNE}. However, for large values of C_{TUNE}, the slope of R', shown in Fig. 8(b), reduces.

Consider the case where C_{TUNE} is modulated by a factor α from $C_{\mathrm{TUNE\text{-}1}}(Q_1)$ to $C_{\mathrm{TUNE\text{-}2}}(Q_2)$ in order to obtain a 5× variation in the shunt resistance. From (2), it can be shown that

$$\frac{R_2'}{R_1'} = 5 = \frac{1+Q_2^2}{1+Q_1^2} = \frac{1+\alpha^2 Q_1^2}{1+Q_1^2}. \tag{4}$$

To obtain insight on the relation between the tuning range and Q_1, (4) can be expressed as

$$\alpha = \sqrt{\frac{4}{Q_1^2} + 5}. \tag{5}$$

As shown in Fig. 8(a), a low Q_1 is desired in circuits where $(R')_{\min} \sim R$. However, from (5), one observes that reducing Q_1 necessitates a larger α (capacitance tuning range) in order to obtain the same shunt resistance variation. Thus, on the higher side, the value of C_{TUNE} is constrained by α and the target R' variation. For $Q < 0.5$, additional increases in the value of

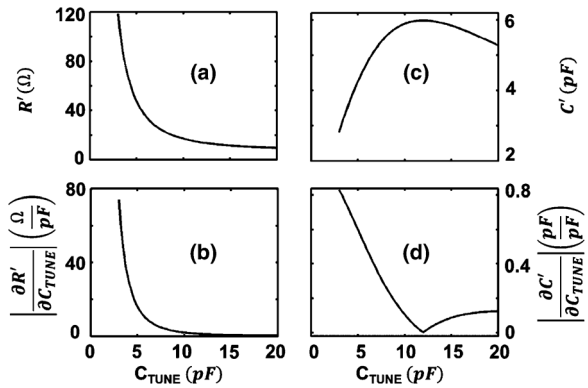

Fig. 8. (a) Shunt resistance (R'), (b) derivative of shunt resistance, (c) shunt capacitance (C'), and (d) derivative of shunt capacitance versus tuning capacitance, $C_{\rm TUNE}$.

$C_{\rm TUNE}$ achieve a negligible change in R'. As an example, if $Q_1 = 0.5$, a $5\times$ R' variation can be obtained with $\alpha = 4.3$ ($Q_2 = 2.3$).

Next, to select the optimal tuning range of $C_{\rm TUNE-1}$, which minimizes the variation in C', consider the derivative C' as a function of $C_{\rm TUNE}$. From (3) the following expression is obtained:

$$\frac{\partial C'}{\partial C_{\rm TUNE}} = \frac{1-(\omega C_{\rm TUNE}R)^2}{\left(1+(\omega C_{\rm TUNE}R)^2\right)^2}. \tag{6}$$

From (6) and Fig. 8(d), one notes that for $Q = 1$, $\partial c\prime/\partial c_{\rm TUNE} = 0$. In Fig. 8(c), C' is relatively independent of $C_{\rm TUNE}$ around this operating point. Thus, if the TMN is designed with $Q_1 < 1 < Q_2$, the variation in the resultant shunt capacitance is minimized.

Consider the example presented earlier where the $5\times$ resistance variation was obtained with $Q_1 = 0.5$ and $Q_2 = 2.3$. From Fig. 8(c), the maximum C' is obtained when $Q = 1$.

$$Q = 1, \qquad C' = C_{\rm TUNE}\frac{Q_3^2}{1+Q_3^2} = 0.5\,C_{\rm TUNE}. \tag{7}$$

For $C_{\rm TUNE}$ modulated within a tuning range of $\{C_{\text{TUNE-1}}(Q = 0.5), C_{\text{TUNE-2}}(Q = 2.3)\}$, the shunt capacitance varies from

$$\begin{aligned} Q_1 = 0.5, \quad C' &= C_{\text{TUNE-1}}\frac{Q_1^2}{1+Q_1^2} = 2\,C_{\rm TUNE} * 0.2 \\ &= 0.4C_{\rm TUNE} \end{aligned} \tag{8}$$

$$\begin{aligned} Q_2 = 2.3, \quad C' &= C_{\text{TUNE-2}}\frac{Q_2^2}{1+Q_2^2} = \frac{1}{2.3}C_{\rm TUNE} * 0.84 \\ &= 0.36C_{\rm TUNE}. \end{aligned} \tag{9}$$

Equations (7)–(9) reveals that a TMN designed with a $0.5 < Q < 2.3$, produces a desired $5\times$ variation in the shunt resistance while restricting the variation of the shunt capacitance to less than 30%, helping to reduce any variation in the resonant frequency as the shunt resistance changes.

The TMN, which relies on the discussed principles of series-to-parallel transformations, consists of an integrated transformer along with a tunable series capacitance, $C_{\rm TUNE}$, implemented with a switch-capacitance bank. A simplified circuit model of the TMN is shown in Fig. 9. If the primary and secondary capacitances, C_P and C_S, are selected to resonate with the leakage inductance of the primary and the self-inductance of the secondary at the carrier frequency, $\omega_{\rm RF}$, then (as derived in Appendix II) the input impedance of the transformer is described by

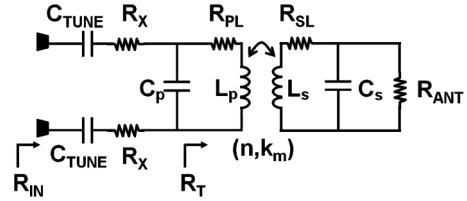

Fig. 9. Half of the power combiner used to model the tunable matching network (TMN).

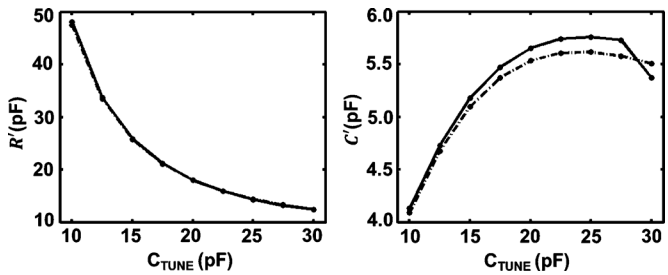

Fig. 10. $\boldsymbol{R'}$ and $\boldsymbol{C^{prime}}$ variation as a function of the tuning capacitance.

$$R_T = \left\{1+Q_L^2\right\} * (R_{\rm TXFRM} + R_{PL}) \tag{10}$$

The load on the PA, which now simplifies to R_T in series with R_X (resistance of the switch) and $C_{\rm TUNE}$, can now be analyzed using the series-parallel transformation described earlier. The input impedance of the TNM ($R_{\rm IN}$), or the effective load on the PA, is then controlled via $C_{\rm TUNE}$,

$$R_{\rm IN} = \left[1+Q_C^2\right] * (R_T + 2R_X) \tag{11}$$

where

$$Q_C = \frac{1}{\left\{\omega_{\rm RF}\left(\frac{C_{\rm TUNE}}{2}\right)(R_T+2R_X)\right\}}. \tag{12}$$

In Fig. 10, the model derived for input admittance, (11) and (12), is compared with simulation results using an extracted model of the power combiner laid out in the 90-nm TSMC process. These plots show close agreement between the model and the simulated admittance values. As shown in Fig. 10, by varying $C_{\rm TUNE}$ from 10 to 30 pF, approximately 400% variation in the parallel equivalent resistance is achieved, while the capacitance variation is limited to less than 40%.

A key challenge with respect to realizing the TMN in CMOS is the implementation of $\rm C_{TUNE}$. This capacitor can be realized as either a varactor or a bank of discrete capacitors. Varactor-based tuning techniques [24], [25] allow for high-capacitor resolution, and the value of capacitance can be modulated

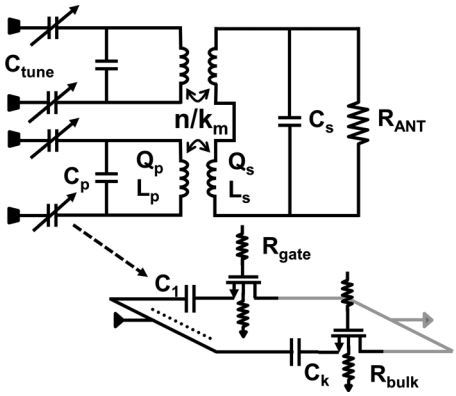

Fig. 11. Series capacitance-bank-based TMN shown in relation to the power combiner.

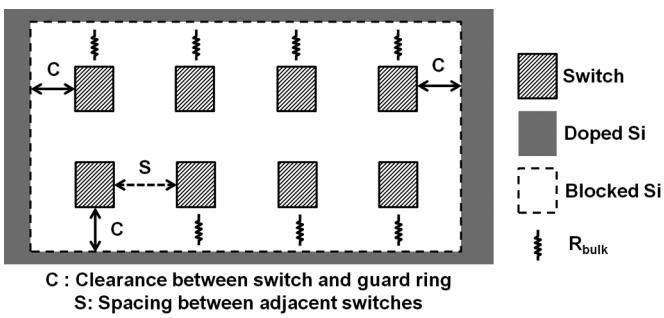

Fig. 12. Layout of the TMN switch on high-impedance substrate.

by an analog voltage control loop. However, the addition of a varactor to the output of a switching Class-E PA adds a highly nonlinear element to the signal path, potentially contributing to spectral regrowth and degradation of the modulation spectrum. For the implementation shown in Fig. 11, a metal–insulator–metal (MiM) based capacitor bank was used to realize C_{TUNE}.

Voltage excursions greater than $2.5\mathrm{V_{DD}}$ at the TNM input make the implementation of the switches in the capacitor bank challenging. To address reliability issues of these switches, a bootstrap technique was employed by attaching a resistor, R_{GATE} and R_{BULK} to the source and bulk device terminals, respectively. The addition of R_{GATE} is straightforward, with a physical resistor placed in series with the switch gate. However, the realization of R_{BULK} in standard CMOS relies on increasing the distributed resistance of the substrate in the immediate vicinity of the switch. The switches in the capacitor bank exploit the high-resistivity property of the native silicon to realize a high-impedance path between the device bulk terminal and ground [26]. The layout of the capacitor bank switches shown in Fig. 12 is similar to the T/R switch implemented in [27].

V. PA Circuit Implementation

A block diagram of the sensor PA is shown in Fig. 13. The power-combined PA architecture utilizes two parallel signal paths. The PA consists of an injection locked *LC*-oscillator based predriver (DR) stage cascaded with a pair of common-source switching devices in the output driver stage, followed by the TMN and an on-chip power combiner. A

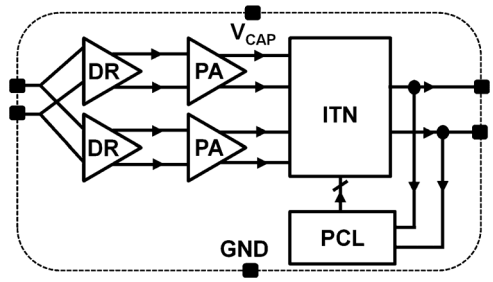

Fig. 13. Block diagrams of the long-range sensor transmitter.

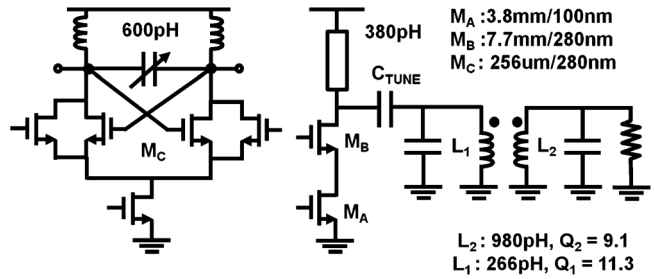

Fig. 14. Injection-locked oscillator driver and PA output stage.

digital power-control feedback loop, which digitally modulates the switches in the TMN, is also integrated with the PA core. Further design details of the individual blocks are described in the following section.

A. PA Forward Path

1) Switching PA: Switch-based PAs operate the active device in an ON–OFF fashion, in contrast to a linear amplifier which utilizes an active device as a transconductance stage, in order to achieve higher efficiency. The PA implemented for this sensor TX most closely matches the traditional Class-E topology in which the load matching network is designed to meet a zero-voltage switching (ZVS) condition [28]. However, unlike a traditional Class-E PA which utilizes a series *LC* filter at the output, this PA implements a parallel resonant network with a transformer and series tuning capacitance to realize the TMN; this is shown in Fig. 14.

2) Injection Locked Predriver: The PA predriver stage exploits the constant-envelope nature of a GMSK signal by using an injection-locked oscillator (ILO), which drives the gate of the output stage rail-to-rail [17]. The ILO is designed with a free running frequency $\mathrm{F_{FREE}}$ and lock range $\mathrm{F_{LOCK}}$ such that

$$\mathrm{F_{FREE}} - \mathrm{F_{LOCK}} < \mathrm{F_{RF}} < \mathrm{F_{FREE}} + \mathrm{F_{LOCK}}. \qquad (13)$$

B. PA Feedback Path and Power Control Loop

The block diagram and algorithm for the power-control loop (PCL) are shown in Figs. 15 and 16, respectively. The on-chip logic requires only two explicit external control signals: CAL and $\mathrm{V_{REF}}$. CAL is a trigger signal to initiate the operation of the PCL while $\mathrm{V_{REF}}$ is an external reference voltage, which maps to a desired output power level. The PCL includes a three-bit counter that controls the switches in the TMN. A peak detector detects the voltage swing at the antenna and maps it to a voltage $\mathrm{V_{FB}}$, which goes to the feedback loop. The

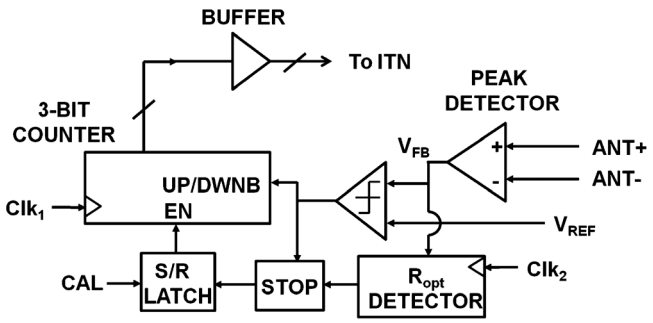

Fig. 15. Power control loop block diagram.

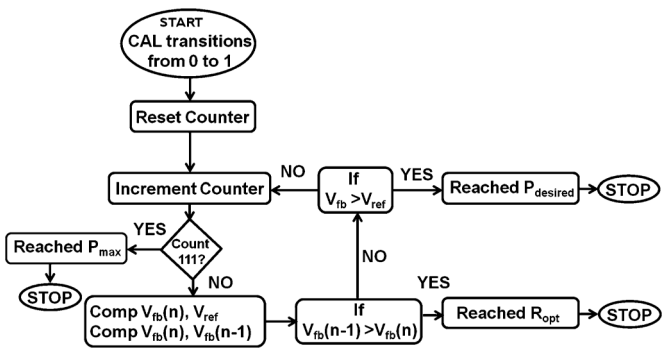

Fig. 16. Algorithm for regulatorless power control loop.

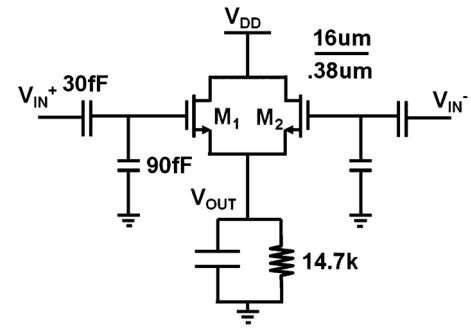

Fig. 17. Peak detector circuit.

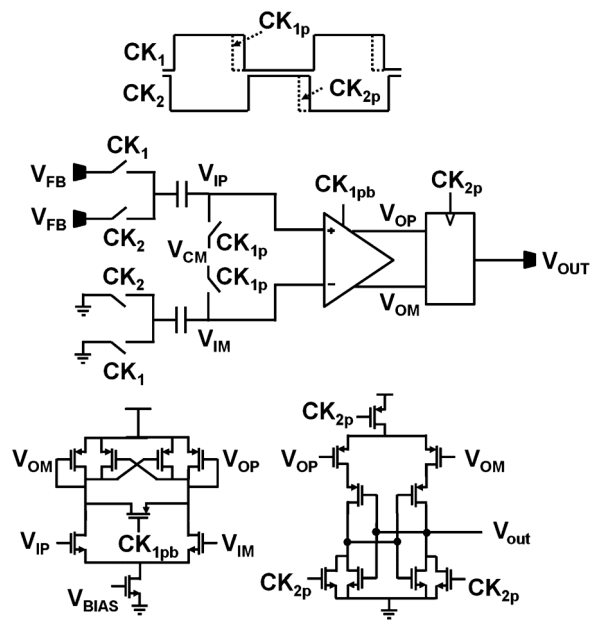

Fig. 18. Comparator schematic and timing diagram.

relative values of $\mathrm{V_{FB}}$ and $\mathrm{V_{REF}}$ determine the operation of the feedback loop and control the state of the three-bit counter.

Upon receiving the CAL signal, the counter resets the TMN to 000. In response to the 000 counter state, the TMN presents a large resistive load and extracts minimum power from the PA. The resultant swing at the antenna is measured at the peak detector output $(\mathrm{V_{FB}})$ and compared with $\mathrm{V_{REF}}$. If $\mathrm{V_{FB}} < \mathrm{V_{REF}}$, then the counter increments by one, changing the state of the TMN and impedance, to drive the output power higher. As described in Fig. 16, this process continues until the comparator detects that $\mathrm{V_{FB}} > \mathrm{V_{REF}}$, a condition which signifies the target output power has been reached. The optimal resistance [29] (R_{OPT}) detector monitors for nonmonotonic variation in the voltage swing at the antenna as the counter increments at each clock cycle. A switched-capacitor comparator monitors the slope of $\mathrm{V_{FB}}$; when a change in the sign of the slope is detected, the PCL operation stops. In the case where the TMN is incapable of achieving the target output power specified by $\mathrm{V_{REF}}$, the feedback loop stops at the maximum output power setting.

The counter, latch and all other digital blocks were realized using standard static-CMOS logic. A description of the remaining PCL blocks, the peak and R_{OPT} detectors, are given next.

1) Peak Detector: A differential source follower [30], shown in Fig. 17, is used for the peak detection circuit. The detector maps power levels in the range of 20–30 dBm to a voltage, $\mathrm{V_{FB}}$, at the detector output. Two design challenges exist for this detector. First, $\mathrm{V_{FB}}$ should monotonically increase with increasing power levels, and second, the voltage mapping of $\mathrm{V_{FB}}$ needs to be supply independent as there is no regulator for this chip. While delivering 30 dBm of output power to a 100-Ω differential antenna, the single-ended voltage swing of the PA can reach $\sim$7 V. To protect the input devices of the detector, a capacitor divider is used between the antenna and the detector input. The capacitance values are selected to minimize the loading on the secondary side of the power combiner.

2) R_{OPT} Detector: While the PCL modulates the TMN, the output of the peak detector $(\mathrm{V_{FB}})$ is monitored by the $\mathrm{R_{OPT}}$ detection circuitry (RDC). The output of the RDC $(\mathrm{V_{OUT}})$ toggles its state when the slope of $\mathrm{V_{FB}}$ changes from positive to negative, or vice versa. A change in the slope of $\mathrm{V_{FB}}$ indicates that the output power of the PA is no longer monotonically increasing as the PA load resistance reduces. In response to the RDC, as shown in Fig. 16, the PCL stops the counter, and the TMN is maintained in a state that extracts maximum output power from the PA.

A switch-capacitor comparator lies at the core of the RDC. The timing diagram and schematic of the comparator that contain the sampling capacitors, preamplifier, and latch are shown in Fig. 18. To determine the slope of $\mathrm{V_{FB}}$, the difference of the two consecutive samples of the peak detector, $\mathrm{V_{FB}}[n]$ and $\mathrm{V_{FB}}[n-1/2]$, is stored on a sampling capacitor. $(\mathrm{V_{FB}}[n] - \mathrm{V_{FB}}[n-1/2])$ is compared with zero to detect a positive or negative slope. The output $\mathrm{V_{OUT}}[n]$ is stored in a flip-flop. Similarly, in the next cycle, $\mathrm{V_{OUT}}[n+1]$ is determined by comparing

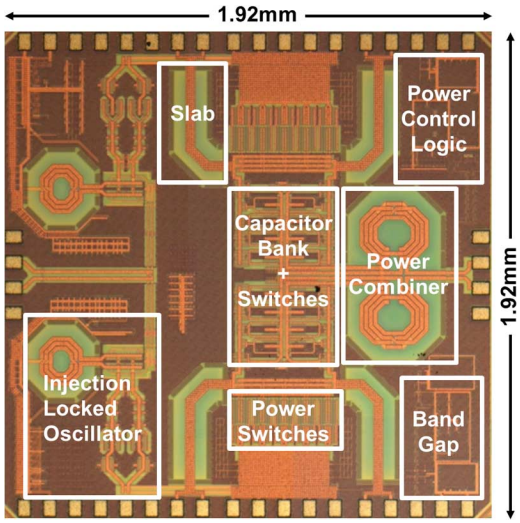

Fig. 19. Sensor PA chip micrograph.

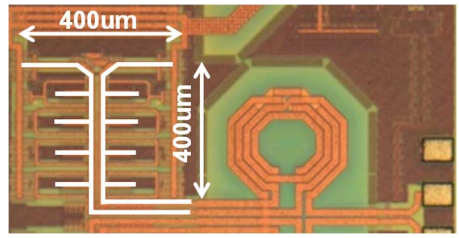

Fig. 20. Extra routing introduced by switches on high-resistivity substrate.

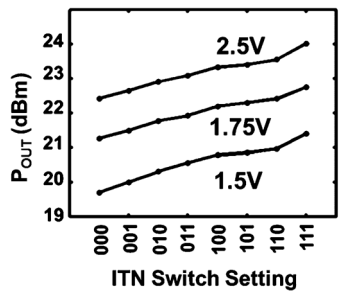

Fig. 21. Output power as a function of TMN switch settings for different supply voltages.

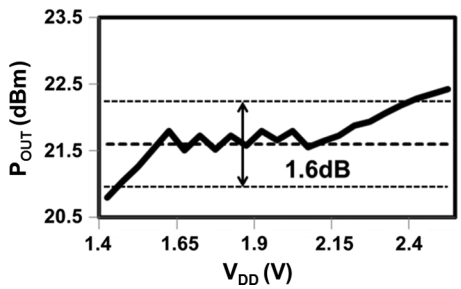

Fig. 22. Power control as a function of the supply voltage.

$(\mathrm{V_{FB}}[n+1]-\mathrm{V_{FB}}[n+1/2])$ with zero. Finally, $(\mathrm{V_{OUT}}[n+1]$ XOR $\mathrm{V_{OUT}}[n])$ is computed to detect a change in the slope of $\mathrm{V_{FB}}$.

Nonoverlapping clock generation circuitry is used to generate the clock phase signals $\mathrm{CK}_1, \mathrm{CK}_2$. The falling edges of CK_{1P} and CK_{2P} are slightly advanced in time as compared with CK_1 and CK_2; this helps to reduce charge-injection effects. The comparator's preamplifier has diode-connected cross-coupled PMOS loads in order to increase the gain. A preamplifier output stage is connected to a dynamic latch which generates full swing digital levels.

VI. Measurement Results and Comparison

The PA was implemented in a standard 90-nm CMOS process with a nine-metal stack, including one ultra-thick metal (UTM) layer; the die photo is shown in Fig. 19. All passive components, including the TMN and the finite choke inductance [31], [32], have been integrated on chip. The core measures 1.92 mm $\times$ 1.92 mm.

On-chip wafer probing was done to measure the PA's performance. There are two modes of operation to characterize this device: open-loop and closed-loop power control. In the open-loop mode, the switches in the TMN are controlled with off-chip digital codes; for the closed-loop mode, the TMN settings are controlled by the PCL. For the PCL to function, a one-time calibration is required for the on-chip peak detector. Performed in open-loop mode, this calibration consists of measuring $\mathrm{V_{FB}}$ while the TMN is cycled through the different power settings to generate an output power versus detector-voltage table. The external reference voltage $(\mathrm{V_{REF}})$, indicating the target output power, is then selected based on this table.

The power modulation curves as a function of the TMN switch settings, for three different supply voltages, are shown in Fig. 21. This plot shows that the power monotonically increases as the TMN switch-control cycles through the settings 000 to 111. These results verify that the shunt-load resistance and the PA output power can be modulated by varying C_{TUNE}. The output power regulation as a function of the variable supply voltage is shown in Fig. 22. As the super-capacitor discharges from 2.5 to 1.5 V, the total variation in output power delivered to the antenna is limited to 21.5 dBm $\pm$0.8 dB. The power can be controlled within $\pm$0.2 dB over the voltage range of 2.1 to 1.6 V.

To test the functionality of the power control loop, an external CAL signal was applied to the PCL. Based on the voltage output power versus detector-voltage table, a suitable value of $\mathrm{V_{REF}}$ is selected. The PA output, which could initially be at any arbitrary power level, is reset to its low-power state for each calibration period. The plot in Fig. 23 shows the output of the peak detector as the PA power is modulated. The steps in time correspond to switching states in the TMN series capacitor bank, C_{TUNE}. The loop eventually locks to the desired output voltage which corresponds to the target output power. The PCL can operate up to speeds of 1 MHz. At this frequency, the loop can take up to 8 clock-cycles, or 8 μs, to achieve either the target output power, or highest output power possible using the given TMN. In this example, the target output power is achieved after five clock-cycles.

While the PCL and the TMN have been experimentally verified, the sensor PA's output power is approximately 5 dB lower than the designed value. The source of this loss has been traced back to the high bulk-impedance switches in the TMN.

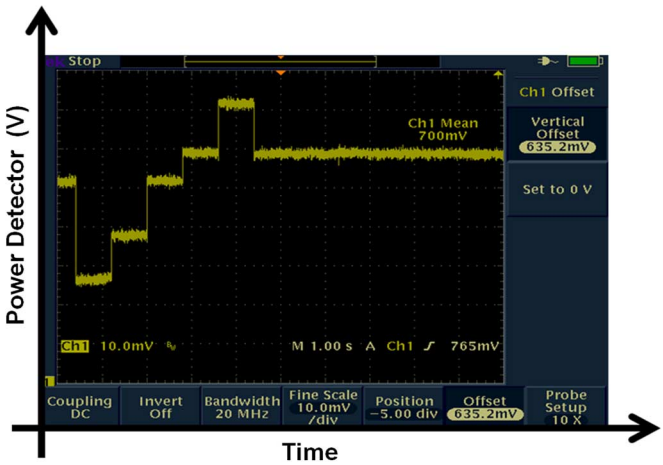

Fig. 23. Oscilloscope screen capture of the PCL reaching the target output power.

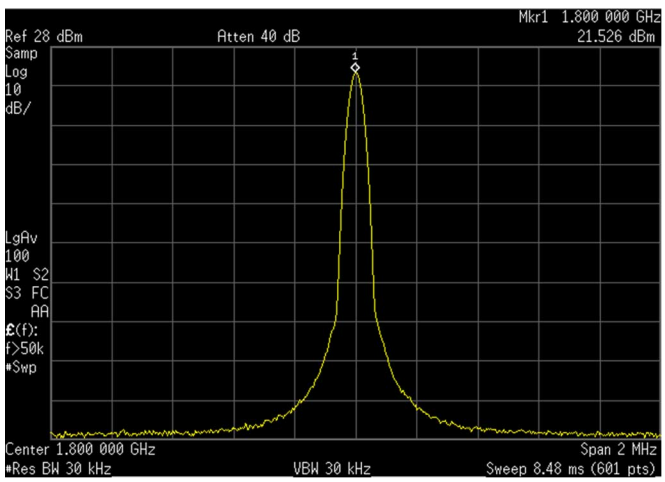

Fig. 24. Measured PA output power (including the 2.5-dB cable loss) with a 1.8-GHz single-tone input, 2.5-V supply voltage, and TMN in the maximum output-power state.

As mentioned in Section IV, in order to obtain a large R_{BULK}, the spacing between the switches and the surrounding substrate contacts were an important consideration. The NMOS switches in the TMN consumed 0.4 mm $\times$ 0.4 mm as indicated in Fig. 20. This large spacing introduces significant area overhead and parasitics in the signal path. The capacitance bank introduces approximately 600 μm of additional routing between the PA and the power combiner. While extensive simulations were performed to capture the effects of distributed resistance in the substrate and metal routing, inaccurate modeling resulted in lower peak efficiency (12%) compared with design. After de-embedding the 2.5-dB cable loss, a peak output power, as shown in Fig. 24, of 24 dBm is measured.

Finally, to observe the linearity with modulated data, the sensor PA is tested with a GSM input signal. The PA is set to its peak output power state, with all the switches of the TMN turned on. The resolution bandwidth in the spectrum analyzer was set to 30 KHz for the power spectral density (PSD) measurement. The spectrum, shown in Fig. 25, was averaged over 500 samples. The measured PSD at offset frequencies of

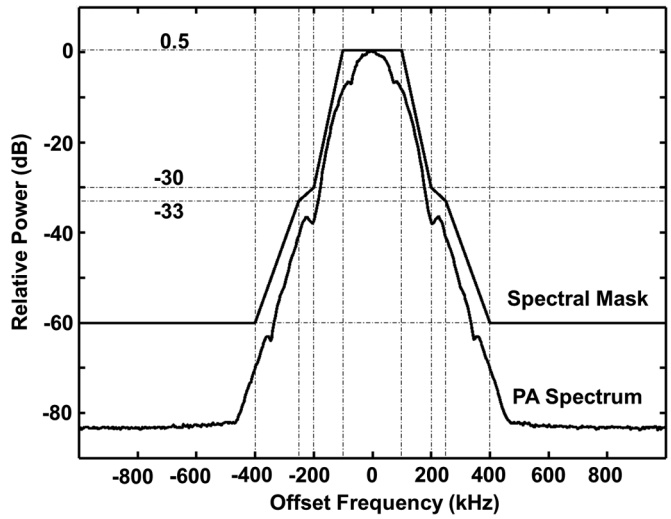

Fig. 25. Measured PA output spectrum at peak output power with a GSM modulated input signal.

$\pm$200 KHz, $\pm$250 KHz and $\pm$400 KHz meet the GSM spectral mask requirements.

A. Comparison to Prior Art

Impedance tuning networks have gained widespread interest in recent years [33]–[36]. However, a fair quantitative comparison between the different approaches is difficult because the prior art has been implemented in diverse technologies and for different applications. The TMN proposed in this paper completes the integration of the tuning network and power control loop on-chip. Thus, a qualitative comparison between the relative merits of the different techniques is provided.

To date, tunable elements at the output of the PA have been proposed for efficiency and linearity improvement [33], [34], as well as multimode [35], [36] and multiband operation [24]. Circuits addressing the issue of high-voltage standing wave ratio (VSWR) variation at the antenna–PA interface also exploit tunable matching techniques. While the work in this paper has been presented in the context of a sensor TX for long-range transmission, the PA load impedance tuning techniques are easily extended to the aforementioned applications. A majority of the solutions previously proposed use discrete, off-chip components [37], [39], MEMS [25], [40] or nonstandard CMOS processes like silicon-on-sapphire [41] and SOI [42]. In contrast, the PA, TMN, and digital PCL described in this paper are fully integrated in a standard CMOS process. More recently, [43] introduced a transmission line actuator to perform tuning in an output matching network for a 28-GHz self-healing PA. However, the area overhead associated with transmission lines at lower RF frequencies would preclude their use in a fully integrated solution. Reference [36] explores the use of a transformer-based matching network with shunt-capacitance-based tuning for dual mode (low-power and high-power) operation. The multibit series capacitance bank used in conjunction with the transformer-based matching network proposed in the current work allows for finer-resolution control of the output power. Finally, the feedback to control the tuning network is another

TABLE I
COMPARISON WITH PRIOR ART

	Tech	Tuning Element	Control Loop	Freq
[39]	Discrete	Off-Chip Varactor	None	-NA-
[40]	LDMOS PA	Abrupt Junction Si-Varactor L-C Match	None	1GHz
[41]	0.13um CMOS	Duty Cycle modulation with off-chip switch capacitance	None	
[45]	180nm CMOS	Transformer Matching with Capacitance Tuning	None	1.95GHz
[48]	RF-MEMS	RF-MEMs Switched Capacitor Array	On-Chip	--
[49]	0.13um SOI CMOS	On-chip shunt switched capacitor array	None	2.4GHz
[51]	CMOS	Transmission Line Actuator With Bias Voltage Control	On-Chip	28GHz
This Work	90nm CMOS	Transformer Matching with On-chip capacitor Array	On-Chip	1.9GHz

important component in this system, which has received attention in recently published work [40], [43]. In this work, an up–down counter-based power control loop that exploits the monotonic nature of the shunt-resistance/output-power relationship in switching PAs has been proposed.

B. Future Directions

The voltage-mode Class-E type PA, implemented in this chip, experiences large voltage swings, up to $2.5\mathrm{V_{DD}}$, at the drain of the power NMOS switch. Therefore, to ensure transistor reliability, the C_{TUNE} capacitor bank was implemented using high-bulk impedance switches. As noted earlier, the considerable area overhead of these switches resulted in high insertion loss. An alternate PA topology, which might be more suitable for this application, could include zero-voltage switching, current-mode inverse Class-D topologies [45]. In the current-mode PA topology, the PA output voltage is limited between VDD and ground, thereby obviating the need for high-voltage switches and the excessive routing throughout the capacitor bank.

VII. CONCLUSION

To complement existing ultra-low-power short-range, multihop mesh-network based sensors, a sensor PA designed with the explicit goal of enabling long-range single-hop data transmission has been presented in this paper. To enable efficient utilization of harvested ambient energy, a regulatorless PA has been proposed. An impedance tuning network and feedback-loop to autonomously regulate the output power with a variable supply voltage are presented. A prototype circuit fabricated in a 90-nm CMOS process achieves a peak output power of 24 dBm and power regulation within 21.5 ± 0.8 dB for a variation in the supply voltage variation from 2.5 to 1.5 V. A comparison with other tunable matching network PAs is given in Table I.

APPENDIX I

Consider a system with a switching PA with a linear regulator in the supply path [Fig. 4(a)]. The matching network $(\mathrm{M_2})$ is assumed to be ideal with 0 dB of insertion loss. The energy delivered to the load R_{L1} over a time interval t is

$$E_{\mathrm{PA}}(t) = \mathrm{V_{DD}} I_{\mathrm{OUT}} t \tag{14}$$

where $\mathrm{V_{DD}}$ is the regulated supply voltage across the PA and I_{OUT} is the fixed current drawn from the power supply via the linear regulator. Considering this simplified model, the linear regulator has a time-varying voltage drop $\mathrm{V_{REG}}(t)$ described by

$$\mathrm{V_{REG}}(t) = (\mathrm{V_{MAX}} - \mathrm{V_{DD}}) \left(1 - \frac{t}{t_{\mathrm{CROSS}}}\right) \tag{15}$$

where $\mathrm{V_{MAX}}$ is the initial super capacitor voltage and t_{CROSS} is the time instant, where $\mathrm{V_{MAX}} = \mathrm{V_{DD}}$.

$$t_{\mathrm{CROSS}} = (\mathrm{V_{MAX}} - \mathrm{V_{DD}}) \frac{C}{I_{\mathrm{OUT}}}. \tag{16}$$

The energy loss associated with an LDO is determined by integrating the power dissipation of the regulator over the entire transmission burst:

$$\begin{aligned} E_{\mathrm{REG}}(t_{\mathrm{CROSS}}) &= I_{\mathrm{OUT}} \int_0^{t_{\mathrm{CROSS}}} \mathrm{V_{REG}}(t) dt \\ &= \frac{(\mathrm{V_{MAX}} - \mathrm{V_{DD}})}{2} I_{\mathrm{OUT}} t_{\mathrm{CROSS}}. \end{aligned} \tag{17}$$

Based on (14) and (17), the total energy efficiency of the system can be described by

$$\eta = \frac{E_{\mathrm{PA}}}{E_{\mathrm{PA}} + E_{\mathrm{REG}}} = \frac{2}{1 + \frac{\mathrm{V_{MAX}}}{\mathrm{V_{DD}}}}. \tag{18}$$

APPENDIX II

The input admittance model for the TMN can be derived through a sequence of series-to-parallel transformations. Consider the model shown in Fig. 9. The loss in the primary and secondary inductors are modeled by series resistance R_{PL} and R_{SL}, respectively. The load resistance presented by the antenna is assumed to be real R_{ANT}. The imaginary component of the load impedance is absorbed into the secondary tuning capacitance C_s. The effective load resistance on the secondary of the transformer can be shown to be

$$R_{\mathrm{S,LOAD}} = \left\{ \frac{R_{\mathrm{ANT}}}{1 + Q_{\mathrm{CP}}^2} + R_{\mathrm{SL}} \right\} \left\{1 + Q_{\mathrm{CS}}^2\right\} \tag{19}$$

where

$$Q_{\mathrm{CP}} = \omega C_s R_{\mathrm{ANT}}; \quad Q_{\mathrm{CS}} = \frac{1}{\left(\omega C_s \left\{ \frac{R_{\mathrm{ANT}}}{1+Q_{\mathrm{CP}}^2} + R_{\mathrm{SL}} \right\}\right)}. \tag{20}$$

If capacitance C_s resonates with L_s at the carrier frequency, $\omega_{RF} = 1/\sqrt{L_s C_s}$, the real part of the admittance at the primary

[46] of a transformer with turn ratio and mutual-coupling coefficient (n, k_m) is given by

$$R_{\mathrm{TXFRM}} = \frac{R_{\mathrm{S,LOAD}}}{\left(\frac{n}{k_m}\right)^2}. \tag{21}$$

The input impedance of the transformer appears as a series L–R circuit of $R_{\mathrm{TXFRM}} + R_{PL}$ in series with the leakage inductance $L_P(1 - k_m^2)$. A series-to-parallel transformation on this L–R circuit results in shunt inductance $L_{PX} = L_P(1 + Q_L^2/Q_L^2$, where $Q_L = \omega_{\mathrm{RF}} L_p(1 - k_m^2)/(R_{PL} + R_{\mathrm{TXFRM}})$. A resonating capacitor C_p at the primary of the transformer, chosen such that $\omega_{\mathrm{RF}} = 1/\sqrt{L_{PX} C_p}$, results in input shunt resistance

$$R_T = \left\{1 + Q_L^2\right\} * (R_{\mathrm{TXFRM}} + R_{PL}). \tag{22}$$

The resistance $(R_T + 2R_X)$ now appears in series with the tuning capacitance $C_{\mathrm{TUNE}}/2$. The final series-to-parallel transformation leads to the net shunt resistive load on the PA

$$R_{\mathrm{in}} = \left[1 + Q_C^2\right] * \left(\left\{1 + Q_L^2\right\}(R_{\mathrm{TXFRM}} + R_{PL}) + 2R_X\right). \tag{23}$$

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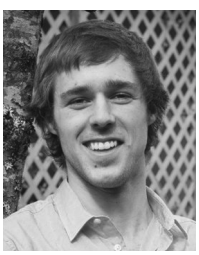

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