A 0.8–2 GHz Fully-Integrated QPLL-Timed Direct-RF-Sampling Bandpass $\Sigma\Delta$ ADC in 0.13 μm CMOS

Subhanshu Gupta, *Member, IEEE*, Daibashish Gangopadhyay, *Member, IEEE*, Hasnain Lakdawala, *Member, IEEE*, Jacques C. Rudell, *Senior Member, IEEE*, and David J. Allstot, *Fellow, IEEE*

Abstract—A reconfigurable bandpass continuous-time $\Sigma\Delta$ RF ADC tunable over the 0.8–2 GHz frequency range is presented. System- and circuit-level innovations provide low power consumption and reduced circuit complexity. The proposed architecture operates in both the first- and second-Nyquist zones to enable a wide tuning range from a fixed sampling frequency of 3.2 GHz. A fully-integrated on-chip quadrature phase-locked loop (QPLL) allows quadrature phase synchronization between a raised-cosine DAC and a quantizer. Implemented in 0.13 μm CMOS the fully-integrated prototype achieves SNDR values of 50 dB, 46 dB, and 40 dB over a 1 MHz bandwidth at 796.5 MHz, 1.001 GHz and 1.924 GHz carrier frequencies, respectively, with a total power consumption of 41 mW. The measured phase noise of the QPLL is -113 dBc/Hz at an offset frequency of 1 MHz and the reference spur is -74.5 dBc. The RMS period jitter is 1.38 ps at 3.2 GHz.

Index Terms—Charge pump, direct-RF sigma-delta ADC, direct sampling RF, finite-impulse response DAC, harmonic-rejection injection-locked oscillator, integer-N phase-locked loop, narrowband programmable LNA, reconfigurable, reference spur, SDR.

I. INTRODUCTION

MANY wireless standards are used to meet the increasing demands for high bandwidth, low power, compact form factor and cost in a single-chip solution. Thus, there is a need for reconfigurable fully-integrated wireless front-ends [1]. Previous research has explored the programmability of different receiver architectures including homodyne or direct-conversion, integrated heterodyne and low-IF systems [2]–[5]. However, the bandwidth, dynamic range and power consumption associated with the analog-to-digital converter (ADC) limit the level of integration. Implementing multiple standards in a single RF receive path as envisioned in a Cognitive or Software-Defined Radio (SDR) requires programmability and flexibility [6], which usually are achieved more efficiently in
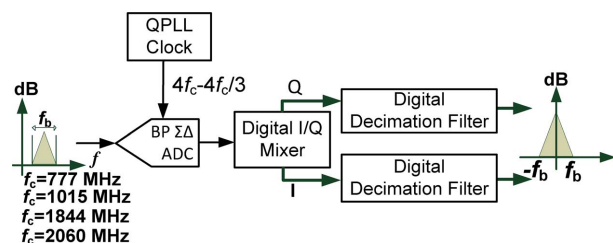
Fig. 1. RFADC-based SDR architecture.

the digital domain. The key enabling feature of multi-standard receivers is the ability to digitize the signal as close to the antenna as possible. A programmable ADC that performs direct sampling at RF is presented in this paper.

A tunable bandpass $\Sigma\Delta$ modulator in which a digital receiver follows the antenna, bandpass filter, low-noise amplifier (LNA) and RF ADC (Fig. 1) facilitates the programmability of both bandwidth and dynamic range. A brief overview of RF ADCs with emphasis on continuous-time $\Sigma\Delta$ ADCs is given in Section II. Section III details a design methodology for the bandpass $\Sigma\Delta$ ADC and Section IV considers circuit topologies and design challenges. Measurement results are presented in Section V.

II. BACKGROUND

A software-defined radio requires a high-performance ADC which operates in excess of 1 GHz with a large dynamic range, to digitize the RF signal immediately after the front-end LNA. Recent SDR architectures are classified broadly according to the location of the sampler (Fig. 2):

(a) direct-conversion/low intermediate frequency (DCR-low-IF) [3];

(b) discrete-time bandpass charge-sampling (DT-BP-CS) [4];

(c) continuous-time bandpass sigma-delta (CT-BP-$\Sigma\Delta$) [13].

In the DCR-low-IF topology (Fig. 2(a)), the sampler and ADC follow the down-conversion mixer and low-pass filter. This approach is attractive for low-power, low-area designs because of the relaxed anti-alias filter and ADC requirements [2]. However, a reconfigurable implementation requires multiple front-ends tuned to different frequencies which render this option inefficient in terms of area and power dissipation. In the DT-BP-CS architecture (Fig. 2(b)), the sampler precedes the down-conversion mixer, low-pass filter, and ADC. The requirements for the converter are relaxed but the tunable discrete-time filter is difficult to design and is area inefficient. A

TABLE I
RFADC SPECIFICATIONS

Standard	GSM	CDMA	ZigBee	Bluetooth	802.11b	WiMax
Sensitivity (dBm)	-104	-117	-92	-80	-85	-117
Noise Figure (dB)	3	3	3	3	3	3
LNA Gain (dB)	15	15	15	15	15	15
Thermal Noise (dBm/Hz)	-174	-174	-174	-174	-174	-174
Channel Bandwidth (MHz)	0.2	1.25	5.0	1.0	10.0	20.0
Total Bandwidth (MHz)	25	75	80	83	83	200
ADC Noise/Channel (dBm)	-103	-95	-89	-96	-86	-83
Maximum Blocker (dBc)*	-13	-30	-20	-20	-36	-20
Full-scale Input (dBm)	2	-15	-5	-5	-10	-5
ADC SNR (dB)	90	65	69	76	50	63
Required Resolution (bits)	15	10.8	11.5	12.7	8.33	10.5
Sampling Jitter (ps)	25.2	71.3	11.3	25.2	50.3	5.64

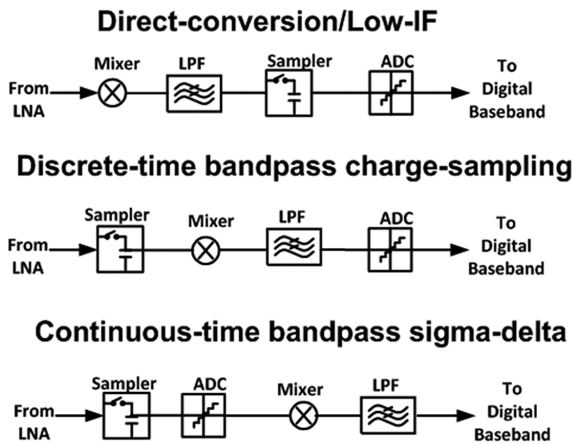* Assuming (on- or off-chip) 15 dB blocker attenuation at the RF input

Fig. 2. General block-level architectures of SDR chains. Note the relative position of the sampler and ADC.

narrowband bandpass (BP) $\Sigma\Delta$ ADC (Fig. 2(c)) is well-suited for multi-standard, multi-mode systems because it exhibits low sensitivity to analog circuit imperfections and facilitates reconfigurability [7]. The integrator/resonator loop can be either discrete-time (DT) using switched-capacitor filters [8] or continuous-time (CT) using active-RC [9], g_m-C [10], or LC filters [11]–[13]. Inherent anti-alias filtering is an advantage of the CT approach and any residual aliasing artifacts are noise shaped out of the band of interest. The resonator (e.g., LC with on-chip inductors) is area and power efficient at GHz frequencies in scaled CMOS technologies. Sensitivity to clock jitter, however, is more of a concern for CT implementations.

Several publications describe advances toward SDR systems. A second-order BP modulator in a 0.5 μm SiGe HBT process achieved SNR $= 45$ dB (57 dB) for BW $= 3$ MHz (200 kHz) with $f_s = 3.8$ GHz [11]. A direct-RF receiver in 65 nm CMOS

down-converted the input signal to baseband and digitized it using a second-order low-pass $\Sigma\Delta$ ADC with $f_s = 900$ MHz, BW $= 9$ MHz, SNDR $= 56$ dB and $P_D = 80$ mW. The DAC current is up-converted to RF and fed back to the LNA [12]. A fourth-order $\Sigma\Delta$ ADC in 90 nm CMOS had $f_s = 3$ GHz, dynamic range (DR) $= 40$ dB, BW $= 60$ MHz and $P_D = 40$ mW. Power is saved by sampling at 3.2X below $f_{\text{Nyquist}} = 9.6$ GHz [13].

Specifications for the RFADC front-end for several standards are detailed in Table I. Although achieving 15-bit resolution with sufficient dynamic range remains a daunting challenge, direct-RF sampling reconfigurable receivers are evolving as CMOS scales.

III. BANDPASS CT $\Sigma\Delta$ ADC DESIGN PROCEDURES

The receive chain and the signal (STF) and noise (NTF) transfer functions of the proposed reconfigurable CT-BP-$\Sigma\Delta$ ADC tunable from 800 MHz to 2.4 GHz are shown in Figs. 3(a) and (b), respectively. A FIR-DAC (finite-impulse-response pulse-shaped DAC) (Fig. 3(c)) is used to combat jitter; timing mismatches between the feedback DAC and the loop quantizer are mitigated using the fully-integrated Type-II low-power, low-spur, harmonic-rejection injection-locked PLL described below.

A. A BP $\Sigma\Delta$ ADC is synthesized from a low-pass prototype using a low-pass to bandpass transformation [14], [15]

$$z^{-1} \Rightarrow -\frac{z^{-2} - a_1 z^{-1} + a_2}{a_2 z^{-2} - a_1 z^{-1} + 1} \tag{1}$$

$$a_1 = \frac{2\alpha k}{k+1}, \quad a_2 = \frac{k-1}{k+1}, \quad k = \cot\frac{\omega_{c2} - \omega_{c1}}{2}\tan\frac{\omega_{lp}}{2},$$

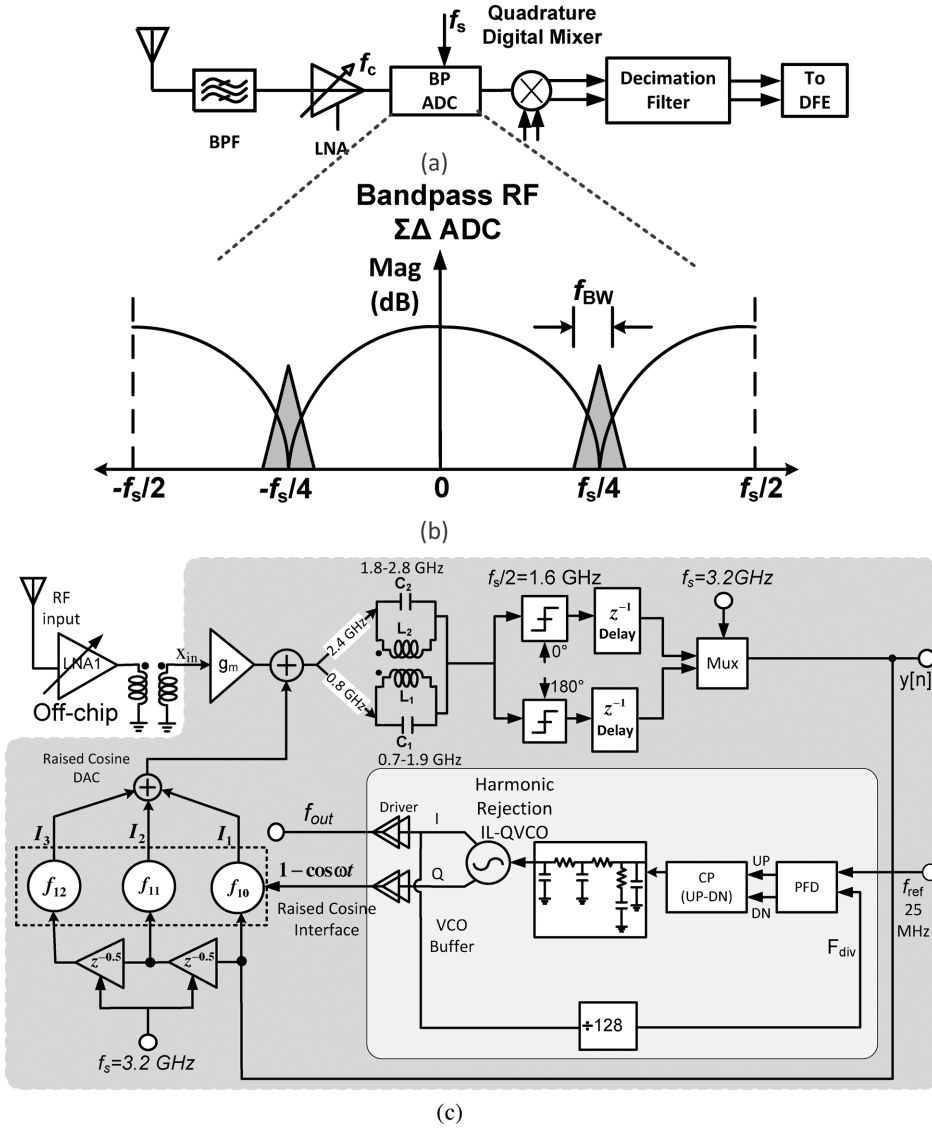$$\alpha = \frac{\cos\frac{\omega_{c1}+\omega_{c2}}{2}}{\cos\frac{\omega_{c2}-\omega_{c1}}{2}} \tag{2}$$

Fig. 3. (a) High-level representation of a CT-BP-ΣΔ RFADC in a radio receiver. (b) STF and NTF frequency responses. (c) Overall architecture including the QPLL.

where ω_{lp} is the LPF cutoff frequency and $\omega_{\mathrm{c}1}$ and $\omega_{\mathrm{c}2}$ are the BPF lower and upper cutoff frequencies, all normalized over DC to $f_{\mathrm{s}}/2$. ω_{lp} can be arbitrarily set to the BPF bandwidth, ω_{B}. $\omega_{\mathrm{c}1}$ and $\omega_{\mathrm{c}2}$ may be set to the resonator frequency, ω_{c}, in which case ω_{B} approaches zero and $\alpha = \cos(\omega_{\mathrm{c}})$ and $k = 1$. Thus, (1) and (2) simplify to

$$z^{-1} \rightarrow \frac{\cos \omega_{\mathrm{c}} z^{-1} - z^{-2}}{1 - \cos \omega_{\mathrm{c}} z^{-1}}, \quad \text{where } \omega_{\mathrm{c}} = 2\pi \frac{f_{\mathrm{c}}}{f_{\mathrm{s}}}. \quad (3)$$

The transfer function representing a *reconfigurable* topology obtained from (3) using selected ω_{c} values is then used to calculate the STF and NTF responses. The results are equated to the CT-DT transformation results to find the coefficients for the CT ADC.

B. The performance of a non-return-to-zero (NRZ) DAC (Fig. 4(a)) is limited by the distortion created during switching events caused by inter-symbol interference (ISI), lack of synchronization, and clock jitter. A return-to-zero (RZ) DAC (Fig. 4(b)) mitigates ISI but requires a greater amplitude to

maintain the output energy [16]–[18]. The use of a raised-cosine DAC (Fig. 4(c)) alleviates ISI and achieves low jitter sensitivity [19]. The sinusoidal pulse (for the raised-cosine DAC) and sampling clock are aligned so that the DAC switches during the zero-slope intervals of the sinusoidal pulse. Thus, first- and second-order jitter insensitivities are achieved at the sampling instants. Raised-cosine pulses also feature less signal attenuation at higher under-sampling ratios as depicted in Fig. 5.

C. Establishing equivalence between a CT BP ADC using *LC* resonators and a DT BP ΣΔ ADC using integrators is difficult because of fewer coefficients in the latter. Thus, a raised-cosine DAC is combined with a 3-tap FIR response to realize a three-tap raised-cosine FIR filter (Fig. 3(c)) [20]–[22]. To realize $H_{\mathrm{CT-DT}}(z)$, the transfer function of the CT loop filter, $H(s)$, is multiplied by the impulse response of the DAC, $R_{\mathrm{COSDAC-FIR}}(s)$, and the modified z-transform is applied

$$H(z)_{\mathrm{CT-DT}} = \sum_{m_{\mathrm{i}}} \{H(s)R_{\mathrm{COSDAC-FIR}}(s)\}. \quad (4)$$
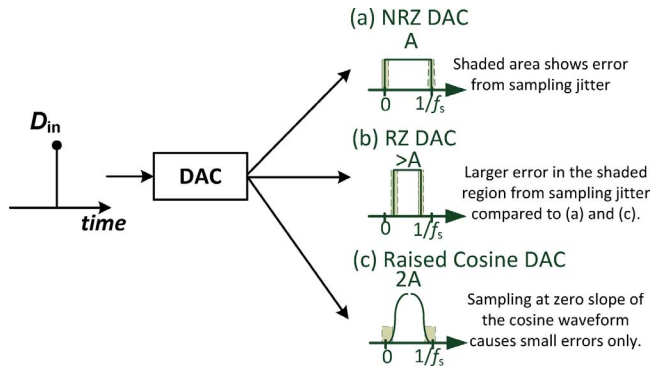
Fig. 4. DAC pulse shapes: (a) Non-return-to-zero, (b) return-to-zero, and (c) raised cosine. Sensitivity to jitter is depicted by the shaded area.
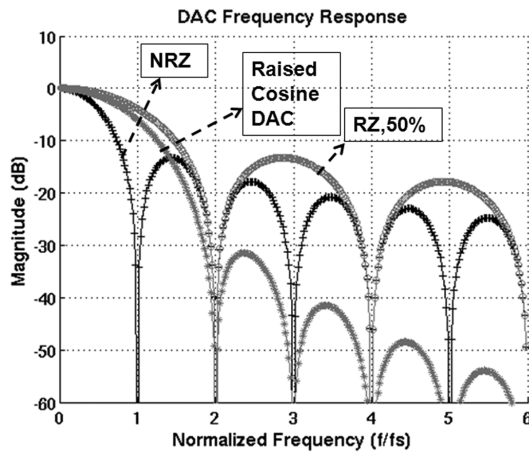

Fig. 5. Ideal frequency responses of several DACs.

TABLE II
THREE-TAP FIRDAC COEFFICIENTS

Frequency	DAC1 (f_{10})	DAC2 (f_{11})	DAC3 (f_{12})
$f_s/4$ (800 MHz)	25/64	(15/64)√2	5/64
$3f_s/4$ (2.4 GHz)	-35/192	(7/64)√2	-7/192
$3f_s/8$ (1.2 GHz)	-0.91	0.21	-0.80

The delay factor, m_i, is normalized to the sampling period (i.e., $0 < m_i < 1$). The resulting filter coefficients are listed in Table II.

D. A BP $\Sigma\Delta$ ADC achieves a high signal-to-quantization-noise ratio (SQNR) using a high over-sampling ratio, OSR = $f_{\text{CLK}}/(2f_{\text{BW}})$ (e.g., 200–1000X). A conventional $f_{\text{CLK}}/4$ BP $\Sigma\Delta$ modulator requires f_{CLK} = 3.2 GHz (9.6 GHz) for an 800 MHz (2.4 GHz) input signal. Sampling at 9.6 GHz is susceptible to period jitter and problematic for low-power implementations. These shortcomings are side-stepped by under-sampling RF input signals > 1.6 GHz (i.e., the second-Nyquist zone). Thus, this architecture over-samples at frequencies $< f_{\text{CLK}}/2$ and under-samples at center frequencies $> f_{\text{CLK}}/2$ (e.g., $3f_{\text{CLK}}/4, 5f_{\text{CLK}}/8$, etc.) which increases the tuning range. Under-sampling factors of 2–3X typically degrade the SNDR by only 3–5 dB if other spurious signals are negligible.

TABLE III
NOISE AND POWER CONSUMPTION

Noise Source	Noise Contribution		Power Consumption
	Worst-case (%) (First Nyquist Zone)	Worst-case (%) (Second Nyquist Zone)	
Thermal Noise (RF Front-End) incl. g_m-LC resonator, FIRDAC, Source-Follower)	30	25	14 mA (Resonator) 1 mA (DAC) 7 mA (PLL)
Quantization Noise	40	45	4.5 mA (Comparator)
Clock Jitter	25	27	1.5 mA (Clock Buffers)
Quantizer Offset/Metastability	5	5	6 mA (Test circuits + O/p Buffers)
Total	100	100	34 mA (Total)

E. Sensitivity analysis is used to determine the impact of excess loop delay (ELD), clock jitter, and $\Sigma\Delta$ ADC coefficient variations on STF, NTF, group delay, and phase margin of the second-order system. A cycle-to-cycle jitter of 4 ps-rms and a maximum ELD of 25% are required for SNR = 50 dB. Table III details the overall noise budgets for operation in the first- or second-Nyquist zone. Quantization noise dominates thermal noise and clock jitter.

F. Key circuits include a tunable variable-gain resonator, a re-configurable raised-cosine DAC, a low-power 1-bit comparator, and a low-jitter low-power QPLL. Architectural choices and specifications are described below.

- Resonator: Frequency range = 0.8–2.4 GHz; Noise Figure (NF) < 4.5 dB with and < 3 dB without Q-enhancement; low-power consumption; Dynamic Range (DR) > 9 bits, and a wideband input match using a common-gate topology.
- 1-bit time-interleaved comparator: Low metastability, hysteresis, and input-referred offset voltage; time-interleaved to reduce power consumption.
- Jitter-insensitive DAC: 3-tap raised-cosine FIR-DAC for jitter < 4 ps-rms. A QPLL generates the raised-cosine waveform and maintains I-Q phase synchronization with the comparator.
- Type-II fourth-order 3.2 GHz QPLL: Phase noise < -110 dBc/Hz at an offset frequency of 1 MHz. The loop bandwidth is chosen as the frequency offset where the CP/PFD and VCO phase noise contributions are equal.
- QVCO: A 3.2 GHz quadrature oscillator employs strong injection with small K_{VCO} and K_{VDD} values to achieve low phase noise and supply sensitivity. A higher frequency VCO with dividers to generate the I-Q signals is not feasible because the DAC requires a cosine waveform with small amplitude.
- PFD: A dead-zone-free tri-state PFD which limits the in-band phase noise of the PLL also determines the maximum closed-loop bandwidth.
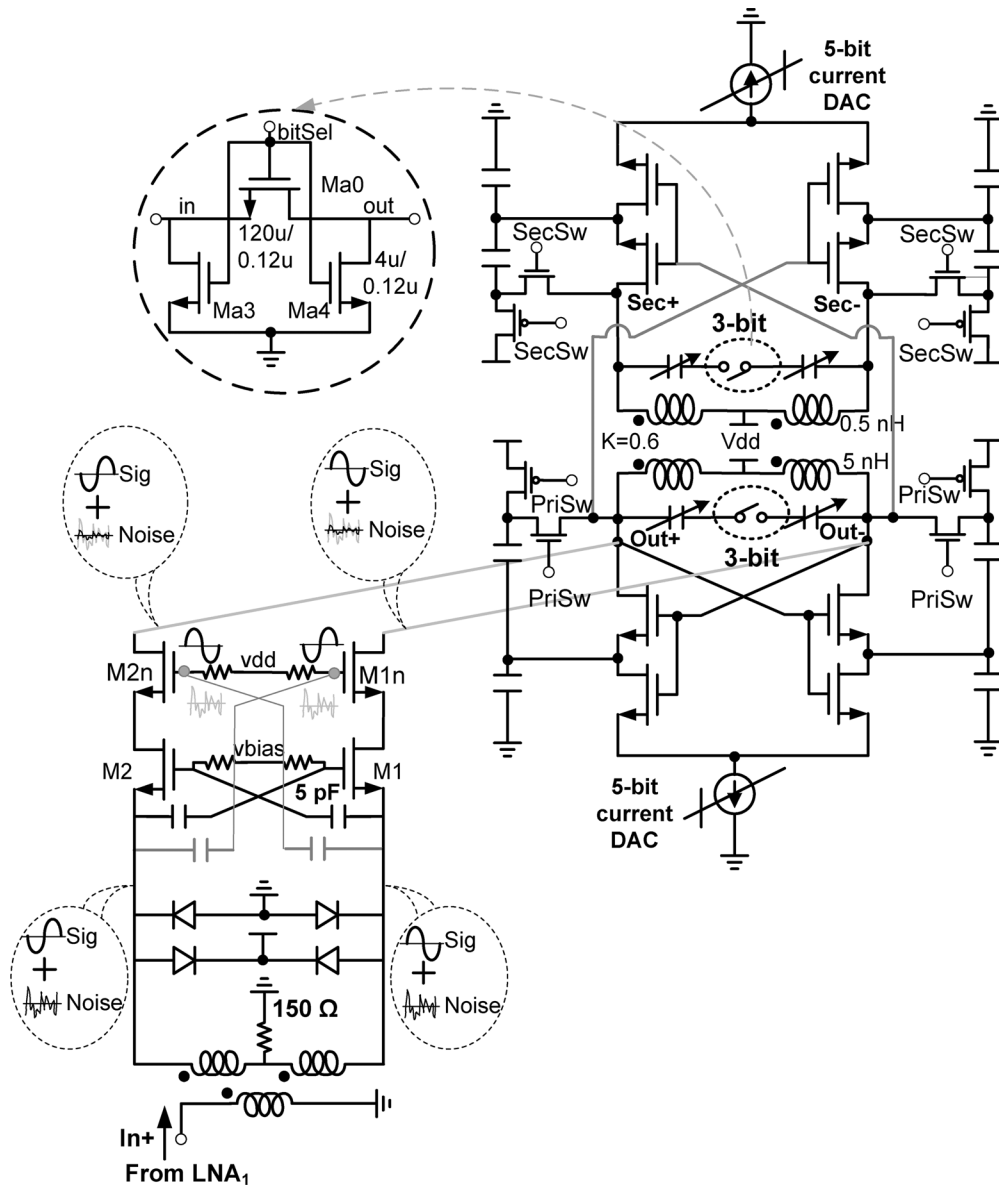
Fig. 6.   Common-gate narrowband transformer-coupled tunable resonator.

- CP: Good matching accuracy is assured between the UP and DN currents to achieve a highly-linear PFD/CP transfer characteristic and a small reference spur.
- LPF: A fourth-order LPF uses an external pole for increased attenuation of the reference spur and out-of-band noise.

G. PLL-RFADC interface: A programmable delay line may be used to match the I-Q routing delays at higher frequencies.

H. To meet the SNR requirements for the different standards, the order of the RFADC loop, the number of bits in the quantizer and/or the number of cascaded ADC stages may be increased.

IV. CIRCUIT DESCRIPTION

A. Tunable NarrowBand LNA/Resonator

1) Common-Gate Cross-Coupled g_m*-Cell With One-Stage Thermal Noise Cancellation:* The inductor-degenerated common-source LNA (CSLNA) is popular for narrowband

applications because it offers both high gain and low noise figure. The common-gate LNA (CGLNA) is attractive owing to its $1/g_m$ input resistance, and superior broadband input matching, linearity, stability, and robustness to PVT variations [23]. Noise factor, $F = 1 + \gamma/\beta$ where $\beta = g_m/g_{d0}$ and β and γ are empirical process- and bias-dependent parameters. Moreover, an inverting gain, A, added between the gate and source terminals boosts g_m to $(1 + A)g_m$, reduces F to $F = 1 + \gamma/\beta/(1 + A)|_{g_m R_s(1+A)=1}$, and uses less bias current [23]. Passive implementations for A are attractive for noise reasons although $A < 1$ for the divider between C_{gs} and C_c. Additional coupling paths from the inputs to the cascode terminals further improve both the forward-gain (S_{21}) and NF (Fig. 6). The additional feedback path saves area compared to a transformer-based CGLNA and provides noise cancellation in one rather than two stages [24]. The noise cancellation works as follows: The drain current noise of M_1 is injected into *Out-* through M_{1n} and capacitively coupled to M_2 and M_{2n}.
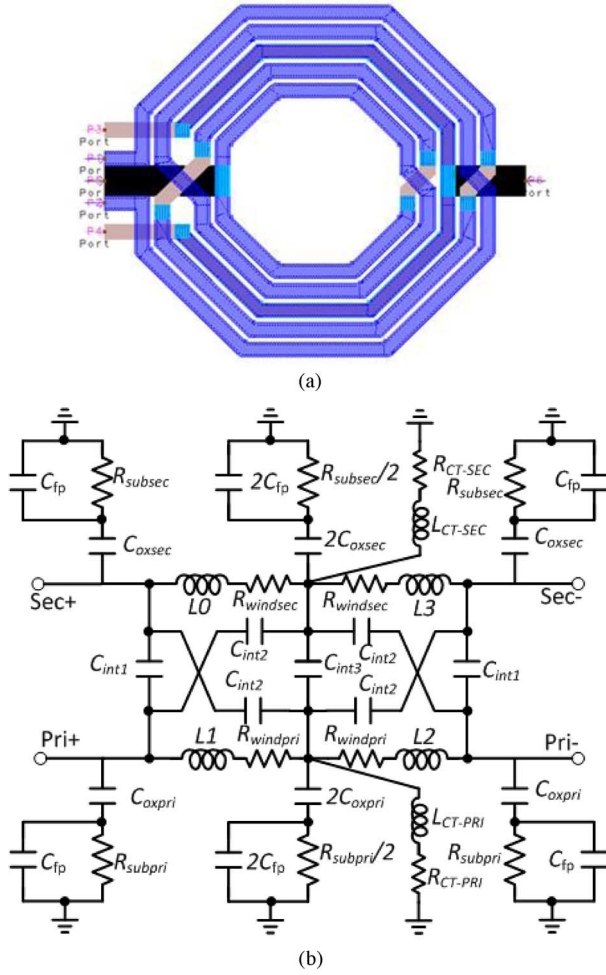
(a)

(b)

Fig. 7. (a) Layout of the 4:1 transformer. (b) Corresponding linear model [31].

Fig. 8. Post-layout simulations of S_{21} of the resonator (w/ and w/o Q-enhancement).

Correlated common-mode drain current noise appearing at the source nodes of M_1 and M_2 will be out of phase at the drains of M_{1n} and M_{2n}, which yields a reduction in the thermal noise from M_1 and M_2.

The input stage includes 4 dB of gain programmability to prevent saturation for large input signals. Lower NF (higher linearity) is achieved at higher (lower) gain settings.

2) Transformer-Based Dual-Mode Frequency Tuning: A low-power tunable narrowband LNA with high linearity operates from $f_0 = 800$ MHz to 2.4 GHz. The DR of the Q-enhanced *LC* BPF is [25]

$$\text{DR} \leq \frac{V_{\max}^2 C}{\text{KT}(\gamma + 1)Q}Q_o \approx \frac{\eta P_{\text{DC}}}{2\pi kT(\gamma + 1)BQ^2}Q_0^2 \quad (5)$$

where $Q_0(Q)$ is the quality factor of the inductor (resonator), B is the resonator bandwidth, P_{DC} is the DC power consumed and η is the efficiency factor.

Switched inductors which degrade Q_0 are compensated using a negative conductance cell at the cost of reduced DR [26]. The self-inductance of an on-chip metal spiral depends on the number of turns of the metal traces which is unaffected by PVT variations. However, the loss associated with a series CMOS switch reduces Q significantly [26]. Another tuning option, a CMOS varactor, exhibits an unacceptable level of
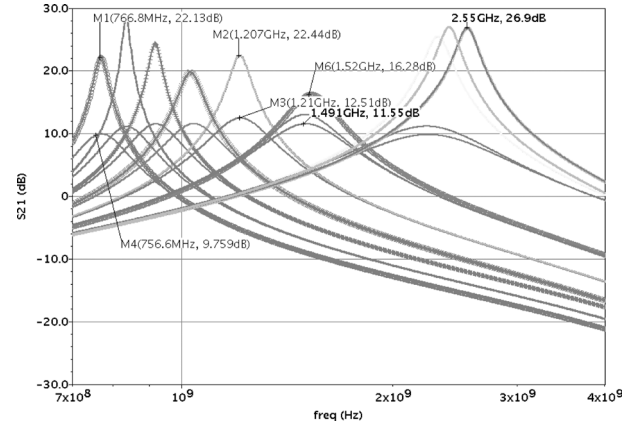
second-order distortion [27]. Hence, the resonator is tuned using a 3-bit switched-capacitor bank to achieve the desired tuning range (Fig. 6) [28]. The nMOS switch sizes are optimized to trade ON-state resistance against OFF-state parasitic capacitance. In the OFF-state, parasitic capacitance affects the high-frequency performance (e.g., $f_0 = 2.4$ GHz). Two extra nMOS devices are added to realize a small ON-state resistance [29]: M_{a3} (M_{a4}) connects the source (drain) to ground when M_{a0} is ON. Small sizes of M_{a0} are used to maximize Q and the tuning range.

A custom transformer (Fig. 7) replaces the spiral inductors whose parasitics limit the tuning range to about 1.7 GHz. It uses the thick top metal layer and shows a simulated Q of $\sim$8–12 from 0.8 to 2.4 GHz. Q is optimized to maximize DR and minimize P_{D}. The primary (secondary) windings are used for low-band (high-band) RF input signals. The coupling coefficient is $k = 0.6$ and the element values are $L_1 = 5.5$ nH, $L_2 = 0.5$ nH, $C_1 = 11$ pF, and $C_2 = 1$ pF.

A wider tuning range can be achieved with a higher k value but multi-mode oscillation becomes a concern [30]; hence, a moderate value is chosen (i.e., $k = 0.64-0.72$). An estimate of the size of the transformer is obtained using *ASITIC®* [31]. A 4:1 octagonal-shaped transformer (Fig. 7(a)) is then designed with minimal parasitics and modeled using *Agilent Momentum®*. A linear model (Fig. 7(b)) is developed for *Cadence®* transient simulations [32]. Finally, a hybrid of concentric and interleaved designs is used to achieve a high Q and a wide tuning range. Simulations of post-layout extractions show a tuning range of 2.51 GHz (Fig. 8). At maximum gain (including the LNA and the FIRDAC), NF varies from 2.8 to 7.5 dB over the entire tuning range. At minimum gain with no Q-enhancement, NF varies from 4.5 dB @ 730 MHz to 3 dB @ 2.51 GHz; 0.5 dB is contributed by the FIRDAC. NF is increased using the Q-enhancement circuits as expected. The input-referred noise contribution of the RFADC is less than 0.2 dB using a typical wideband LNA with gain = 12 dB and NF = 2.5 dB.

A negative conductance cell that boosts the Q of the lossy *LC* tank is implemented using a linearized *Colpitts* transconductor which achieves a wide tuning range and good linearity [23].
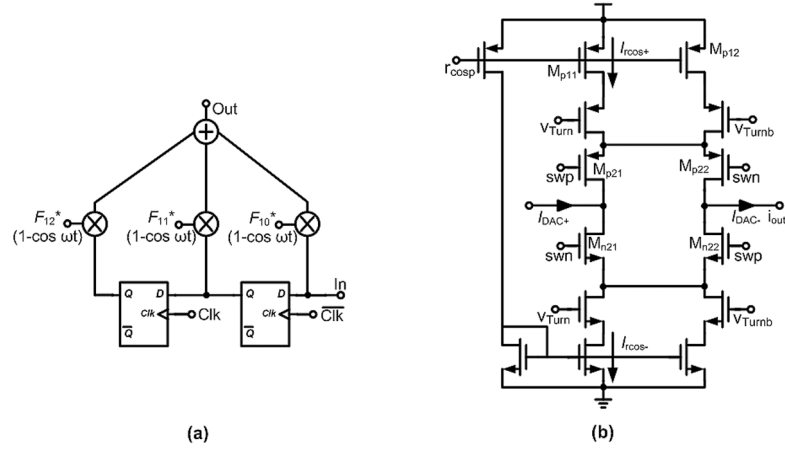
Fig. 9. (a) Three-tap raised-cosine FIR filter and (b) a DAC cell showing raised-cosine waveforms from the QPLL. V_{turn} and V_{turnb} are used to switch between the two Nyquist zones.

Q tuning is implemented using a 5-bit programmable current source for both sides of the transformer.

3) Input-Impedance Matching With Package Effects: The input impedance of the single-ended LNA including package effects is

$$Zin = \frac{1}{sC_{\text{oc}}} \left\| \left(sL_{\text{bw}} + R_{\text{bw}} + \left(R_{\text{in}} \left\| \frac{1}{sC_{\text{in}}} \right) \right) \right. \quad (6)$$

where L_{bw} and R_{bw} are the inductance and resistance of the bond-wire; C_{oc} models the parasitic capacitance of the lead-frame and soldering pad on the test-board and C_{in} is the total capacitance looking into M_1. Typical values are: $C_{\text{oc}} = 1.2$ pF, $R_{\text{bw}} = 2$ Ω, $L_{\text{bw}} = 2$ nH and $C_{\text{in}} = 100$ fF. Note that smaller C_{oc} gives a better input match. With $R_s = 50$ Ω and a balun ratio of 1:1, $R_{\text{in}} = 25$ Ω achieves superior $|S_{11}| = (Z_{\text{in}} - R_s/2)/(Z_{\text{in}} + R_s/2)$. Reducing R_{in} to 11 Ω improves linearity but reduces the bandwidth. The transistor bias points and device sizes are optimized for 22 Ω of differential impedance obtained using a 3:2 balun at the input. R_{in} varies from 12 Ω at 0.8 GHz to about 8 Ω at 2.4 GHz.

B. Three-Tap FIR Raised-Cosine D/A Converter

The DAC uses 3-tap FIR filters and raised-cosine DACs in the feedback loop (Fig. 9(a)). The output currents correspond to the coefficients in Table II.

A raised-cosine tap is shown in Fig. 9(b) wherein a current-steering DAC regulates the maximum DC current to realize the required coefficient value. The sinusoidal currents $I_{\text{rcos}+}$ and $I_{\text{rcos}-}$ are diverted to the positive or negative output through nMOS ($M_{\text{N21}}/M_{\text{N22}}$) and pMOS ($M_{\text{P21}}/M_{\text{P22}}$) switches. The switches are sized for high output impedance and minimal loading of the resonator. The differential output signals, $I_{\text{DAC}+}$ and $I_{\text{DAC}-}$, vary from $+200$ μA to -200 μA. The DAC is configured to operate in the first- or second-Nyquist zone by switching V_{Turn} or V_{Turnb} in tandem with the mode of the transformer.

The input to M_{P11} is a small sinusoidal signal with peak-to-peak amplitude scalable from 50–150 mV. Conventional DAC designs use a reduced swing at the output of the switch drivers to reduce charge injection which reduces the switching speed.

In contrast, a full-swing switch driver is used in this design [33] for high speed switching. The half-cycle delay is achieved using a dynamic SR-latch with a half cycle delayed clock. Rise/fall times of 95/97 ps are achieved with the latch.

C. Time-Interleaved Comparator With Shunt-Peaked Pre-Amplifier

The quantizer uses two interleaved comparators to halve the sampling rate of the each (Fig. 10). Thus, each comparator has more time to settle ($\sim$312.5 ps) which saves power compared to a single comparator operating at 3.2 GHz.

The regeneration- and tracking-mode time constants of the comparator are reduced using shunt-peaking. The resulting bandwidth extension reduces the power dissipation for a given sampling speed [34]. The optimal inductance is $L = R^2 C/1.41$ for the maximum tracking bandwidth. Another important aspect to note is that the input signal amplitude is only 5–40 mV at the pre-amplifier input. Hence, the common-source pre-amplifier is used to generate sufficiently large swings for the latch stage. Time interleaving also allows sufficient time to track the small-signal swings at the inputs. An additional D-type flip-flop (not shown) inserted after the comparator holds the data for an extra clock period to alleviate meta-stability and excess loop delay concerns.

D. 3.2 GHz Integer-N Harmonic-Rejection Injection-Locked Quadrature PLL

The spectral purity of the frequency synthesizer used to synchronize the DAC and comparator is critical to the overall performance of the RFADC. A phase-locked loop that uses charge pumps (CP-PLLs) is widely used because of its wide capture range and zero static-phase offset. However, mismatches in the source (UP) and sink (DN) currents combined with a low reference frequency cause close-in reference spurs that are not sufficiently filtered by the low-pass action of the PLL. Recently, a sub-sampling phase detector (SSPD) CP-PLL achieved a -80 dBc reference spur using a cancellation scheme wherein a separate SSPD-based delay-locked loop (DLL) generated a duty-cycle controlled reference signal [35]. In another design, a -70 dBc reference spur is achieved using a mismatch-cancelling
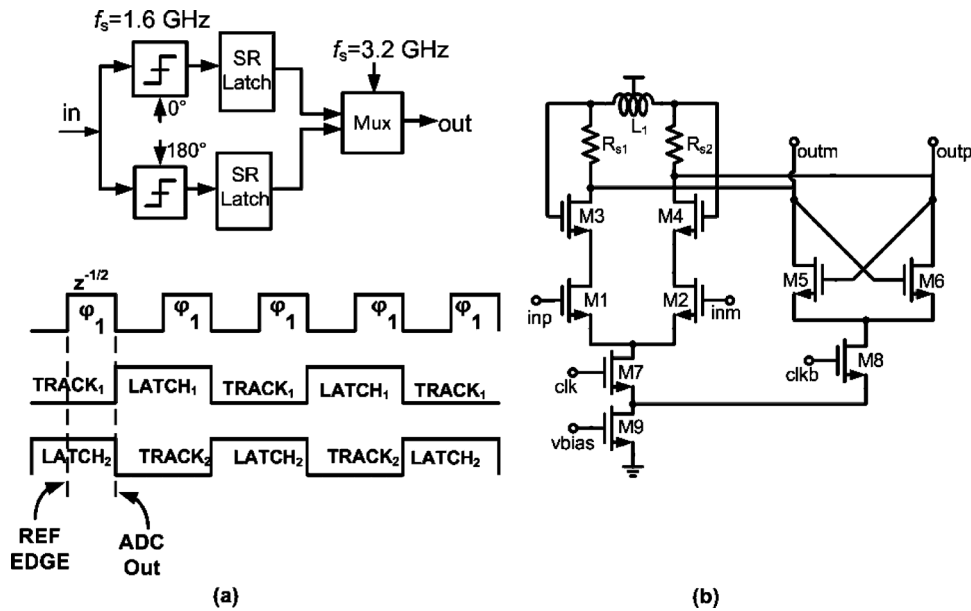
Fig. 10.   Time-interleaved 1-bit shunt-peaked comparator.

DAC with an offset CP and a sampled loop filter [36]. Also, a reference spur of -69.5 dBc is achieved using offline digital calibration of the UP/DN currents [37].

This section describes a CP-PLL that exhibits a -74.5 dBc reference spur without any digital calibration or mismatch cancellation to reduce area and power overhead. The type-II fourth-order quadrature PLL utilizes an injection-locked QVCO, a third-order loop filter and an additional out-of-band pole (Fig. 3(c)). The loop bandwidth is optimized to be the frequency offset at which the QVCO and PFD/CP have equal phase-noise contributions. This usually results in minimal peaking in the closed-loop transfer function. The out-of-band pole increases spur suppression without affecting loop stability. Mismatch in the UP/DN currents is the primary cause of a reference spur. When the loop is locked, mismatch results in a leakage current pulse injected into the loop filter every $1/f_{ref}$ period. The resulting reference spur may also cause in-band aliasing of the ADC quantization. A CP with enhanced linearity and matching (Fig. 11) eliminates the need for cancellation/calibration schemes. An off-chip resistor connected to V_{DD} supplies the bias current, I_{BIAS}, to the cascode current mirror ($M_{n1}-M_{n4}$). I_{BIAS} is mirrored into $M_{p2}-M_{p4}$ and $M_{n5}-M_{n7}$. $M_{p9}-M_{p10}$ or $M_{n13}-M_{n14}$ enable current steering to minimize charge sharing at the sources. Cascode devices M_{p6} and M_{n10} increase the output impedance and reduce charge feed-through. A replica circuit biased by M_{p3} and M_{n6} uses cascode devices M_{p5} and M_{n9} and current switches $M_{p7}-M_{p8}$ and $M_{n11}-M_{n12}$. However, both switches are always ON to replicate the current mirror outputs steered into the loop filter. Dummy capacitors placed at the drains of M_{p5} and M_{n9} match the output load capacitances. These techniques significantly reduce the CP current mismatches over PVT variations. Moreover, the closed-loop low-pass response and the out-of-band pole further suppress reference spurs. The CP requires $V_{DD} > 0.9$ V because of increased headroom for cascoding and is suitable for constant voltage process scaling.
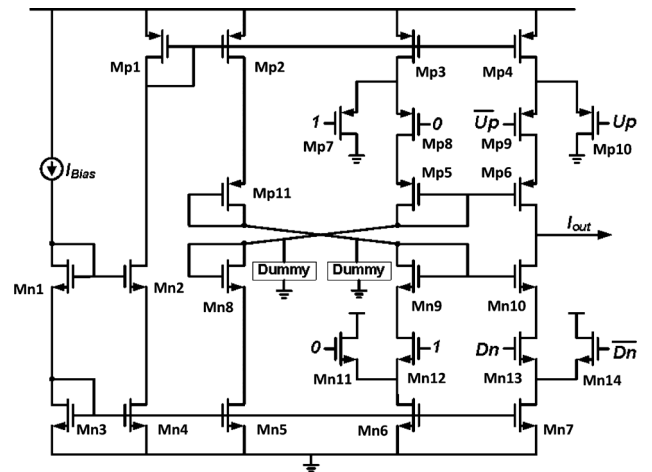

Fig. 11.   Charge-pump with enhanced linearity and matching.

Large CP UP/DN currents can be used to dominate mismatch currents to reduce the spurs and phase noise. However, the loop bandwidth is also increased which allows the PFD to dominate the phase-noise at higher offset frequencies. One solution to this problem is to use a sub-sampling PD wherein the phase noise is significantly smaller due to its divider-less operation [38]. Because the tri-state PFD-CP has a higher in-band phase noise, a lower loop bandwidth and a moderate CP current are preferred. The optimal CP UP/DN current in this design was found to be ~200 μA.

The quadrature voltage-controlled oscillator (QVCO) is the dominant power consuming block in the PLL. Its phase noise is inversely proportional to the bias current and output amplitude. The injection-locked LC-QVCO (IL-QVCO) (Fig. 12) uses cross-coupled pMOS transistors and series nMOS injection devices to achieve high injection strength and low phase-noise. The QVCO tail current employs an even-harmonic LC-tank tuned to $2f_{out}$ to minimize the coupling of spurious tones and

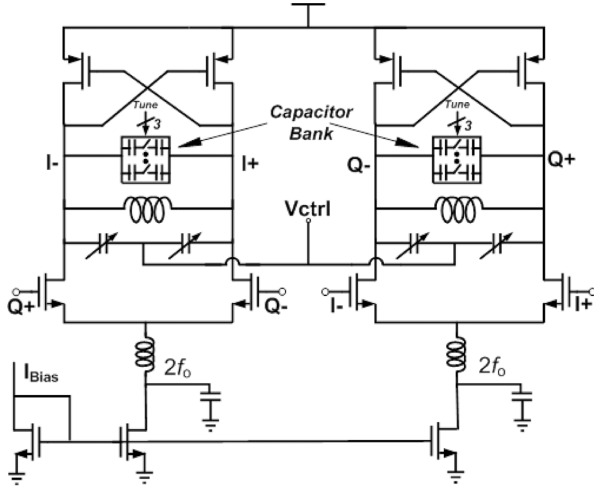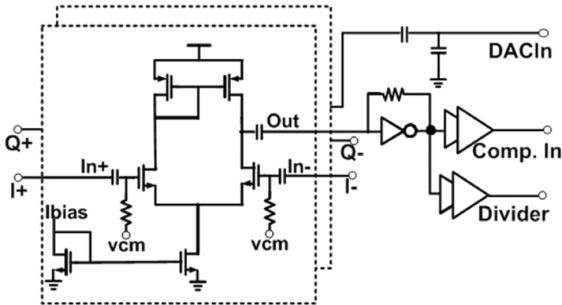Fig. 12. LC-based injection-locked QVCO (IL-QVCO).

Fig. 13. Buffer used to isolate the QVCO from capacitive loading.

Fig. 14. PCB with embedded CMOS chip using COB techniques.

Fig. 15. RFADC/PLL in 0.13 μm CMOS.

quantization noise from the ADC. A 3-bit binary-weighted frequency tuning network compensates for PVT variations. An actively-loaded differential amplifier (Fig. 13) isolates the QVCO from capacitive loading of the subsequent blocks and reduces reverse injection from the dividers and frequency pulling. A self-biased inverter centers the oscillations to $V_{\mathrm{DD}}/2$ and enhances the gain required to switch the output pad and divider chains [39]. A fixed 128X frequency divider locks the PLL to an external 25 MHz reference. Because of the high input frequency, the divider uses a true single-phase clocked (TSPC) DFF configured as a divide-by-2 pre-scalar operating at 3.2 GHz. This is followed by a divide-by-64 implemented with static DFFs. A conventional tri-state dead-zone-free PFD is used.

V. MEASUREMENT RESULTS

The prototype is embedded on a PCB using chip-on-board (COB) techniques to minimize parasitic inductances and capacitances. Several off-chip low-dropout (LDO) regulators are used to minimize the power supply noise. The PCB is shown in Fig. 14. An RF probe station and a digital sampling oscilloscope are used to ensure the integrity of the 1-bit output data from the ADC. A serial digital control port, I^2C, is used to control the on-chip tuning capacitors that switch the ADC between the two Nyquist zones. The ADC/PLL is implemented in 0.13 μm CMOS in 3 mm $\times$ 1.2 mm including test structures and pads (Fig. 15). A wide tuning range for a CT-BP-$\Sigma\Delta$ ADC is
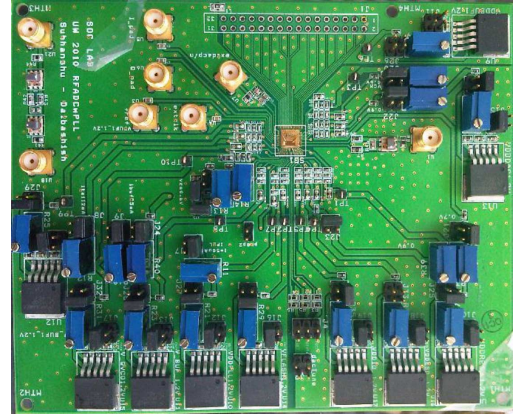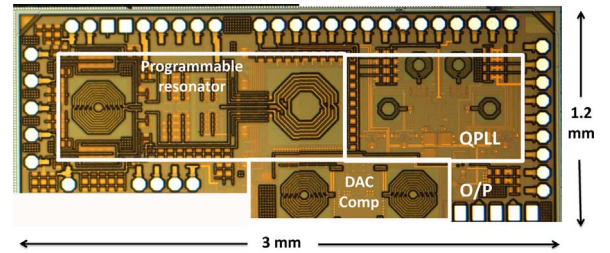
achieved with a total power consumption of only 41 mW with $V_{\mathrm{DD}} = 1.2$ V. Table III shows the power consumption breakdown of different blocks and Table IV compares its performance to other recent designs.

The phase noise of the 3.2 GHz PLL is measured using an Agilent E4446A spectrum analyzer. The in-band phase noise is -80 dBc whereas the out-of-band phase noise is -90 dBc, -113 dBc, and -139 dBc at 300 kHz, 1 MHz, and 10 MHz offset frequencies, respectively, as shown in Fig. 16. The in-band phase noise is limited by the PFD-CP which has a loop bandwidth of 325 KHz. This measured phase noise corresponds to an RMS jitter of 1.38 ps. Fig. 17 shows the measured reference spur with a 3.2 GHz output frequency locked to a 25 MHz external reference. The worst-case spur of -74.5 dBc is one of the lowest reported for a divider-based CP-PLL. An Agilent TDS8200 digital sampling oscilloscope was used to measure the quadrature phase error (Fig. 18). An I-Q mismatch of 0.63 degrees is achieved at the highest (i.e., worst-case) QVCO frequency of 3.52 GHz.

Fig. 19 shows the output spectra for input frequencies of 777 MHz and 1.827 GHz. The self-biased inverters used in the buffer path cause harmonic tones at higher sampling frequencies, which are reduced at a higher supply voltage of 1.4 V. Two input tones at -35 dBm are applied to the RF input for measuring dynamic range. The signal power for this two-tone test is -10 dBFS per tone. The IM3 power is -50.1 dBFS which yields an output-referred third-order intermodulation of 10 dBFS ($\mathrm{OIP3} = 3/2\mathrm{P_{sig}} - 1/2\mathrm{P_{IM3}}$). The integrated noise power over a 3.84 MHz channel is -62 dBFS. The two-tone spurious-free dynamic range (SFDR) is thus measured as 52 dB where $\mathrm{SFDR} = 2/3(\mathrm{OIP_3} - P_{\mathrm{noise}} + 10\log(\mathrm{RBW/MHz}))$.

TABLE IV
COMPARISON OF RFADCs FOR SDR APPLICATIONS

	This work	[11]	[13]	[6]	[20]
Topology	Second-order BP ΣΔ	Fourth-order BP ΣΔ	Sixth-order BP ΣΔ	LP ΣΔ / Passive Mixer	Second-order BP ΣΔ
Center Freq. (GHz)	0.8 – 2	950	2.4	0.4 - 1.7	2.4
Clock Freq. (GHz)	1.6/3.2 (2.6-3.4)	3.8	3	0.4 - 1.7	3.2
SNR (dB) (Norm. to 1 MHz)	50 - 40	59	48	62	42
SFDR (dB)	52 - 42	-	70	60	-
3-dB BW Noise Notch (MHz)	40	1	60	1	25
Power (mW)	41 (30+11) (ADC + PLL)	75 (no PLL)	40 (no PLL)	50.4 (no PLL)	26 (no PLL)
Area (mm²)	2.3	1.36	0.8	0.8	0.27
IIP3 (dBm)	-5 / -7	-	-9	19	
RX Sensitivity (dBm)	-75 / -65	-77	-	-	-
Reconfigurability	Yes	No	No	Yes	No
Technology	0.13 μm CMOS	0.25 μm SiGe	90 nm CMOS	90 nm CMOS	0.13 μm CMOS
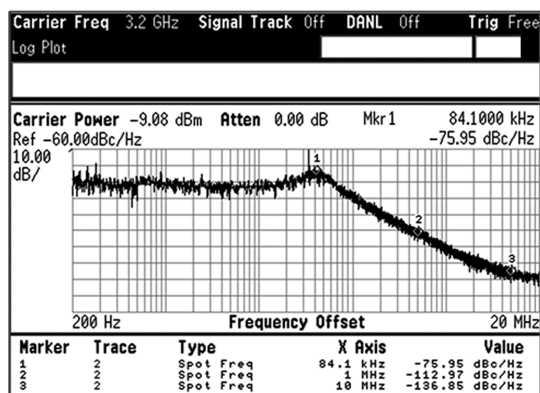
Fig. 16. Phase noise of the PLL measured using an Agilent E4446A spectrum analyzer is < -110 dBc/Hz at an offset frequency of 1 MHz.
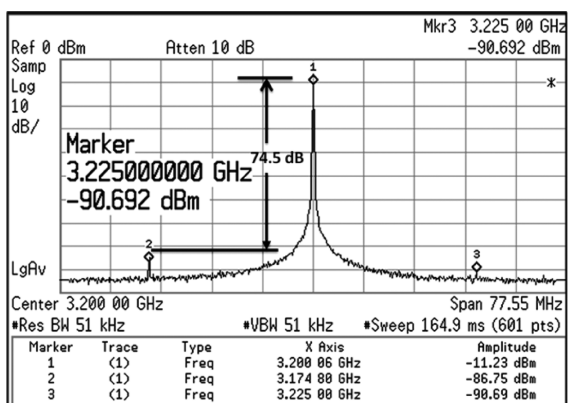

Fig. 17. Worst-case spur is -74.5 dBc for the 3.2 GHz output locked to a 25 MHz external reference.

Measured third-order intercept points for input frequencies of 796.5 MHz, 1.0015 GHz and 1.924 GHz are -5 dBm, -5.5 dBm, and -6.7 dBm, respectively (Fig. 20(a)). The integrated noise values over a 1 MHz bandwidth about 796.5 MHz and 1.0015 GHz result in maximum signal-to-(noise+distortion) ratios (SNDR) of 50 dB and 48 dB (Fig. 20(b)). Measured
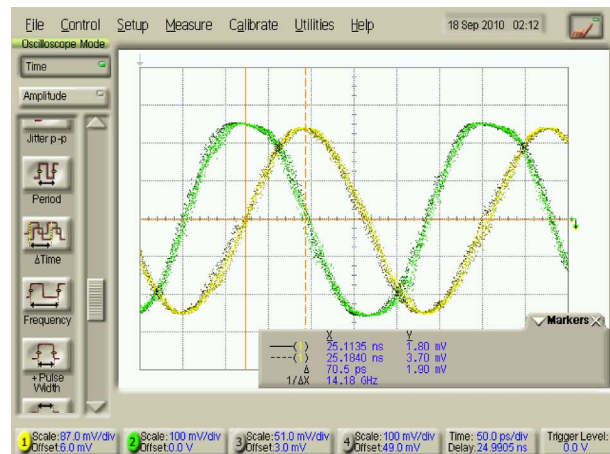

Fig. 18. Measured quadrature phase error between I and Q paths is 0.63 degrees at the highest QVCO frequency of 3.52 GHz.

SNDR values for a 20 MHz bandwidth are 36 dB and 38 dB, respectively. The highest dynamic range is obtained for moderate Q-enhancement and low input-g_m in a single-tone environment as expected. The ADC can also be reconfigured using 3X/5X under-sampling factors where its functionality is verified for sampling frequency of 1.6 GHz.

VI. CONCLUSION

With the increasing demand for single-chip solutions for multi-standard, compact form factor, low-power wireless transceivers, the RF signal is being digitized ever closer to the antenna. Through system- and circuit-level innovations, this paper introduces a fully-integrated highly-reconfigurable (0.8–2 GHz) bandpass $\Sigma\Delta$ RFADC-PLL system. The architecture achieves low-power with reduced circuit complexity by operating in both the first- and second-Nyquist zones with minimal required tuning. The prototype implemented in 0.13 μm CMOS, features a highly-programmable narrowband resonator, a reconfigurable pulse-shaping DAC and a harmonic-rejection injection-locked quadrature PLL for phase synchronization. The chip consumes only 41 mW in 2.8 mm². Future work
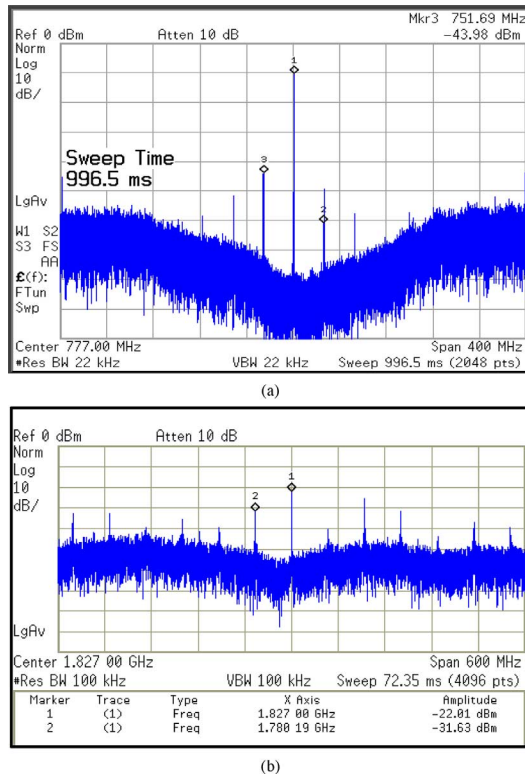
Fig. 19. Measured output spectra at input frequencies of 777 MHz and 1.827 GHz where the ADC operates in the first- and second-Nyquist zones, respectively. It exhibits second-order noise shaping which is not limited by jitter.
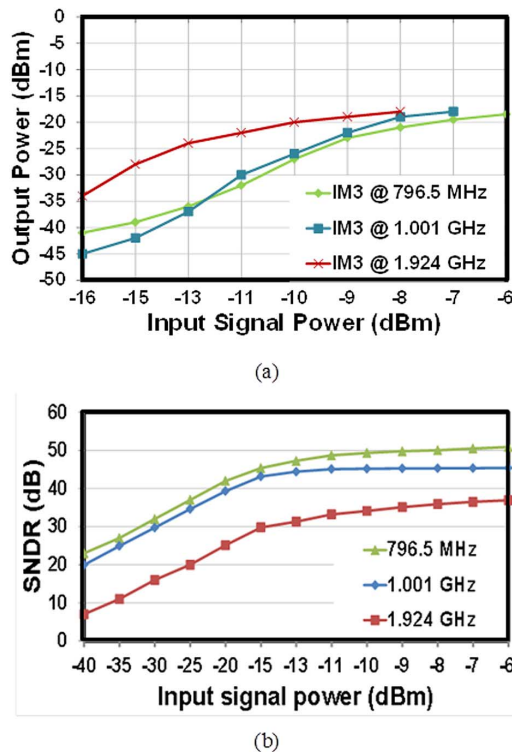

Fig. 20. (a) Measured ADC linearity at 796.6 MHz, 1.001 GHz and 1.924 GHz, respectively. (b) Measured SNDR at the same frequencies.

includes integration of wideband reconfigurable blocker reduction techniques to reduce the linearity constraints of the RFADC and enable true SDR operation.

REFERENCES

[1] G. Hueber, J. Zipper, R. Stuhlberger, and A. Holm, "An adaptive multi-mode RF front-end for cellular terminals," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, 2008, pp. 25–28.

[2] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz wideband IF double conversion CMOS integrated receiver for cordless telephone applications," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 1997, pp. 304–305, 476.

[3] V. Giannini, P. Nuzzo, C. Soens, K. Vengattaramane, M. Steyaert, J. Ryckaert, M. Goffioul, B. Debaillie, J. Van Driessche, J. Cranincks, and M. Ingels, "A 2 mm² 0.1-to-5 GHz SDR receiver in 45 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2009, pp. 408–409.

[4] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, M. Tang, and A. Abidi, "An 800 MHz to 5 GHz software-defined radio receiver in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2006, pp. 480–481, 667.

[5] R. Winoto and B. Nikolic, "A highly reconfigurable 400–1700 MHz receiver using a down-converting sigma-delta A/D with 59-dB SNR and 57-dB SFDR over 4-MHz bandwidth," in *Proc. IEEE Symp. VLSI Circuits*, 2009, pp. 142–143.

[6] S. Gupta, D. Gangopadhyay, H. Lakdawala, J. C. Rudell, and D. J. Allstot, "A QPLL-timed direct-RF sampling bandpass ΣΔ ADC with a 1.2 GHz tuning range in 0.13 μm CMOS," in *IEEE RFIC Symp. Dig.*, 2011, pp. 25–28.

[7] K. T. Tiew, A. J. Payne, and P. Y. K. Cheung, "MASH delta-sigma modulators for wideband and multi-standard applications," in *Proc. IEEE ISCAS*, 2001, pp. 778–781.

[8] S. A. Jantzi, W. M. Snelgrove, and P. F. Ferguson, Jr., "A fourth-order bandpass sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 282–291, Mar. 1993.

[9] J. F. Jensen, G. Raghavan, A. E. Cosand, and R. H. Walden, "A 3.2-GHz second-order delta-sigma modulator implemented in InP HBT technology," *IEEE J. Solid-State Circuits*, vol. 30, no. 10, pp. 1119–1127, Oct. 1995.

[10] O. Shoaei and W. M. Snelgrove, "Optimal (band-pass) continuous-time ΣΔ modulator," in *Proc. IEEE ISCAS*, 1994, pp. 489–492.

[11] W. Gao and W. M. Snelgrove, "A 950-MHz IF second-order integrated *LC* bandpass delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 723–732, May 1998.

[12] K. Koli, J. Jussila, P. Sivonen, S. Kallioinen, and A. Parssinen, "A 900 MHz direct ΔΣ receiver in 65-nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2010, pp. 64–65.

[13] J. Ryckaert, J. Borremans, B. Verbruggen, and L. Bos, "A 2.4 GHz low-power sixth-order RF bandpass ΣΔ converter in CMOS," *IEEE J. Solid-State Circuits*, vol. 44, pp. 2873–2880, Nov. 2009.

[14] R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 43, no. 4, pp. 324–332, Apr. 1996.

[15] F. Gerfers and M. Ortmanns, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. New York: Springer, 2006.

[16] S. Paton, A. Di Giandomenico, L. Hernandez, A. Wiesbauer, T. Potscher, and M. Clara, "A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.

[17] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 661–676, Jun. 1999.

[18] T. Kaplan, J. Cruz-Albrecht, M. Mokhtari, D. Matthews, J. Jensen, and M. F. Chang, "A 1.3-GHz IF digitizer using a 4th-order continuous-time bandpass ΔΣ modulator," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2003, pp. 127–130.

[19] S. Luschas, R. Schreier, and H.-S. Lee, "Radio frequency digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, Sep. 2004.

[20] T. Okamoto, Y. Maruyama, and A. Yukawa, "A stable high-order delta-sigma modulator with an FIR spectrum distributor," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 730–735, Jul. 1993.

[21] A. Kammoun, N. Beilleau, and H. Aboushady, "Undersampled *LC* bandpass $\Sigma\Delta$ modulators with feedback FIRDACs," in *Proc. IEEE ISCAS*, 2006, pp. 4427–4430.

[22] D. K. Su and B. A. Wooley, "A CMOS oversampling D/A converter with a current-mode semi-digital reconstruction filter," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 1993, pp. 230–231.

[23] X. Li, S. Shekhar, and D. J. Allstot, "G_m-boosted common-gate LNA and differential Colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[24] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[25] W. B. Kuhn, F. W. Stephenson, and A. Elshabini-Riad, "Dynamic range of high-Q OTA-C and enhanced-Q *LC* RF bandpass filters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, 1994, pp. 767–771.

[26] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proc. IEEE Custom Integr. Circuits Conf.*, 1998, pp. 555–558.

[27] A. Jerng and C. G. Sodini, "A wideband $\Delta\Sigma$ digital-RF modulator for high data rate transmitters," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1710–1722, Aug. 2007.

[28] A. D. Berny, A. M. Niknejad, and R. G. Meyer, "A 1.8-GHz *LC* VCO with 1.3-GHz tuning range and digital amplitude calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 909–917, Apr. 2005.

[29] S. T. Lee, S. J. Fang, D. J. Allstot, A. Bellaouar, A. R. Fridi, and P. A. Fontaine, "A quad-band GSM-GPRS transmitter with digital auto-calibration," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2200–2214, Dec. 2004.

[30] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.

[31] A. M. Niknejad, "Modeling of passive elements with ASITIC," in *IEEE RFIC Symp. Dig.*, 2002, pp. 303–306.

[32] J. S. Walling, "Theory and application of spiral transformers for silicon-based integrated circuits," Master's thesis, Dept. Elect. Eng., Univ. Washington, Seattle, 2005.

[33] S. Luschas and H.-S. Lee, "High-speed $\Sigma\Delta$ modulators with reduced timing jitter sensitivity," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 11, pp. 712–720, Nov. 2002.

[34] S. Park, Y. Palaskas, and M. P. Flynn, "A 4-GS/s 4-bit flash ADC in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1865–1872, Sep. 2007.

[35] X. Gao, E. A. M. Klumperink, G. Socci, M. Bohsali, and B. Nauta, "Spur-reduction techniques for PLLs using sub-sampling phase detection," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2010, pp. 474–475.

[36] K. J. Wang, A. Swaminathan, and I. Galton, "Spurious tone suppression techniques applied to wide-bandwidth 2.4 GHz fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2008.

[37] C.-F. Liang, S. H. Chen, and S. I. Liu, "A digital calibration technique for charge pumps in phase-locked systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 390–398, Feb. 2008.

[38] S. Pellarano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, Feb. 2004.

[39] S. Shekhar, J. S. Walling, S. Aniruddhan, and D. J. Allstot, "CMOS VCO and LNA using tuned-input tuned-output circuits," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1177–1186, May 2008.

Subhanshu Gupta (S'03–M'11) received the B.E. degree from the National Institute of Technology, Trichy, India in 2002, and the M.S. and Ph.D. degrees from the University of Washington, Seattle, in 2006 and 2010, respectively.

He interned with National Semiconductor (now Texas Instruments), Santa Clara, CA from 2005 to 2006 where he worked on high-resolution sigma-delta ADCs. Since 2011, he has been with RFIC/Mixed Signal group at Maxlinear Inc., Irvine, CA, working on wideband analog-to-digital converters for satellite/cable TV applications. His current research interests include architectures for direct-RF wideband sampling ADCs, techniques for mitigating blockers/interferers in radio receivers and applications of digital signal processing algorithms to CMOS receiver design for low-power and area efficiency.

Dr. Gupta received the Analog Devices Outstanding Student Designer Award in 2008 and an IEEE RFIC Symposium Best Student Paper Award in 2011.

Daibashish Gangopadhyay (S'06–M'11) received the B.S. (hons) and M.S. degrees in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India in 2005 and 2006, respectively, and the Ph.D. degree from the University of Washington, Seattle, in 2011.

During 2008–2009, he was an intern with the Qualcomm Research Center, San Diego, CA, where he worked on biomedical sensor circuits for personal area network applications. Since 2011, he has been with the RF-Analog Group, Marvell Semiconductors, Santa Clara, CA. His research interests include CMOS frequency synthesizers, software-defined radio receivers, RF and analog front-ends for biomedical sensors applications and Compressed Sensing.

Dr. Gangopadhyay received the Analog Devices Outstanding Student Designer Award in 2010 and an IEEE RFIC Symposium Best Student Paper Award in 2011.

Hasnain Lakdawala (S'96–M'03) received the B.S. degree from the Indian Institute of Technology, Bombay, India, in 1995, and the M.S. degree from the University of Hawaii, Manoa, in 1997, both in electrical engineering. He received the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 2002.

From 2002 to 2004, he was a Product Architect at IC Mechanics, Inc., Pittsburgh, responsible for the development of single-chip CMOS-based HDD shock sensors. He has been a Research Scientist at Intel Corporation, Hillsboro, OR, since 2004. His research interests include RF and analog circuits for WLAN transceivers that exploit scaled CMOS processes. He holds 13 issued and several pending patents. He has published over 50 conference/journal papers and serves on the technical program committee of IEEE CICC conference.

Jacques C. Rudell (S'94–M'00–SM'09) received the B.S. degree in electrical engineering from the University of Michigan, Ann Arbor, and the M.S.E.E. and Ph.D. degrees from the University of California at Berkeley.

From 1989 to 1991, he was an IC Design Engineer and Project Manager with Delco Electronics (now Delphi), where his work focused mainly on bipolar analog circuits for automotive applications. From late 2000 to 2001, he was a postdoctoral Researcher at the University of California at Berkeley, in addition to holding consulting positions in several Silicon Valley firms. In late 2001, he joined Berkana Wireless (now Qualcomm), San Jose, CA as an Analog/RF IC Design Engineer and later became the Design Manager of the Advanced IC Development Group. From September 2005 until December 2008, Dr. Rudell was with the Advanced Radio Technology Group at Intel. In 2009, he transitioned back to academia as an Assistant Professor of Electrical Engineering at the University of Washington, Seattle.

Dr. Rudell received the Demetri Angelakos Memorial Achievement Award in 2000, a citation given to one student per year by the EECS Department, UC Berkeley. He received the 1998 ISSCC Jack Kilby Best Student Paper Award and was the co-recipient of the 2001 ISSCC Lewis Best Paper Award. He also received an award at the 2008 ISSCC for best evening session. He was a technical program committee member for the International Solid-State Circuits Conference (ISSCC) from 2004 to 2011. Dr. Rudell also serves on the MTT-IMS Radio Frequency Integrated Circuits (RFIC) Symposium steering committee where he is currently the Technical Program Committee Chair. He is also an Associate Editor for the Journal of Solid-State Circuits.

David J. Allstot (S'72–M'72–SM'83–F'92) received the B.S. degree from the University of Portland, Portland, OR, the M.S. degree from Oregon State University, Corvallis, OR, and the Ph.D. degree and the University of California, Berkeley.

He has held several industrial and academic positions and has been the Boeing-Egtvedt Chair Professor of Engineering at the University of Washington, Seattle, since 1999. He was Chair of the Department of Electrical Engineering from 2004 to 2007. He is currently a Visiting Professor of Electrical Engineering at Stanford University, Stanford, CA.

Dr. Allstot has advised approximately 100 M.S. and Ph.D. graduates, published more than 300 papers, and received several awards for outstanding teaching and graduate advising including the 1980 IEEE W. R. G. Baker Award, 1995 and 2010 IEEE Circuits and Systems Society (CASS) Darlington Award, 1998 IEEE International Solid-State Circuits Conference (ISSCC) Beatrice Winner Award, 1999 IEEE CASS Golden Jubilee Medal, 2004 IEEE CASS Charles A. Desoer Technical Achievement Award, 2005 Semiconductor Research Corp. Aristotle Award, 2008 Semiconductor Industries Assoc. University Research Award, and 2011 IEEE CASS Mac Van Valkenburg Award. His service includes: 1990–1993 Assoc. Editor and 1993–1995 Editor of IEEE TCAS II, 1990–93 Member of Technical Program Committee of the IEEE CICC Conference, 1992–1995 Member, Board of Governors of IEEE CASS, 1994–2004, Member, Technical Program Committee, IEEE ISSCC, 1995–1997, 2001, 2003–2004, Member, Executive Committee of IEEE ISSCC, 1996–2000 Short Course Chair of IEEE ISSCC, 2000–2001 Distinguished Lecturer, IEEE CASS, 2001 and 2008 Co-General Chair of IEEE ISCAS, 2006–2007 Distinguished Lecturer, IEEE Solid-State Circuits Society and 2009 President of IEEE CASS.